

NEC

IC Memory

1995 Data Book

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The information in this document is based on documents issued in January, 1995 at the latest. The information is subject to change without notice. For the actual design-in refer to the latest publications of data sheet, etc. for the most up-date specifications of the device.

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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Anti-radioactive design is not implemented in this product.

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 - 特別水準：輸送機器（自動車、列車、船舶等）、交通用信号機器、防災／防犯装置、各種安全装置、生命維持を直接の目的としない医療機器
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Rambus DRAM919

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DRAM Module (2/2) 1175

SO DIMM	3.3V	16MB	4M × 32	MC-42S4000LAB32S SERIES 1175
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		4MB	1M × 32	MC-42S1000LAA32S SERIES 1243
				MC-42S1000LAD32S SERIES 1259

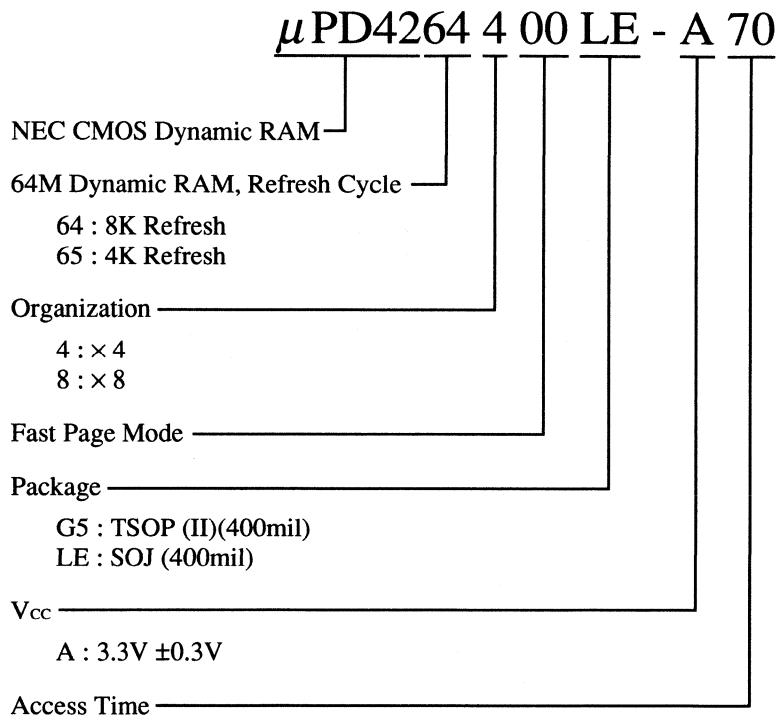
8 Byte DIMM	5.0V	32MB	4M × 72	MC-424000AB72F 1277
				MC-424000AC72F 1297
		16MB	2M × 72	MC-422000AB72F 1317
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	3.3V	32MB	4M × 72	MC-424000LAB72F 1403
		16MB	2M × 72	MC-422000LAB72F 1425



Selection Guide

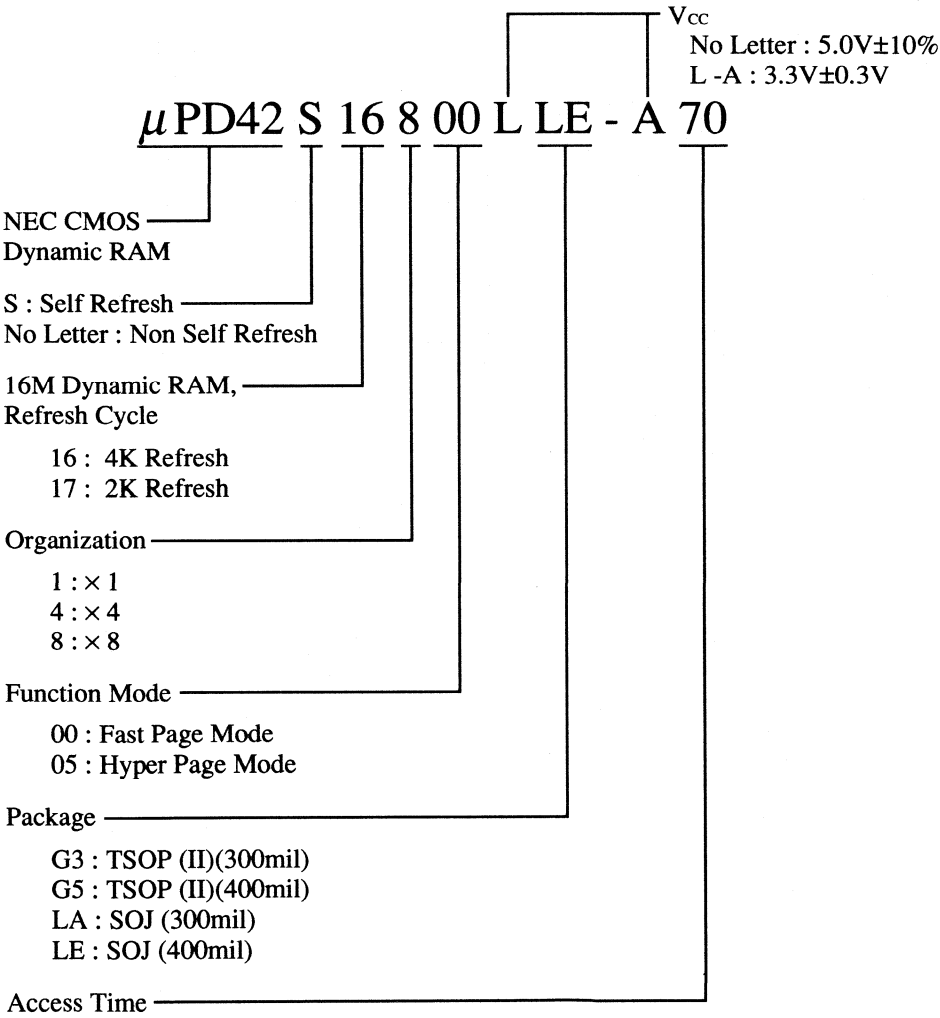
Part Number

64M DRAM

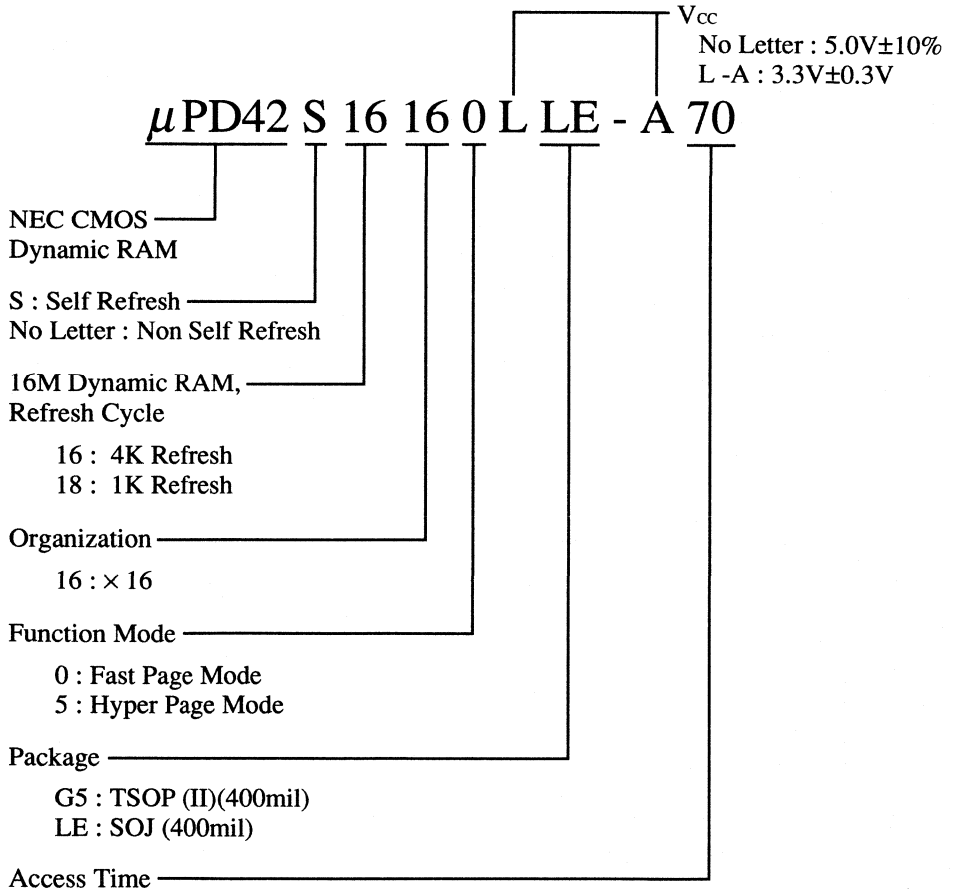


16M DRAM

(1) × 1 / × 4 / × 8

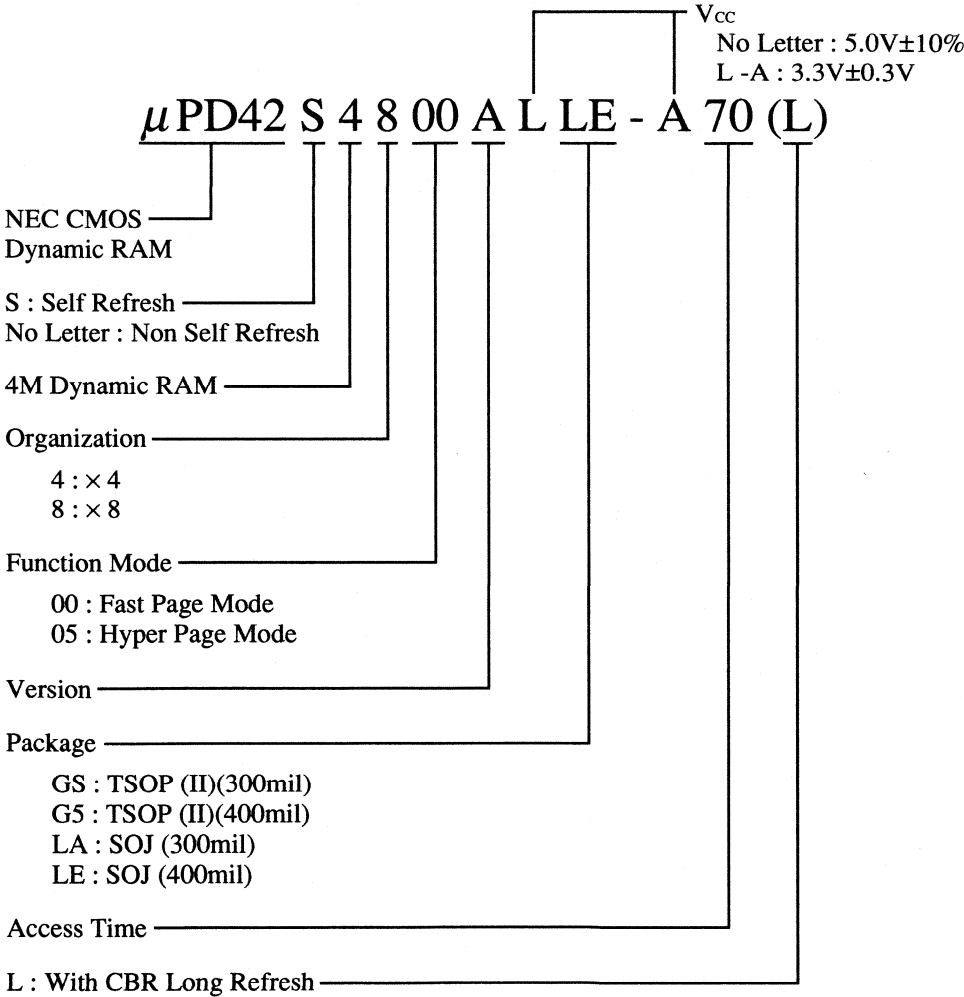


(2) × 16

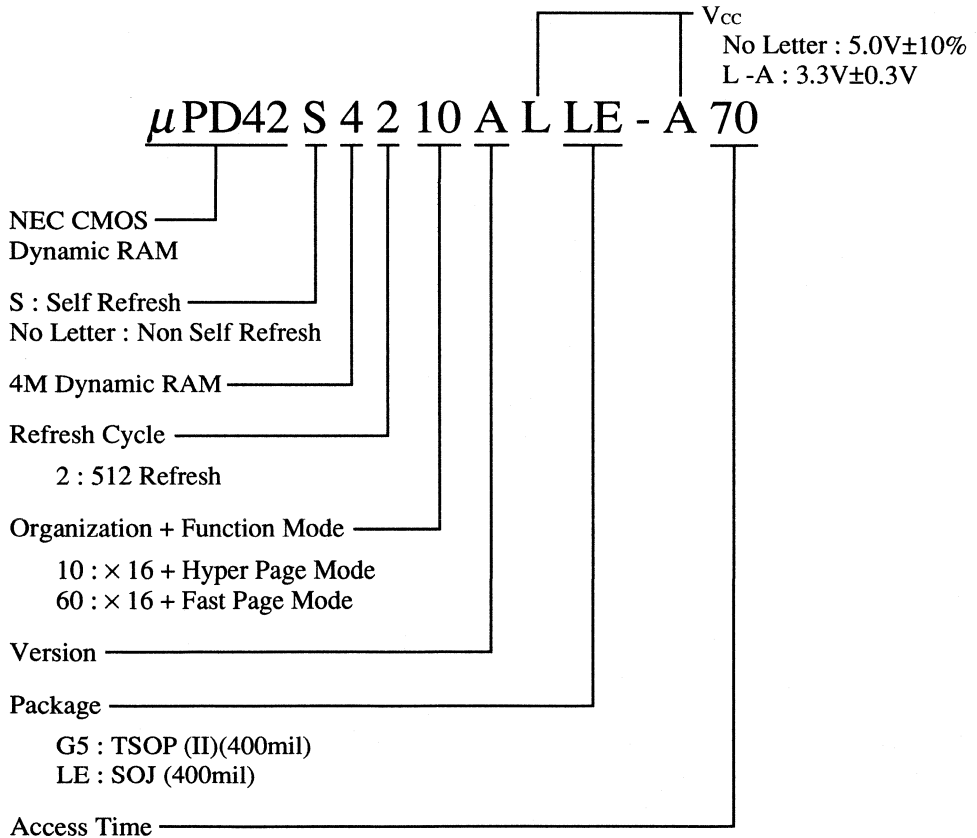


4M DRAM

(1) × 4 / × 8

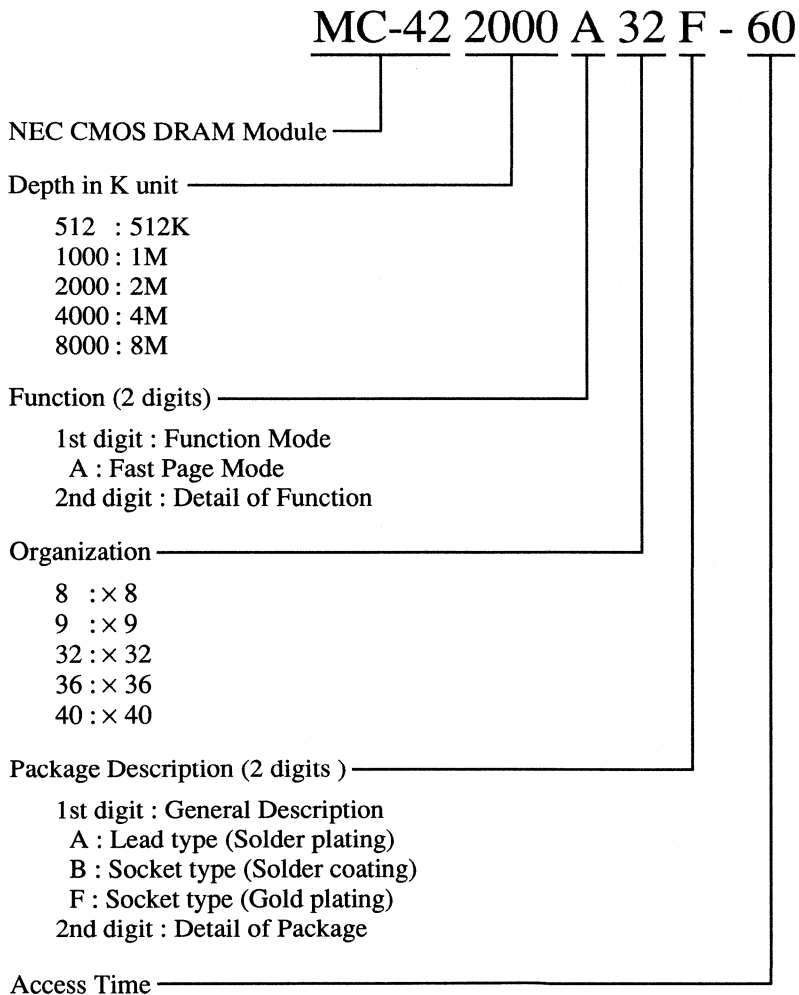


(2) × 16

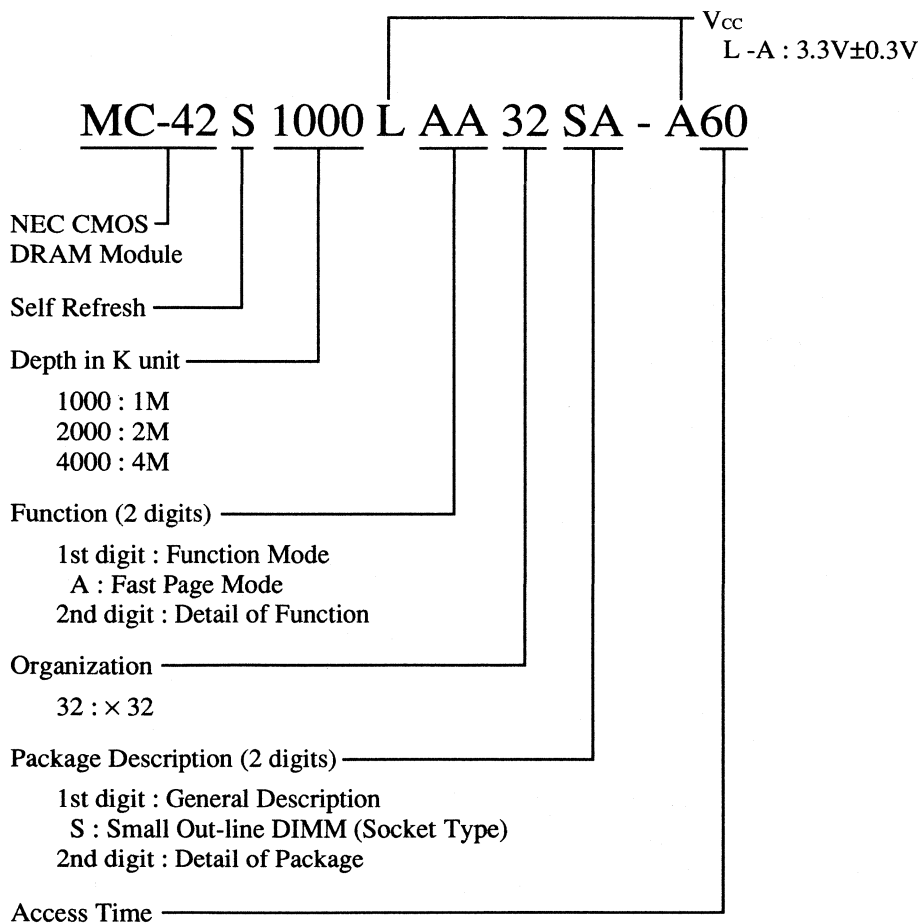


DRAM Module

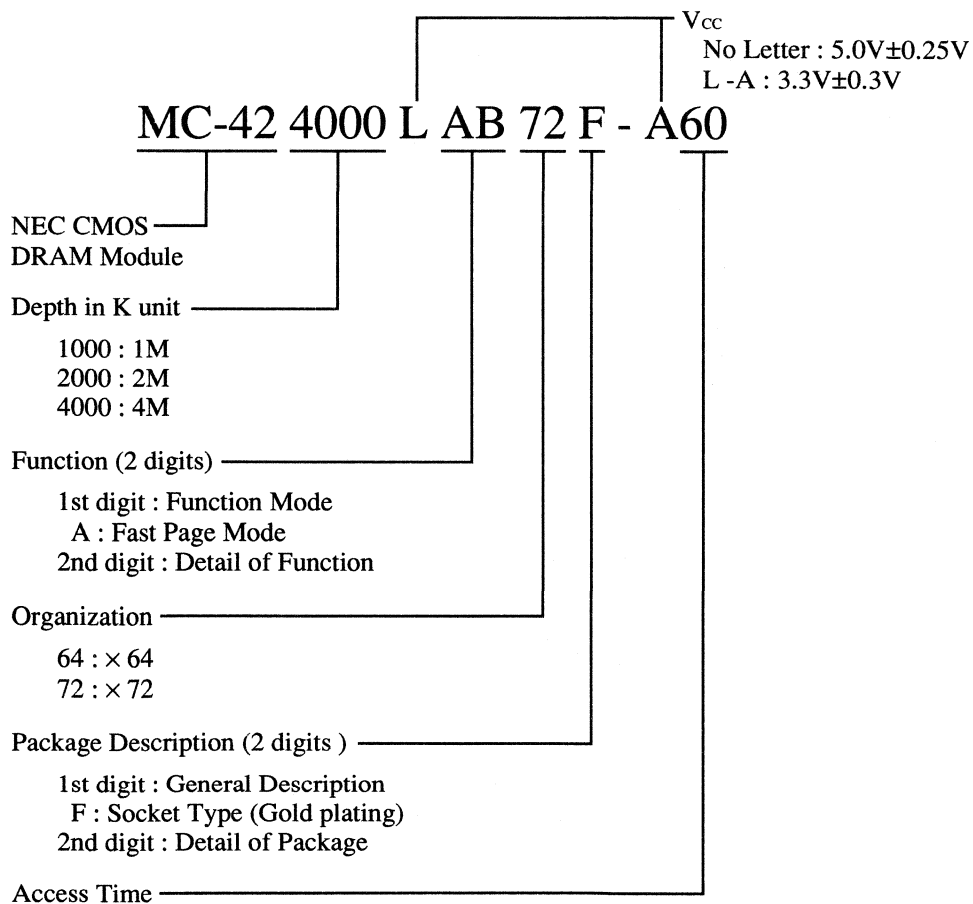
30, 72-pin SIMM



72-pin SO DIMM



168-pin 8Byte DIMM





64M Dynamic RAM

MOS INTEGRATED CIRCUIT

μ PD4264400, 4265400

64 M-BIT DYNAMIC RAM

16 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μ PD4264400, 4265400 are 16,777,216 words by 4 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

These are packaged in 32-pin plastic TSOP(III) and 32-pin plastic SOJ.

Features

- 16,777,216 words by 4 bits organization
- Single +3.3 V $\pm$ 0.3 V power supply
- Fast access and cycle time

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μ PD4264400-A50	360 mW	1.80 mW (CMOS level input)	50 ns	90 ns	35 ns
μ PD4265400-A50	468 mW				
μ PD4264400-A60	324 mW		60 ns	110 ns	40 ns
μ PD4265400-A60	396 mW				
μ PD4264400-A70	288 mW		70 ns	130 ns	45 ns
μ PD4265400-A70	360 mW				
μ PD4264400-A80	252 mW		80 ns	150 ns	50 ns
μ PD4265400-A80	324 mW				

- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh

Part number	Row address	Column address	Refresh	Refresh cycle
μ PD4264400	A0 - A12	A0 - A10	$\overline{\text{RAS}}$ only refresh, Normal read/write	8,192 cycles/64 ms
			$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh	4,096 cycles/64 ms
μ PD4265400	A0 - A11	A0 - A11	$\overline{\text{RAS}}$ only refresh, Normal read/write,	4,096 cycles/64 ms
			$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh	

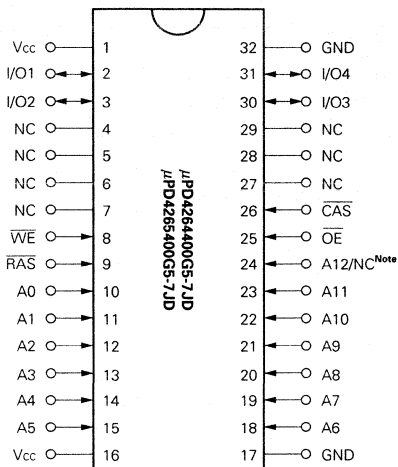
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Ordering Information

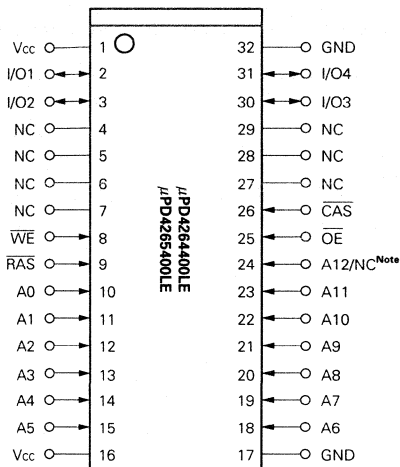
Part number	Access time (MAX.)	Package	Refresh
μ PD4264400G5-A50-7JD	50 ns	32-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4264400G5-A60-7JD	60 ns		
μ PD4264400G5-A70-7JD	70 ns		
μ PD4264400G5-A80-7JD	80 ns		
μ PD4264400LE-A50	50 ns	32-pin Plastic SOJ (400 mil)	
μ PD4264400LE-A60	60 ns		
μ PD4264400LE-A70	70 ns		
μ PD4264400LE-A80	80 ns		
μ PD4265400G5-A50-7JD	50 ns	32-pin Plastic TSOP (II) (400 mil)	
μ PD4265400G5-A60-7JD	60 ns		
μ PD4265400G5-A70-7JD	70 ns		
μ PD4265400G5-A80-7JD	80 ns		
μ PD4265400LE-A50	50 ns	32-pin Plastic SOJ (400 mil)	
μ PD4265400LE-A60	60 ns		
μ PD4265400LE-A70	70 ns		
μ PD4265400LE-A80	80 ns		

Pin Configurations (Marking Side)

32-pin Plastic TSOP (II) (400 mil)



32-pin Plastic SOJ (400 mil)



Note A12 ... μPD4264400

NC ... μPD4265400

A0 to A12 : Address Inputs

I/O1 to I/O4 : Data Inputs/Outputs

$\overline{\text{RAS}}$: Row Address Strobe

$\overline{\text{CAS}}$: Column Address Strobe

$\overline{\text{WE}}$: Write Enable

$\overline{\text{OE}}$: Output Enable

Vcc : Power Supply

GND : Ground

NC : No Connection

Input/Output Pin Functions

The μ PD4264400, 4265400 have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, Address^{Note} and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)	Input	$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A _x ^{Note} (Address inputs)	Input	Address bus. Input total 24-bit of address signal, upper bits and lower bits ^{Note} in sequence (address multiplex method). Therefore, one word is selected from 16,777,216-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μ PD4264400	A0-A12	13	11
μ PD4265400	A0-A11	12	12

Electrical Specifications (Preliminary)

- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_O		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{Stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	
Data input/output capacitance	C_{IO}	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

[μ PD4264400]

Parameter	Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling trc = trc (MIN.) I _O = 0 mA	trac = 50 ns		100	mA	1, 2, 3
			trac = 60 ns		90		
			trac = 70 ns		80		
			trac = 80 ns		70		
Standby current	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$, I _O = 0 mA			1.0	mA	
		$\overline{\text{RAS}}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$, I _O = 0 mA			0.5		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$ trc = trc (MIN.), I _O = 0 mA	trac = 50 ns		100	mA	1, 2, 3, 4
			trac = 60 ns		90		
			trac = 70 ns		80		
			trac = 80 ns		70		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{IL}(\text{MAX.})$, $\overline{\text{CAS}}$ Cycling tpc = tpc (MIN.), I _O = 0 mA	trac = 50 ns		80	mA	1, 2, 5
			trac = 60 ns		70		
			trac = 70 ns		60		
			trac = 80 ns		50		
CAS before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling trc = trc (MIN.) I _O = 0 mA	trac = 50 ns		130	mA	1, 2
			trac = 60 ns		110		
			trac = 70 ns		100		
			trac = 80 ns		90		
Input leakage current	I _{I (L)}	V _I = 0 to 3.6 V All other pins not under test = 0 V		-5	+5	μ A	
Output leakage current	I _{O (L)}	V _O = 0 to 3.6 V Output is disabled (Hi-Z)		-5	+5	μ A	
High level output voltage	V _{OH}	I _O = -2.0 mA		2.4		V	
Low level output voltage	V _{OL}	I _O = +2.0 mA			0.4	V	

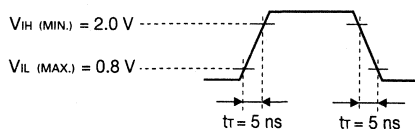
[μ PD4265400]

Parameter	Symbol	Test Condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling		130	mA	1, 2, 3
		tr _{AC} = 50 ns				
		tr _C = tr _C (MIN.), I _O = 0 mA		110		
				100		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$		1.0	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$		0.5		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.})$		130	mA	1, 2, 3, 4
		tr _C = tr _C (MIN.), I _O = 0 mA		110		
				100		
				90		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}} (\text{MAX.}), \overline{\text{CAS}}$ Cycling		80	mA	1, 2, 5
		tr _C = tr _C (MIN.), I _O = 0 mA		70		
				60		
				50		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling		130	mA	1, 2
		tr _C = tr _C (MIN.), I _O = 0 mA		110		
				100		
				90		
Input leakage current	I _I (I _L)	V _I = 0 to 3.6 V All other pins not under test = 0 V	-5	+5	μ A	
Output leakage current	I _O (I _L)	V _O = 0 to 3.6 V Output is disabled (Hi-Z)	-5	+5	μ A	
High level output voltage	V _{OH}	I _O = -2.0 mA	2.4		V	
Low level output voltage	V _{OL}	I _O = +2.0 mA		0.4	V	

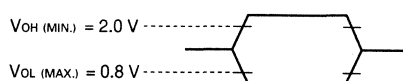
Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (tr_C and tr_C).**2.** Specified values are obtained with outputs unloaded.**3.** I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}} (\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.})$.**4.** I_{CC3} is measured assuming that all column address inputs are held at either high or low.**5.** I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)**AC characteristics Test Conditions**

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	trac = 50 ns		trac = 60 ns		trac = 70 ns		trac = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	trc	90	–	110	–	130	–	150	–	ns	
RAS Precharge Time	trp	30	–	40	–	50	–	60	–	ns	
CAS Precharge Time	tcpn	8	–	10	–	10	–	10	–	ns	
RAS Pulse Width	trās	50	10,000	60	10,000	70	10,000	80	10,000	ns	
CAS Pulse Width	tcās	13	10,000	15	10,000	18	10,000	20	10,000	ns	
RAS Hold Time	trsh	13	–	15	–	18	–	20	–	ns	
CAS Hold Time	tcsH	50	–	60	–	70	–	80	–	ns	
RAS to CAS Delay Time	trcd	18	32	20	45	20	50	25	60	ns	1
RAS to Column Address Delay Time	trad	13	25	15	30	15	35	17	40	ns	1
CAS to RAS Precharge Time	tcRP	5	–	5	–	5	–	5	–	ns	2
Row Address Setup Time	tasR	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	trah	8	–	10	–	10	–	12	–	ns	
Column Address Setup Time	tasc	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	tcaH	13	–	15	–	15	–	15	–	ns	
OE Lead Time Referenced to RAS	toes	0	–	0	–	0	–	0	–	ns	
CAS to Data Setup Time	tclZ	0	–	0	–	0	–	0	–	ns	
OE to Data Setup Time	tolZ	0	–	0	–	0	–	0	–	ns	
OE to Data Delay Time	toed	10	–	13	–	15	–	15	–	ns	
Transition Time (Rise and Fall)	tr	3	50	3	50	3	50	3	50	ns	
Refresh Time	trEF	–	64	–	64	–	64	–	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$trad \leq trad(MAX.)$ and $trcd \leq trcd(MAX.)$	$trac(MAX.)$	$trac(MAX.)$
$trad > trad(MAX.)$ and $trcd \leq trcd(MAX.)$	$tAA(MAX.)$	$trad + tAA(MAX.)$
$trcd > trcd(MAX.)$	$tcac(MAX.)$	$trcd + tcac(MAX.)$

$trad(MAX.)$ and $trcd(MAX.)$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time ($trac$, tAA or $tcac$) is to be used for finding out when data will be available. Therefore, the input conditions $trad \geq trad(MAX.)$ and $trcd \geq trcd(MAX.)$ will not cause any operation problems.

2. $tcRP(MIN.)$ requirement is applied to RAS, CAS cycles preceded by any cycle.

Read Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	t _{RAC}	–	50	–	60	–	70	–	80	ns	1
Access Time from $\overline{\text{CAS}}$	t _{CAC}	–	13	–	15	–	18	–	20	ns	1
Access Time from Column Address	t _{AA}	–	25	–	30	–	35	–	40	ns	1
Access Time from $\overline{\text{OE}}$	t _{OEa}	–	13	–	15	–	18	–	20	ns	
Column Address Lead Time Referenced to RAS	t _{RAI}	25	–	30	–	35	–	40	–	ns	
Read Command Setup Time	t _{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	0	–	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to CAS	t _{RCH}	0	–	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OEZ}	0	10	0	13	0	15	0	15	ns	3
Output Buffer Turn-off Delay Time from CAS	t _{OFF}	0	10	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
t _{RAI} ≤ t _{RAI} (MAX.) and t _{RCD} ≤ t _{RCD} (MAX.)	t _{RAC} (MAX.)	t _{RAC} (MAX.)
t _{RAI} > t _{RAI} (MAX.) and t _{RCD} ≤ t _{RCD} (MAX.)	t _{AA} (MAX.)	t _{RAI} + t _{AA} (MAX.)
t _{RCD} > t _{RCD} (MAX.)	t _{CAC} (MAX.)	t _{RCD} + t _{CAC} (MAX.)

t_{RAI} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions t_{RAI} ≥ t_{RAI} (MAX.) and t_{RCD} ≥ t_{RCD} (MAX.) will not cause any operation problems.

2. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
3. t_{OFF} (MAX.) and t_{OEZ} (MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t _{rac} = 50 ns		t _{rac} = 60 ns		t _{rac} = 70 ns		t _{rac} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	8	–	10	–	10	–	15	–	ns	1
$\overline{\text{WE}}$ Pulse Width	t _{WP}	8	–	10	–	10	–	15	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	13	–	15	–	15	–	15	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	13	–	15	–	15	–	15	–	ns	
$\overline{\text{WE}}$ Setup Time	t _{WCS}	0	–	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0	–	0	–	0	–	0	–	ns	
Data-in Setup Time	t _{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in Hold Time	t _{DH}	10	–	10	–	15	–	15	–	ns	3

- Notes**
1. t_{WP} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH} (MIN.) should be met.
 2. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{rac} = 50 ns		t _{rac} = 60 ns		t _{rac} = 70 ns		t _{rac} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t _{RWC}	128	–	153	–	175	–	195	–	ns	
RAS to $\overline{\text{WE}}$ Delay Time	t _{RWD}	70	–	83	–	95	–	105	–	ns	1
CAS to $\overline{\text{WE}}$ Delay Time	t _{CWD}	33	–	38	–	43	–	45	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	45	–	53	–	60	–	65	–	ns	1

- Note**
1. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN.), t_{CWD} ≥ t_{CWD} (MIN.), t_{AWD} ≥ t_{AWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

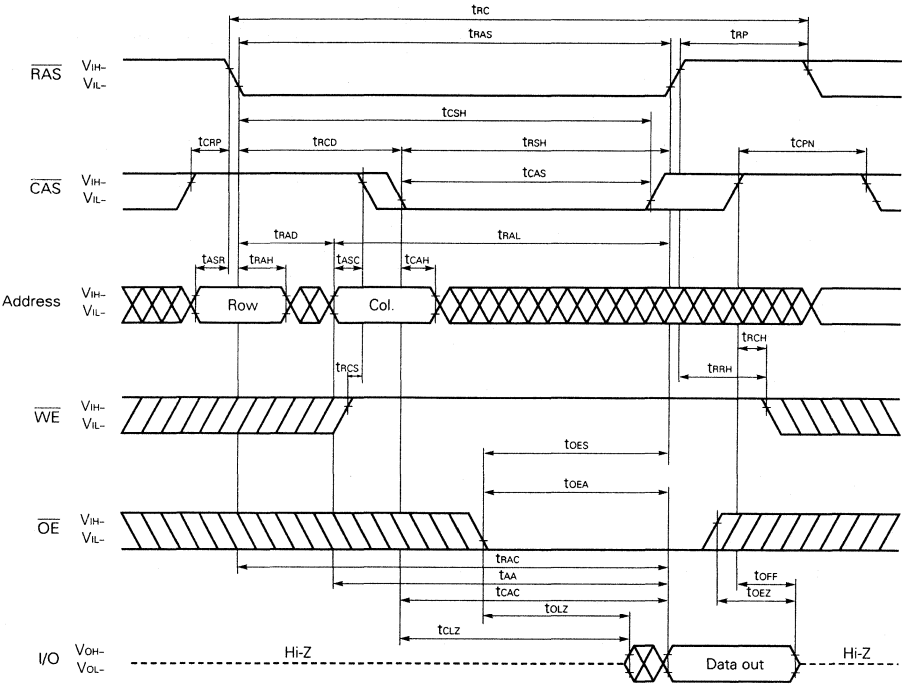
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	35	–	40	–	45	–	50	–	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	–	30	–	35	–	40	–	45	ns	
RAS Pulse Width	t _{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
CAS Precharge Time	t _{CP}	8	–	10	–	10	–	10	–	ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	–	35	–	40	–	45	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	73	–	83	–	90	–	95	–	ns	
CAS Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	50	–	58	–	65	–	70	–	ns	1

Note 1. If $\text{twcs} \geq \text{twcs (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{trwd} \geq \text{trwd (MIN.)}$, $\text{tcwd} \geq \text{tcwd (MIN.)}$, $\text{tawd} \geq \text{tawd (MIN.)}$ and $\text{tcpwd} \geq \text{tcpwd (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

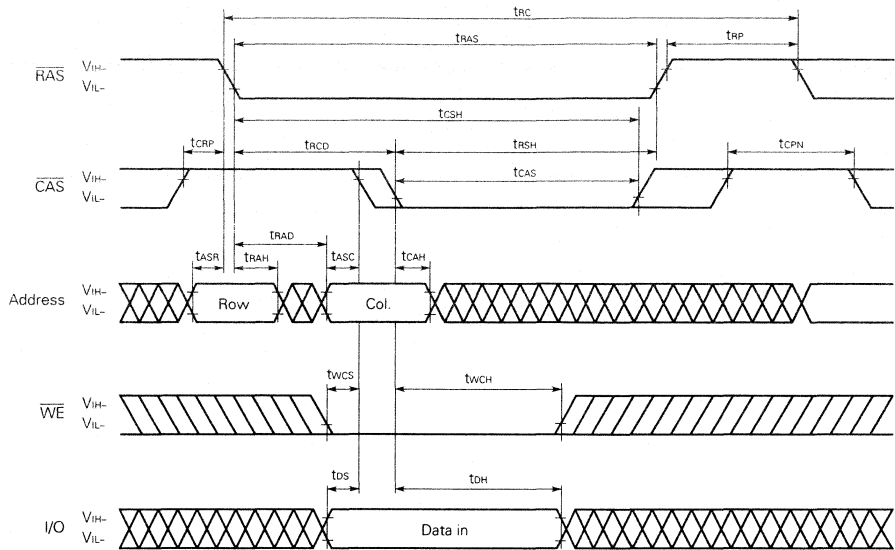
Refresh Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	–	5	–	5	–	5	–	ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10	–	10	–	10	–	10	–	ns	
RAS Precharge CAS Hold Time	t _{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15	–	15	–	15	–	15	–	ns	

Read Cycle

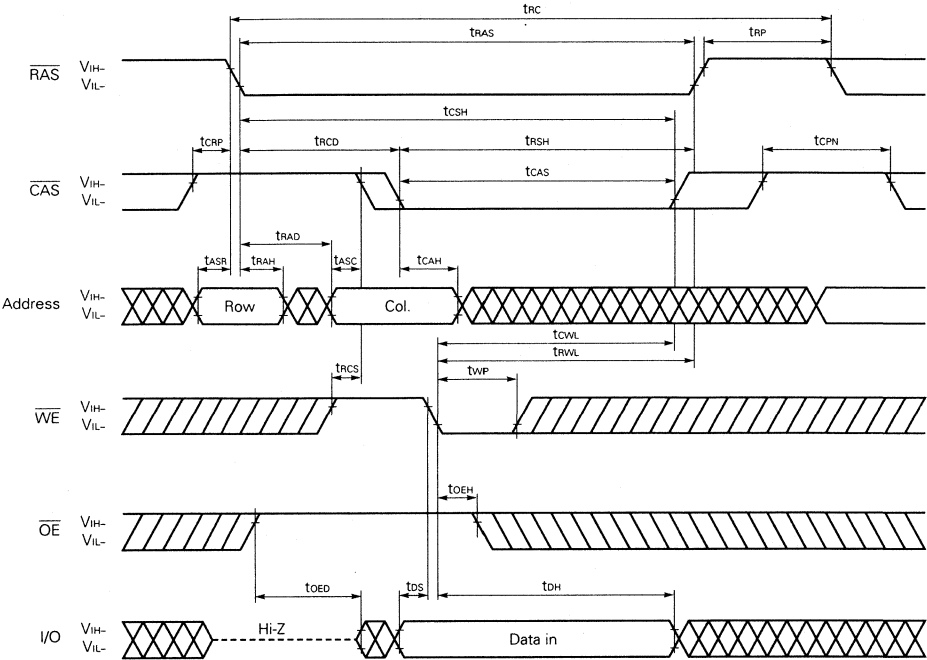


Early Write Cycle

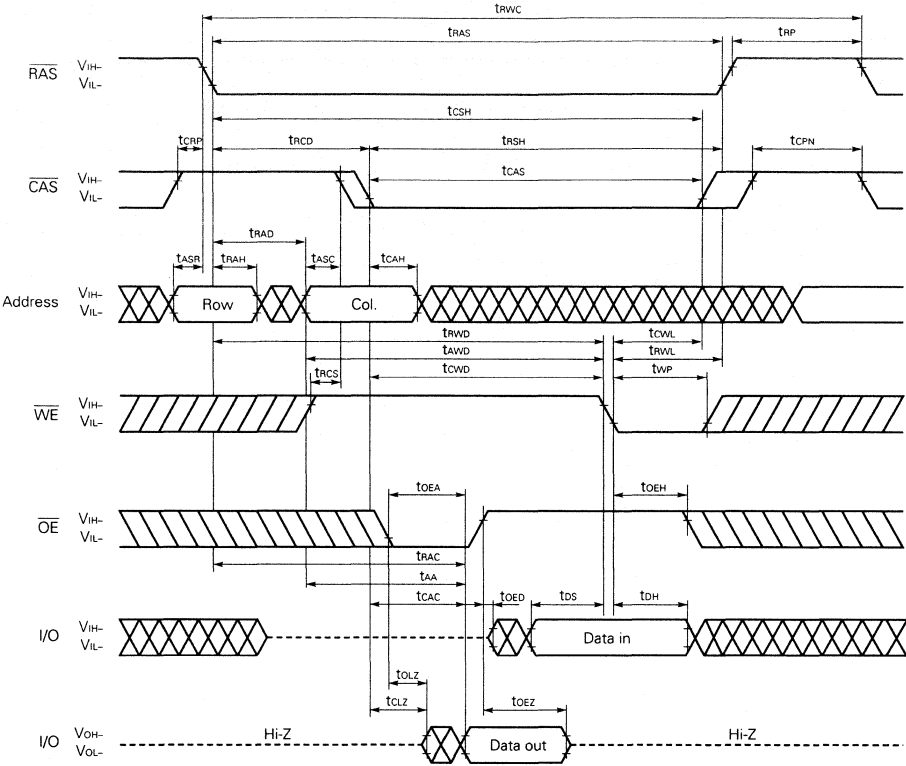


Remark $\overline{\text{OE}}$: Don't care

Late Write Cycle



Read Modify Write Cycle



The timing diagram illustrates the sequence of signals for three memory access cycles: Row-to-Column (Row), Column-to-Column (Col.), and another Column access. The signals shown are:

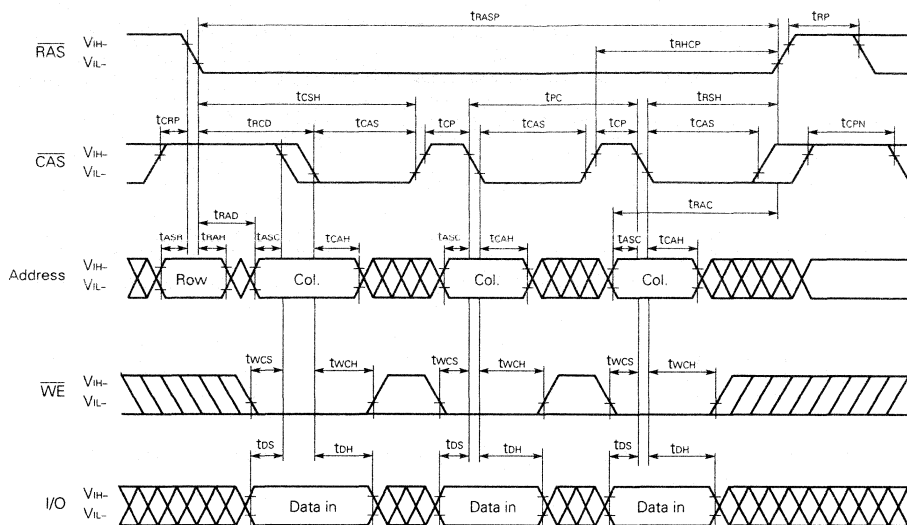
- RAS**: Row Address Strobe, active low.
- CAS**: Column Address Strobe, active low.
- Address**: Data bus carrying row and column addresses.
- WE**: Write Enable, active low.
- OE**: Output Enable, active low.
- I/O**: Data bus showing Hi-Z (high impedance) and Data out states.

Key timing parameters labeled include:

- t_{TRP}**, **t_{TRHCP}**, **t_{TRSH}**: RAS precharge, hold, and setup times.
- t_{CRP}**, **t_{CRD}**, **t_{CRS}**, **t_{CP}**, **t_{CPN}**: CAS precharge, delay, setup, pulse width, and post-pulse times.
- t_{AD}**, **t_{AS}**, **t_{AH}**, **t_{CAH}**: Address delay, setup, hold, and column address hold times.
- t_{WC}**, **t_{WH}**: Write command delay and hold times.
- t_{OE}**, **t_{OLZ}**, **t_{TA}**, **t_{TAA}**, **t_{TOF}**, **t_{TOEZ}**: Output enable delay, output load time, access time, output delay, output disable time, and output enable/disable times.

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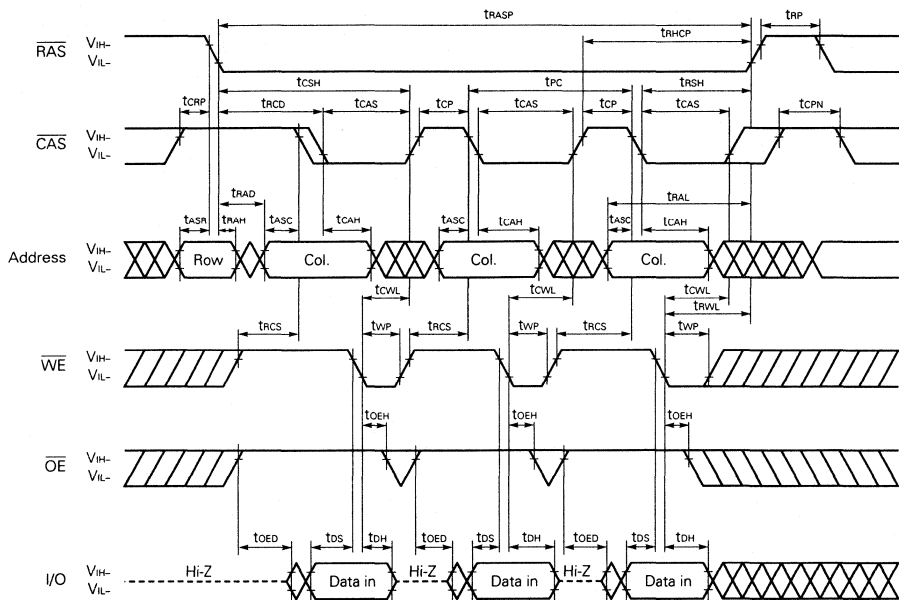
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{\text{OE}}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

The timing diagram illustrates the relationship between the RAS, CAS, Address, WE, OE, and I/O signals for the 64K1602C device. The signals are shown as waveforms with various timing parameters labeled. The RAS signal is active low, and the CAS signal is active low. The Address signal is shown with Row and Column decodes. The WE signal is active low. The OE signal is active low. The I/O signal is shown with output (out) and input (in) states. The timing parameters include tRASP, tCRP, tRCD, tCAS, tCP, tCPW, tCAH, tTAS, tTAD, tTAS, tTCAH, tTAL, tRCS, tRWD, tAWD, tCWD, tTWP, tTCS, tTAC, tTAA, tTOEH, tTAC, tTOEA, tTCLZ, tTOED, tTOEZ, tTOLZ, tTDS, tTDH, tTOS, tTDS, tTDH, tTOS.

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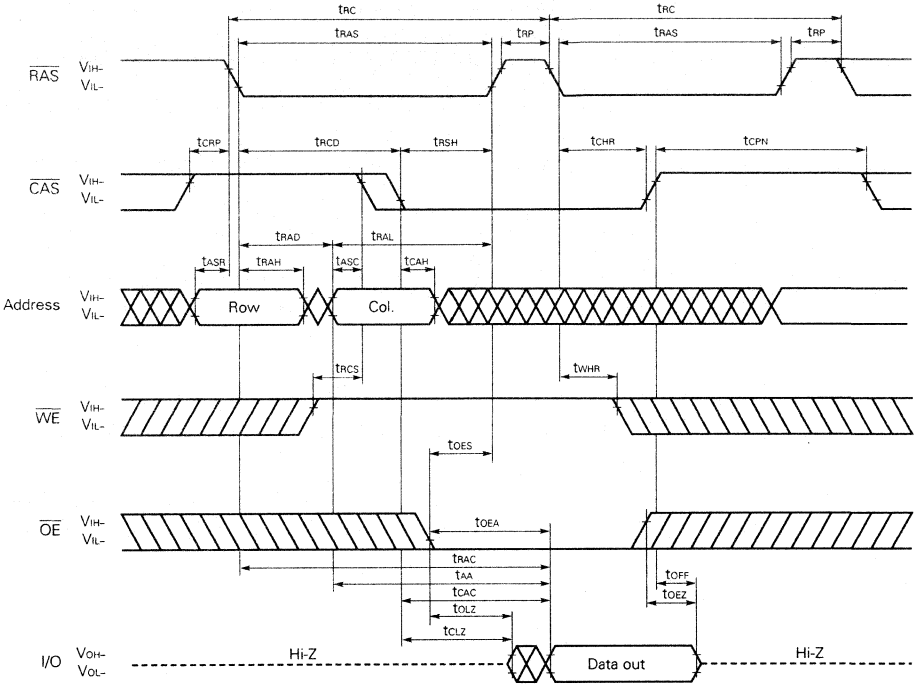
The timing diagram illustrates the relationship between the Read/Write Enable (RAS, CAS, WE) signals and the data bus. The signals are shown as digital waveforms, and the timing parameters are indicated by arrows and labels:

- RAS:** Read/Write Enable signal. Timing parameters include t_{AC} (Access time), t_{RAS} (Read/Write Enable pulse width), t_{AP} (Read/Write Enable setup time), t_{CRP} (Read/Write Enable recovery time), and t_{CPN} (Read/Write Enable setup time).
- CAS:** Column Address Strobe signal. Timing parameters include t_{CSR} (Column Address Strobe setup time), t_{CHR} (Column Address Strobe hold time), and t_{CPC} (Column Address Strobe pulse width).
- WE:** Write Enable signal. Timing parameters include t_{WSR} (Write Enable setup time) and t_{VHR} (Write Enable hold time).

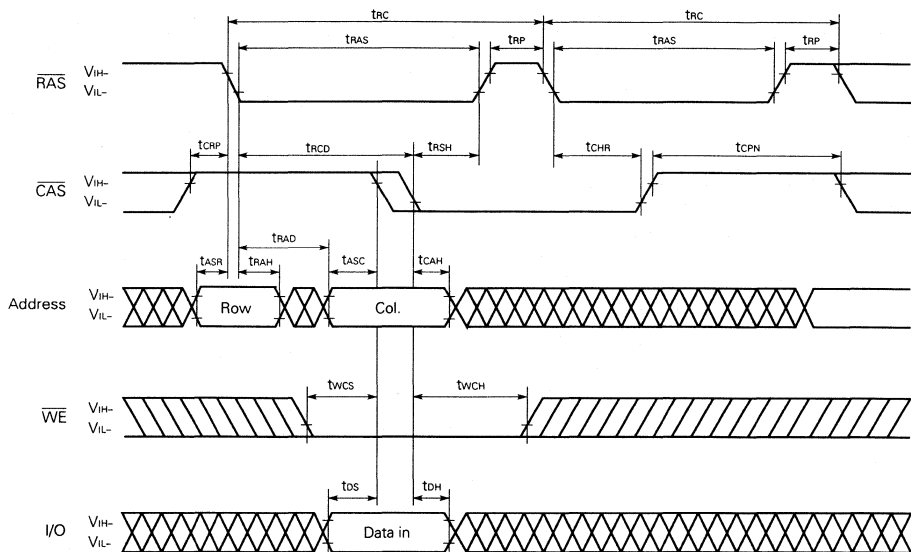
The diagram illustrates the timing relationships for RAS, CAS, and Address signals. The RAS signal is shown as a series of pulses, with parameters t_{RAC} (RAS access time), t_{RAS} (RAS to data delay), and t_{RP} (RAS pulse width) indicated. The CAS signal is shown as a series of pulses, with parameters t_{CRP} (CAS to data delay), t_{RPC} (CAS to data delay), and t_{CPN} (CAS to data delay) indicated. The Address signal is shown as a series of pulses, with parameters t_{ASR} (Address to data delay) and t_{RAH} (Address to data delay) indicated. The diagram also shows the relationship between RAS and CAS signals, with t_{RPC} and t_{CPN} indicating the delay from RAS to CAS.

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Hidden Refresh Cycle (Read)

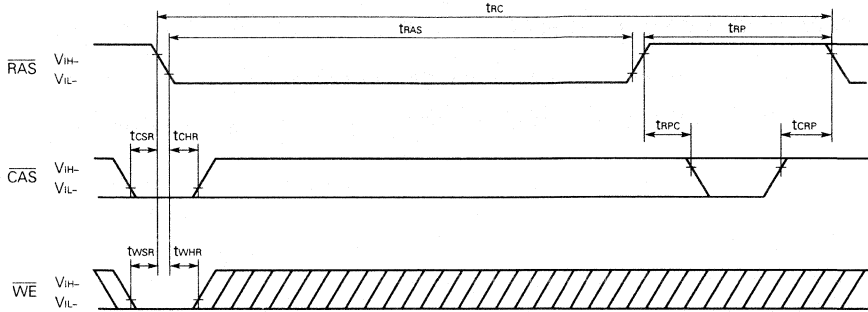


Hidden Refresh Cycle (Write)



Remark $\overline{\text{OE}}$: Don't care

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)



Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 8$ -bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 8 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)

Output = "0": Abnormal write

(3) Refresh

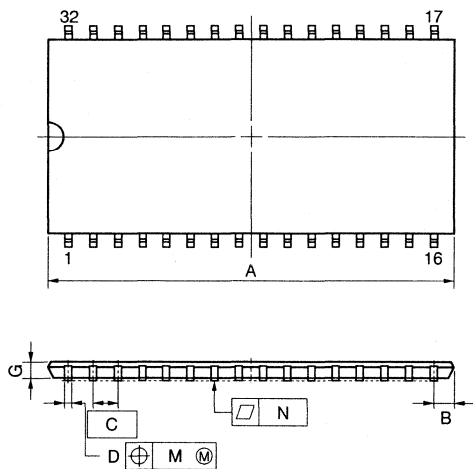
Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

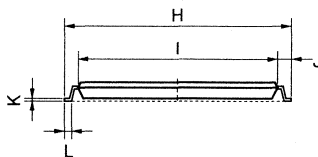
The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

Package Drawings

32PIN PLASTIC TSOP(II) (400 mil)



detail of lead end



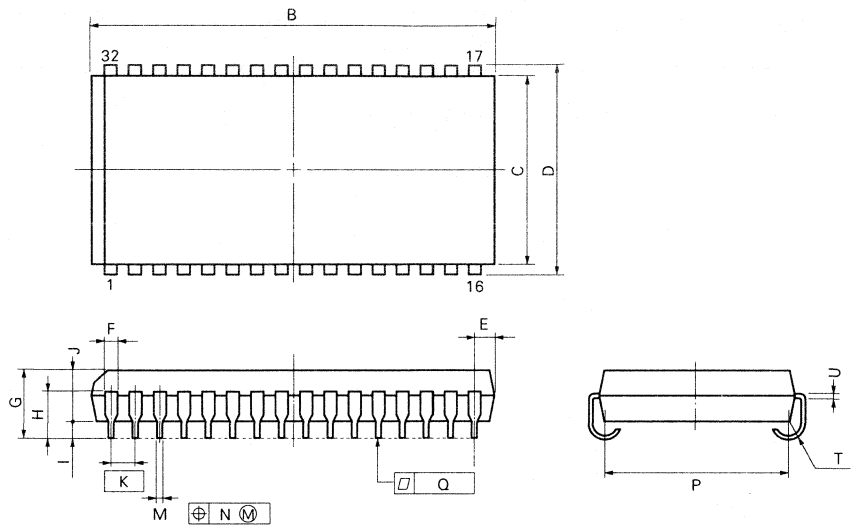
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.42 ^{+0.08} _{-0.07}	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S32G5-50-7JD2

32 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P32LE-400A

ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	0.040 ^{+0.004} _{-0.005}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

MOS INTEGRATED CIRCUIT

μ PD4264800, 4265800

64 M-BIT DYNAMIC RAM

8 M-WORD BY 8-BIT, FAST PAGE MODE

Description

The μ PD4264800, 4265800 are 8,388,608 words by 8 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

These are packaged in 32-pin plastic TSOP(II) and 32-pin plastic SOJ.

Features

- 8,388,608 words by 8 bits organization
- Single +3.3 V $\pm$ 0.3 V power supply
- Fast access and cycle time

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μ PD4264800-A50	378 mW	1.80 mW (CMOS level input)	50 ns	90 ns	35 ns
μ PD4265800-A50	486 mW				
μ PD4264800-A60	342 mW		60 ns	110 ns	40 ns
μ PD4265800-A60	414 mW				
μ PD4264800-A70	306 mW		70 ns	130 ns	45 ns
μ PD4265800-A70	378 mW				
μ PD4264800-A80	270 mW		80 ns	150 ns	50 ns
μ PD4265800-A80	342 mW				

- CAS before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh

Part number	Row address	Column address	Refresh	Refresh cycle
μ PD4264800	A0 - A12	A0 - A9	$\overline{\text{RAS}}$ only refresh, Normal read/write	8,192 cycles/64 ms
			CAS before $\overline{\text{RAS}}$ refresh, Hidden refresh	4,096 cycles/64 ms
μ PD4265800	A0 - A11	A0 - A10	$\overline{\text{RAS}}$ only refresh, Normal read/write, CAS before $\overline{\text{RAS}}$ refresh, Hidden refresh	4,096 cycles/64 ms

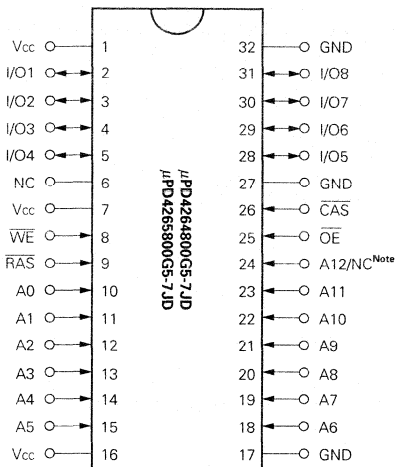
The information in this document is subject to change without notice.

Ordering Information

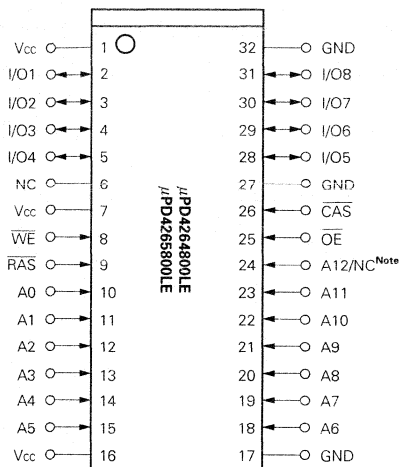
Part number	Access time (MAX.)	Package	Refresh
μPD4264800G5-A50-7JD	50 ns	32-pin Plastic TSOP (II) (400 mil)	CAS before RAS refresh RAS only refresh Hidden refresh
μPD4264800G5-A60-7JD	60 ns		
μPD4264800G5-A70-7JD	70 ns		
μPD4264800G5-A80-7JD	80 ns		
μPD4264800LE-A50	50 ns	32-pin Plastic SOJ (400 mil)	
μPD4264800LE-A60	60 ns		
μPD4264800LE-A70	70 ns		
μPD4264800LE-A80	80 ns		
μPD4265800G5-A50-7JD	50 ns	32-pin Plastic TSOP (II) (400 mil)	
μPD4265800G5-A60-7JD	60 ns		
μPD4265800G5-A70-7JD	70 ns		
μPD4265800G5-A80-7JD	80 ns		
μPD4265800LE-A50	50 ns	32-pin Plastic SOJ (400 mil)	
μPD4265800LE-A60	60 ns		
μPD4265800LE-A70	70 ns		
μPD4265800LE-A80	80 ns		

Pin Configurations (Marking Side)

32-pin Plastic TSOP (II) (400 mil)



32-pin Plastic SOJ (400 mil)



Note A12 ... μPD4264800

NC ... μPD4265800

- A0 to A12 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Input/Output Pin Functions

The μ PD4264800, 4265800 have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, Address^{Note} and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)	Input	$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A _x ^{Note} (Address inputs)	Input	Address bus. Input total 23-bit of address signal, upper bits and lower bits ^{Note} in sequence (address multiplex method). Therefore, one word is selected from 8,388,608-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μ PD4264800	A0-A12	13	10
μ PD4265800	A0-A11	12	11

Electrical Specifications (Preliminary)

- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

[μ PD4264800]

Parameter	Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling t _{RC} = t _{RC} (MIN.) I _O = 0 mA	t _{RAC} = 50 ns		105	mA	1, 2, 3
			t _{RAC} = 60 ns		95		
			t _{RAC} = 70 ns		85		
			t _{RAC} = 80 ns		75		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH} \text{ (MIN.)}, I_O = 0 \text{ mA}$			1.0	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}, I_O = 0 \text{ mA}$			0.5		
RAS only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{IH} \text{ (MIN.)}$ t _{RC} = t _{RC} (MIN.), I _O = 0 mA	t _{RAC} = 50 ns		105	mA	1, 2, 3, 4
			t _{RAC} = 60 ns		95		
			t _{RAC} = 70 ns		85		
			t _{RAC} = 80 ns		75		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{IL} \text{ (MAX.)}, \overline{\text{CAS}}$ Cycling t _{PC} = t _{PC} (MIN.), I _O = 0 mA	t _{RAC} = 50 ns		85	mA	1, 2, 5
			t _{RAC} = 60 ns		75		
			t _{RAC} = 70 ns		65		
			t _{RAC} = 80 ns		55		
CAS before RAS refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling t _{RC} = t _{RC} (MIN.) I _O = 0 mA	t _{RAC} = 50 ns		135	mA	1, 2
			t _{RAC} = 60 ns		115		
			t _{RAC} = 70 ns		105		
			t _{RAC} = 80 ns		95		
Input leakage current	I _{I (L)}	V _I = 0 to 3.6 V All other pins not under test = 0 V		-5	+5	μ A	
Output leakage current	I _{O (L)}	V _O = 0 to 3.6 V Output is disabled (Hi-Z)		-5	+5	μ A	
High level output voltage	V _{OH}	I _O = -2.0 mA		2.4		V	
Low level output voltage	V _{OL}	I _O = +2.0 mA			0.4	V	

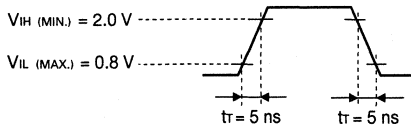
[μ PD4265800]

Parameter	Symbol	Test Condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	135	mA	1, 2, 3
			$t_{\text{RAC}} = 60 \text{ ns}$	115		
			$t_{\text{RAC}} = 70 \text{ ns}$	105		
			$t_{\text{RAC}} = 80 \text{ ns}$	95		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), I_o = 0 \text{ mA}$		1.0	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_o = 0 \text{ mA}$		0.5		
RAS only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.}), I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	135	mA	1, 2, 3, 4
			$t_{\text{RAC}} = 60 \text{ ns}$	115		
			$t_{\text{RAC}} = 70 \text{ ns}$	105		
			$t_{\text{RAC}} = 80 \text{ ns}$	95		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.}), I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	85	mA	1, 2, 5
			$t_{\text{RAC}} = 60 \text{ ns}$	75		
			$t_{\text{RAC}} = 70 \text{ ns}$	65		
			$t_{\text{RAC}} = 80 \text{ ns}$	55		
CAS before RAS refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	135	mA	1, 2
			$t_{\text{RAC}} = 60 \text{ ns}$	115		
			$t_{\text{RAC}} = 70 \text{ ns}$	105		
			$t_{\text{RAC}} = 80 \text{ ns}$	95		
Input leakage current	I _I (L)	$V_i = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V	-5	+5	μA	
Output leakage current	I _O (L)	$V_o = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)	-5	+5	μA	
High level output voltage	V _{OH}	$I_o = -2.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +2.0 \text{ mA}$		0.4	V	

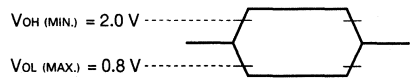
- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)**AC Characteristics Test Conditions**

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{RC}	90	—	110	—	130	—	150	—	ns	
RAS Precharge Time	t _{RP}	30	—	40	—	50	—	60	—	ns	
CAS Precharge Time	t _{CPN}	8	—	10	—	10	—	10	—	ns	
RAS Pulse Width	t _{RA}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
CAS Pulse Width	t _{CA}	13	10,000	15	10,000	18	10,000	20	10,000	ns	
RAS Hold Time	t _{RSH}	13	—	15	—	18	—	20	—	ns	
CAS Hold Time	t _{CSH}	50	—	60	—	70	—	80	—	ns	
RAS to CAS Delay Time	t _{RCD}	18	32	20	45	20	50	25	60	ns	1
RAS to Column Address Delay Time	t _{RAD}	13	25	15	30	15	35	17	40	ns	1
CAS to RAS Precharge Time	t _{CRP}	5	—	5	—	5	—	5	—	ns	2
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	8	—	10	—	10	—	12	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	13	—	15	—	15	—	15	—	ns	
OE Lead Time Referenced to RAS	t _{OES}	0	—	0	—	0	—	0	—	ns	
CAS to Data Setup Time	t _{CLZ}	0	—	0	—	0	—	0	—	ns	
OE to Data Setup Time	t _{OLZ}	0	—	0	—	0	—	0	—	ns	
OE to Data Delay Time	t _{OED}	10	—	13	—	15	—	15	—	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
Refresh Time	t _{REF}	—	64	—	64	—	64	—	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
t _{RAD} ≤ t _{RAD} (MAX.) and t _{RCD} ≤ t _{RCD} (MAX.)	t _{RAC} (MAX.)	t _{RAC} (MAX.)
t _{RAD} > t _{RAD} (MAX.) and t _{RCD} ≤ t _{RCD} (MAX.)	t _{AA} (MAX.)	t _{RAD} + t _{AA} (MAX.)
t _{RCD} > t _{RCD} (MAX.)	t _{CAC} (MAX.)	t _{RCD} + t _{CAC} (MAX.)

t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when data will be available. Therefore, the input conditions t_{RAD} ≥ t_{RAD} (MAX.) and t_{RCD} ≥ t_{RCD} (MAX.) will not cause any operation problems.

2. t_{CRP} (MIN.) requirement is applied to RAS, CAS cycles preceded by any cycle.

Read Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	t _{RAC}	–	50	–	60	–	70	–	80	ns	1
Access Time from $\overline{\text{CAS}}$	t _{CAC}	–	13	–	15	–	18	–	20	ns	1
Access Time from Column Address	t _{AA}	–	25	–	30	–	35	–	40	ns	1
Access Time from $\overline{\text{OE}}$	t _{OE A}	–	13	–	15	–	18	–	20	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RA L}	25	–	30	–	35	–	40	–	ns	
Read Command Setup Time	t _{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0	–	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0	–	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OE Z}	0	10	0	13	0	15	0	15	ns	3
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	10	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
t _{RA D} ≤ t _{RA D} (MAX.) and t _{RC D} ≤ t _{RC D} (MAX.)	t _{RAC} (MAX.)	t _{RAC} (MAX.)
t _{RA D} > t _{RA D} (MAX.) and t _{RC D} ≤ t _{RC D} (MAX.)	t _{AA} (MAX.)	t _{RA D} + t _{AA} (MAX.)
t _{RC D} > t _{RC D} (MAX.)	t _{CAC} (MAX.)	t _{RC D} + t _{CAC} (MAX.)

t_{RA D} (MAX.) and t_{RC D} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions t_{RA D} ≥ t_{RA D} (MAX.) and t_{RC D} ≥ t_{RC D} (MAX.) will not cause any operation problems.

2. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
3. t_{OFF} (MAX.) and t_{OE Z} (MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	8	–	10	–	10	–	15	–	ns	1
$\overline{\text{WE}}$ Pulse Width	t _{WP}	8	–	10	–	10	–	15	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	13	–	15	–	15	–	15	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	13	–	15	–	15	–	15	–	ns	
$\overline{\text{WE}}$ Setup Time	t _{WCS}	0	–	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0	–	0	–	0	–	0	–	ns	
Data-in Setup Time	t _{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in Hold Time	t _{DH}	10	–	10	–	15	–	15	–	ns	3

- Notes**
1. t_{WP} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH} (MIN.) should be met.
 2. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t _{RWC}	128	–	153	–	175	–	195	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	70	–	83	–	95	–	105	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	33	–	38	–	43	–	45	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	45	–	53	–	60	–	65	–	ns	1

- Note**
1. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN.), t_{CWD} ≥ t_{CWD} (MIN.), t_{AWD} ≥ t_{AWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

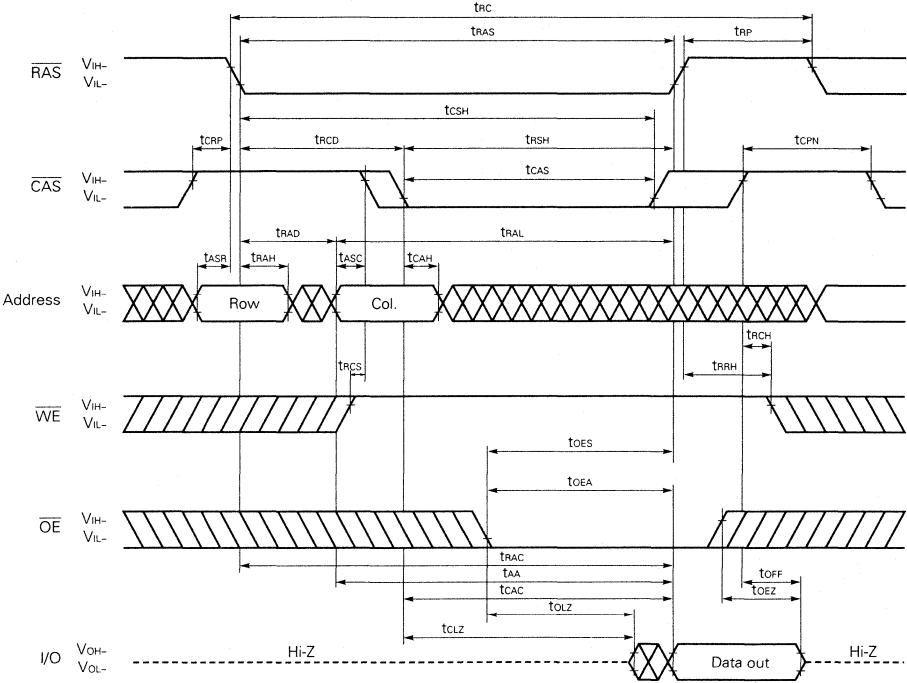
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	35	–	40	–	45	–	50	–	ns	
Access Time from CAS Precharge	t _{ACP}	–	30	–	35	–	40	–	45	ns	
RAS Pulse Width	t _{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
CAS Precharge Time	t _{CP}	8	–	10	–	10	–	10	–	ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	30	–	35	–	40	–	45	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	73	–	83	–	90	–	95	–	ns	
CAS Precharge to WE Delay Time	t _{CPWD}	50	–	58	–	65	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWd} \geq t_{RWd}(\text{MIN.})$, $t_{CWD} \geq t_{CWD}(\text{MIN.})$, $t_{AWd} \geq t_{AWd}(\text{MIN.})$ and $t_{CPWD} \geq t_{CPWD}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

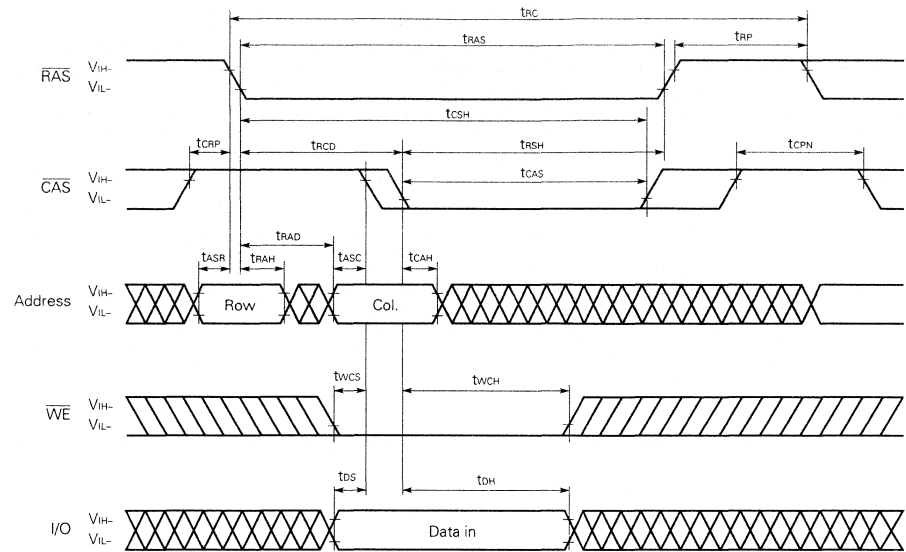
Refresh Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	–	5	–	5	–	5	–	ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10	–	10	–	10	–	10	–	ns	
RAS Precharge CAS Hold Time	t _{RPC}	5	–	5	–	5	–	5	–	ns	
WE Setup Time	t _{WSR}	10	–	10	–	10	–	10	–	ns	
WE Hold Time	t _{WHR}	15	–	15	–	15	–	15	–	ns	

Read Cycle

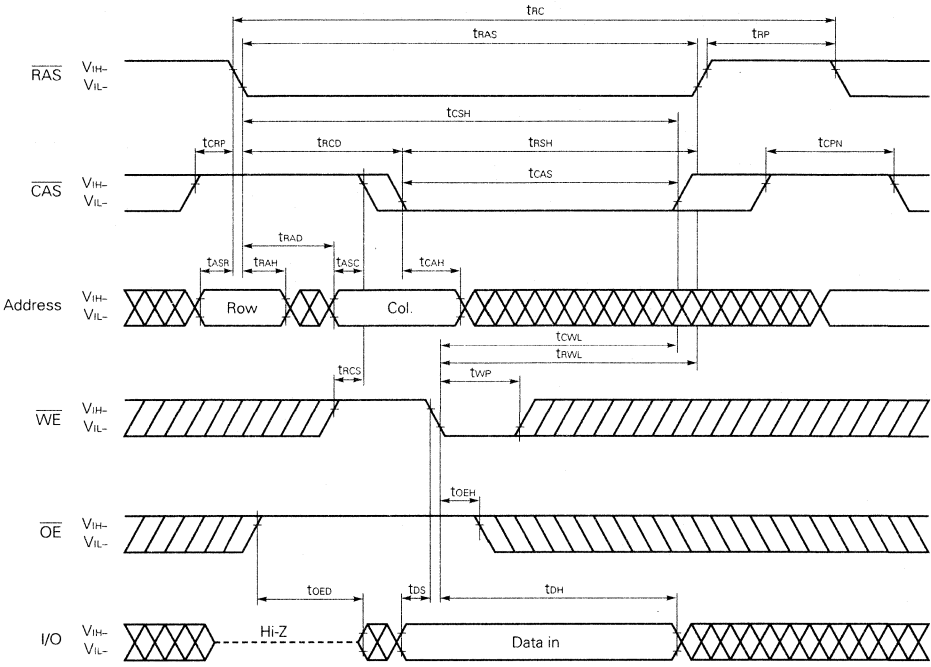


Early Write Cycle

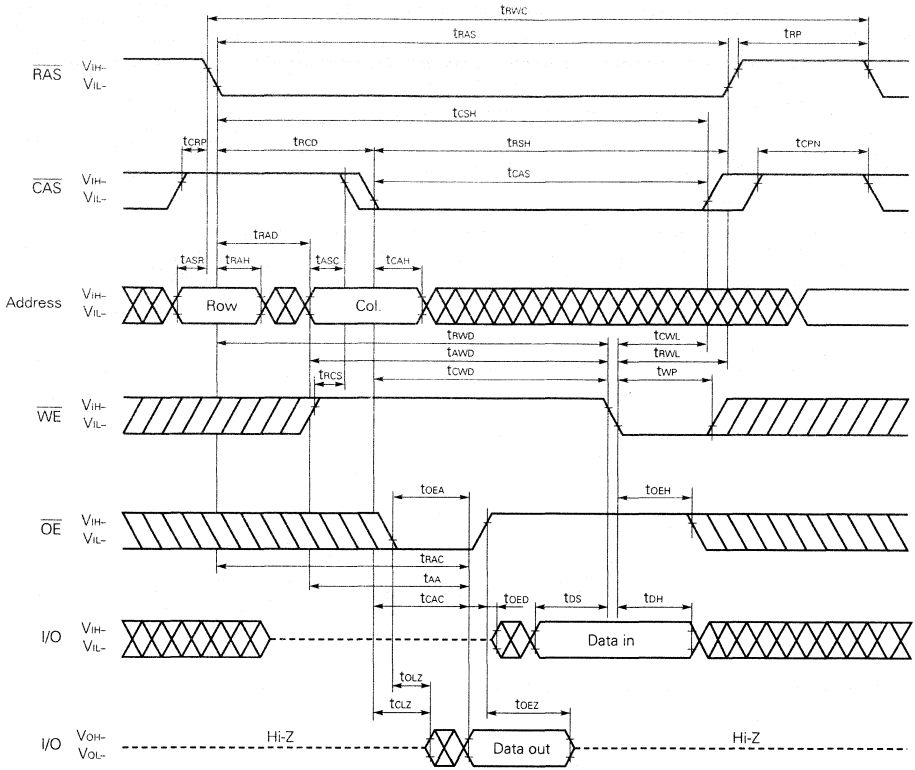


Remark $\overline{OE}$: Don't care

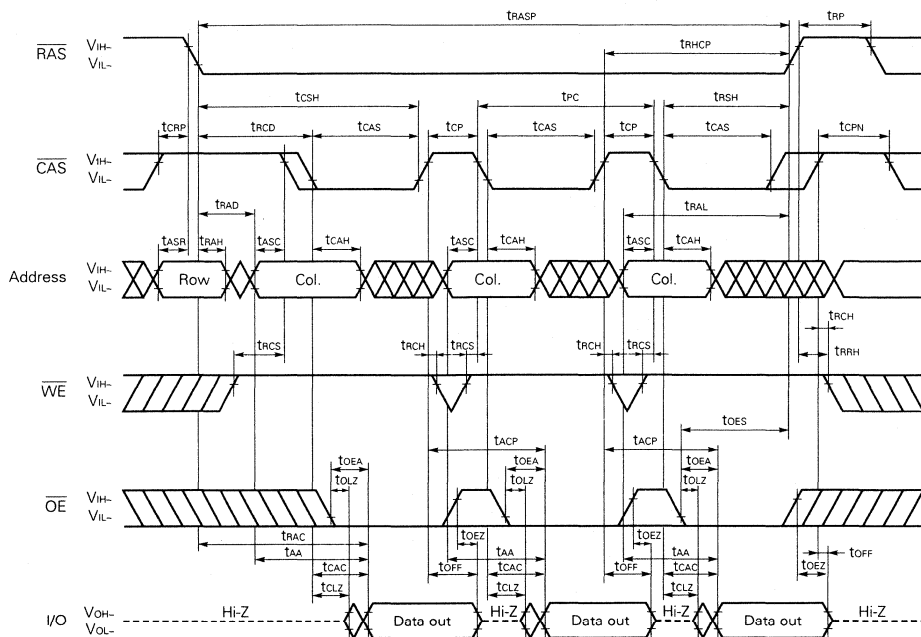
Late Write Cycle



Read Modify Write Cycle



Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

The diagram illustrates the timing relationships for a 256Kbit DRAM (64K x 16). It shows the signals RAS, CAS, Address, WE, and I/O, along with their respective timing parameters:

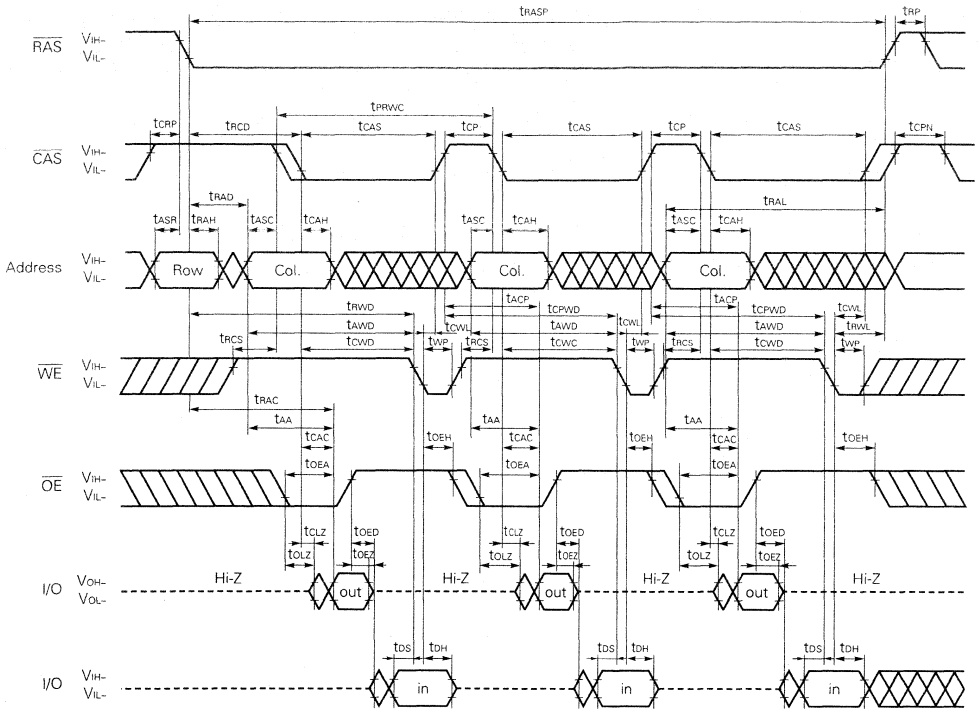
- RAS:** V_{IH} , V_{IL} . Timing parameters: t_{RASP} (RAS pulse width), t_{RCP} (RAS to CAS delay), t_{RSH} (RAS to WE delay), t_{RTP} (RAS to WE delay).
- CAS:** V_{IH} , V_{IL} . Timing parameters: t_{RSH} (RAS to WE delay), t_{RCP} (RAS to CAS delay), t_{RSH} (RAS to WE delay), t_{RTP} (RAS to WE delay).
- Address:** V_{IH} , V_{IL} . Timing parameters: t_{RCP} (RAS to CAS delay), t_{RSH} (RAS to WE delay), t_{RTP} (RAS to WE delay).
- WE:** V_{IH} , V_{IL} . Timing parameters: t_{RCP} (RAS to CAS delay), t_{RSH} (RAS to WE delay), t_{RTP} (RAS to WE delay).
- I/O:** V_{IH} , V_{IL} . Timing parameters: t_{RCP} (RAS to CAS delay), t_{RSH} (RAS to WE delay), t_{RTP} (RAS to WE delay).

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

[illegible]

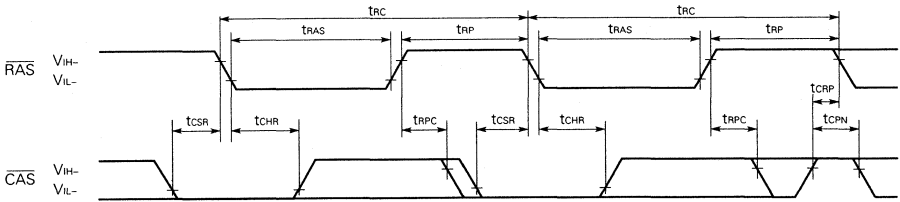
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Read Modify Write Cycle



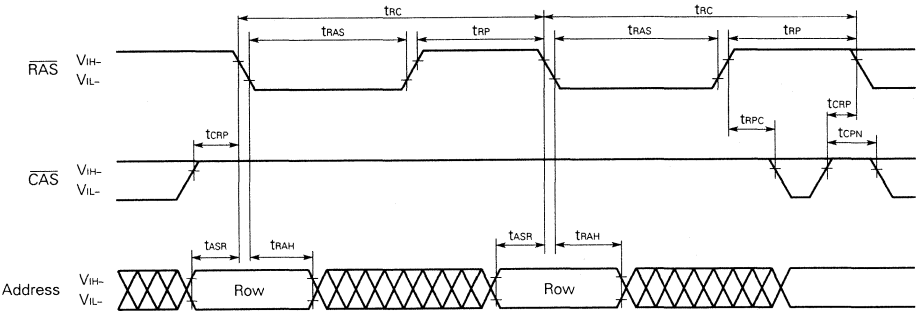
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

CAS Before RAS Refresh Cycle



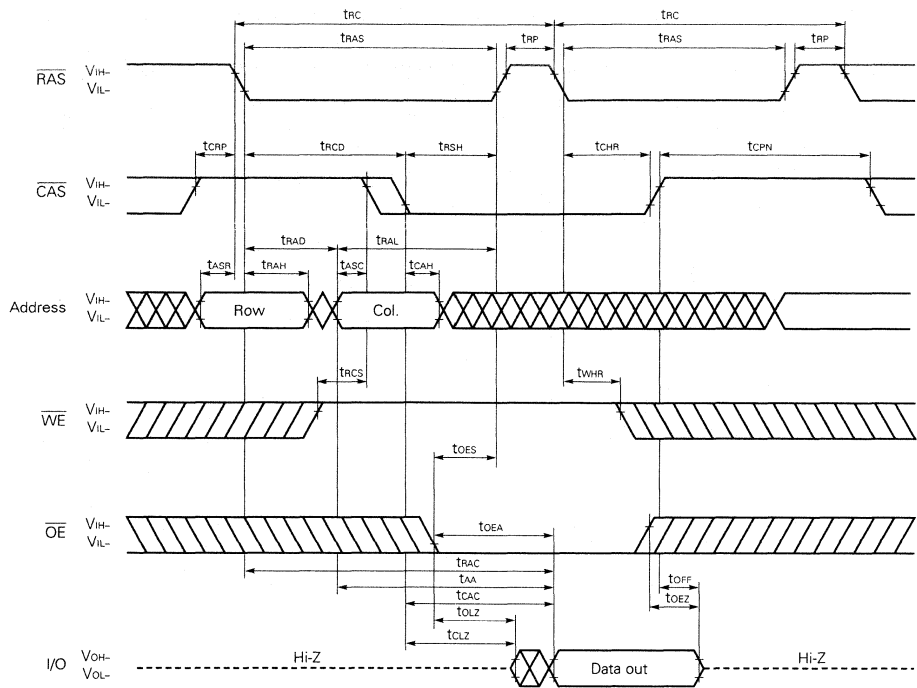
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

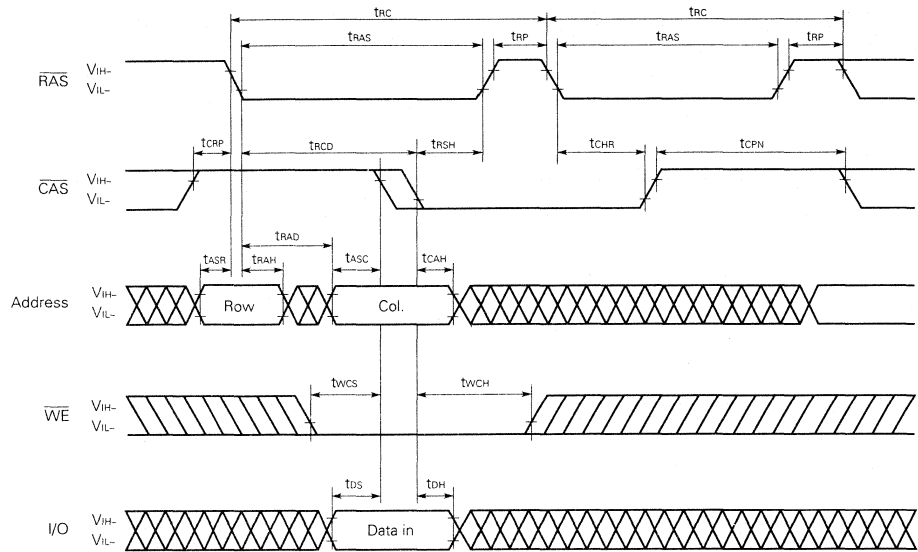


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

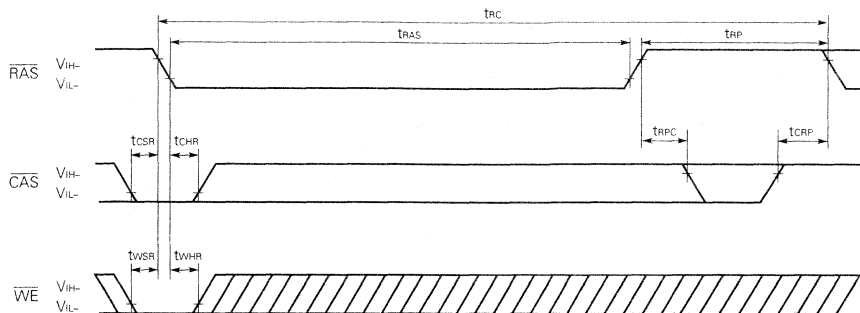


Hidden Refresh Cycle (Write)



Remark $\overline{\text{OE}}$: Don't care

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)



Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 32/64$ ^{Note 1} bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to $4/8$ ^{Note 2} bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)

Output = "0": Abnormal write

(3) Refresh

Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle's internal counter.

(4) Mode Cancellation

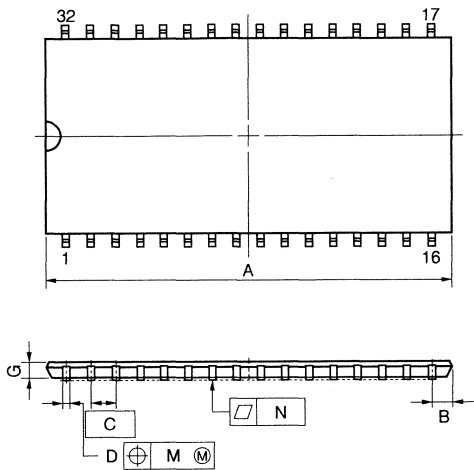
The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

Notes 1. $\times 32$: μ PD4264800 $\times 64$: μ PD4265800

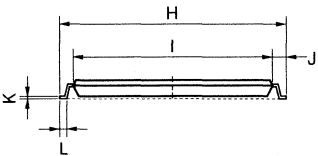
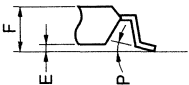
2. 4 : μ PD4264800 8 : μ PD4265800

Package Drawings

32PIN PLASTIC TSOP(II) (400 mil)



detail of lead end

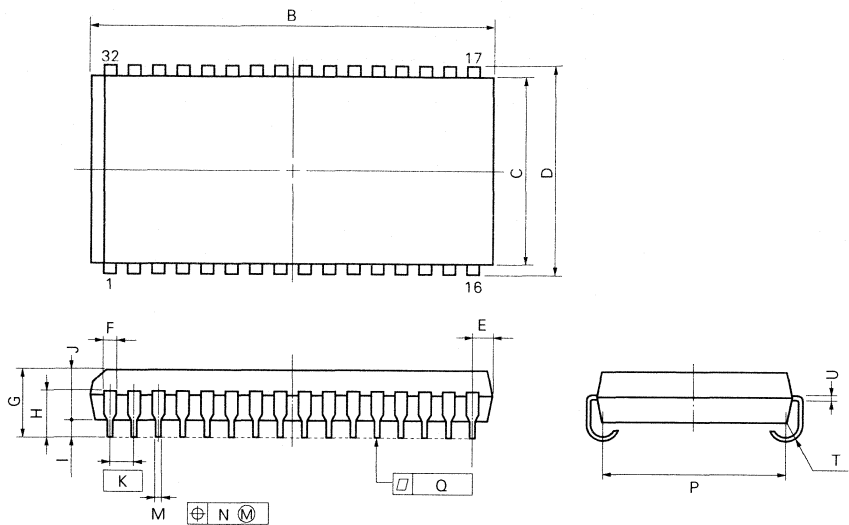


NOTE
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.42 ^{+0.08} _{-0.07}	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S32G5-50-7JD2

32 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P32LE-400A

ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	0.040 ^{+0.004} _{-0.005}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	H 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}



16M Dynamic RAM [5.0V $\pm$ 10%]

MOS INTEGRATED CIRCUIT

μ PD42S16100, 4216100, 42S17100, 4217100

16 M-BIT DYNAMIC RAM

16 M-WORD BY 1-BIT, FAST PAGE MODE

Description

The μ PD42S16100, 4216100, 42S17100, 4217100 are 16 777 216 words by 1 bit dynamic CMOS RAMs. These differ in refresh cycle and the μ PD42S16100, 42S17100 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh. These are packed in 26-pin Plastic TSOP (II) and 26-pin Plastic SOJ.



Features

- 16 777 216 words by 1 bit organization
- Single +5.0 V $\pm$ 10 % power supply
- Fast page mode
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S16100-50, 4216100-50	550 mW	50 ns	90 ns	35 ns
μ PD42S17100-50, 4217100-50	660 mW			
μ PD42S16100-60, 4216100-60	495 mW	60 ns	110 ns	40 ns
μ PD42S17100-60, 4217100-60	605 mW			
μ PD42S16100-70, 4216100-70	440 mW	70 ns	130 ns	45 ns
μ PD42S17100-70, 4217100-70	550 mW			
μ PD42S16100-80, 4216100-80	385 mW	80 ns	150 ns	50 ns
μ PD42S17100-80, 4217100-80	495 mW			

- The μ PD42S16100, 42S17100 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S16100	4 096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μ PD42S17100	2 048 cycles/128 ms		
μ PD4216100	4 096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)
μ PD4217100	2 048 cycles/32 ms		

The information in this document is subject to change without notice.

The mark ★ shows revised points.



Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD42S16100G3-50-7JD	50 ns	26-pin Plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before RAS refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S17100G3-50-7JD			
μPD42S16100G3-60-7JD	60 ns		
μPD42S17100G3-60-7JD			
μPD42S16100G3-70-7JD	70 ns		
μPD42S17100G3-70-7JD			
μPD42S16100G3-80-7JD	80 ns		
μPD42S17100G3-80-7JD			
μPD42S16100LA-50	50 ns	26-pin Plastic SOJ (300 mil)	
μPD42S17100LA-50			
μPD42S16100LA-60	60 ns		
μPD42S17100LA-60			
μPD42S16100LA-70	70 ns		
μPD42S17100LA-70			
μPD42S16100LA-80	80 ns		
μPD42S17100LA-80			
μPD4216100G3-50-7JD	50 ns	26-pin Plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD4217100G3-50-7JD			
μPD4216100G3-60-7JD	60 ns		
μPD4217100G3-60-7JD			
μPD4216100G3-70-7JD	70 ns		
μPD4217100G3-70-7JD			
μPD4216100G3-80-7JD	80 ns		
μPD4217100G3-80-7JD			
μPD4216100LA-50	50 ns	26-pin Plastic SOJ (300 mil)	
μPD4217100LA-50			
μPD4216100LA-60	60 ns		
μPD4217100LA-60			
μPD4216100LA-70	70 ns		
μPD4217100LA-70			
μPD4216100LA-80	80 ns		
μPD4217100LA-80			

Quality Grade

Standard

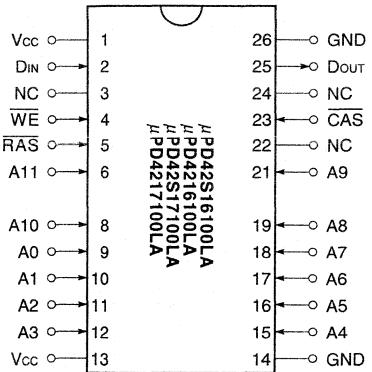
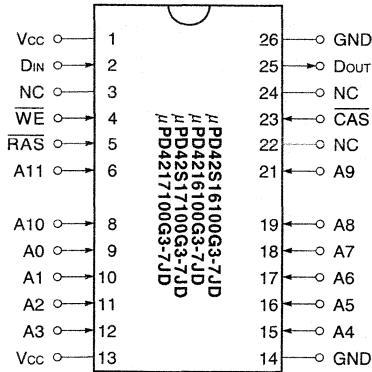
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking Side)



26-pin Plastic TSOP (II) (300 mil)

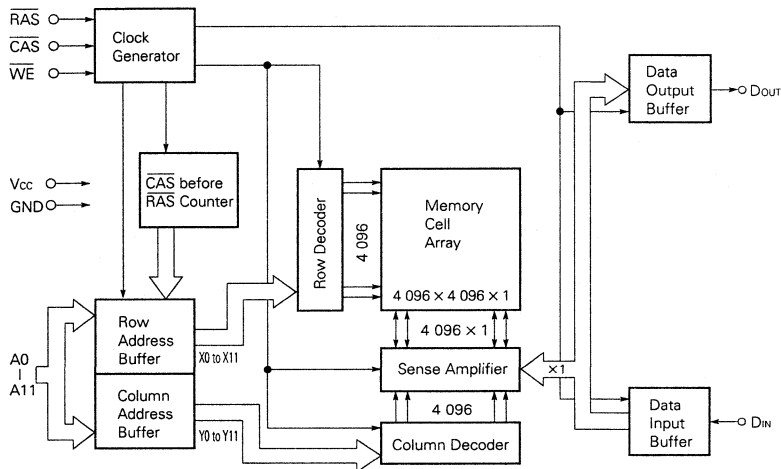
26-pin Plastic SOJ (300 mil)



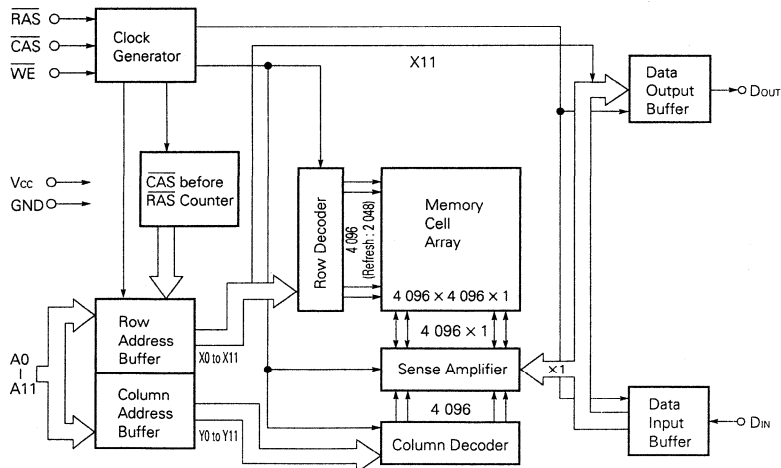
- A0 to A11 : Address Inputs
- DIN : Data Input
- DOUT : Data Output
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram

[μ PD42S16100, 4216100]



[μ PD42S17100, 4217100]



Input/Output Pin Functions

The μPD42S16100, 4216100, 42S17100, 4217100 have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, A0 to A11, D_{IN} and output pin D_{OUT} .

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)		Address bus. Input total 24-bit of address signal, upper 12-bit and lower 12-bit in sequence (address multiplex method). Therefore, one word is selected from 16 777 216-word by 1-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
D_{IN} (Data input)		Data bus. D_{IN} is used to input data.
D_{OUT} (Data output)	Output	Data bus. D_{OUT} is used to output data.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C



Capacitance ($T_a = +25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A11, $\overline{\text{DIN}}$			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$			7	pF
Data Output capacitance	C_O	$\overline{\text{DOUT}}$			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[μ PD42S16100, 4216100]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		100	mA	1, 2, 3
				$t_{\text{RAC}} = 60 \text{ ns}$		90		
				$t_{\text{RAC}} = 70 \text{ ns}$		80		
				$t_{\text{RAC}} = 80 \text{ ns}$		70		
Standby current	$\mu\text{PD42S16100}$	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$I_{\text{O}} = 0 \text{ mA}$		2	mA	
	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$		$I_{\text{O}} = 0 \text{ mA}$		0.25			
	$\mu\text{PD4216100}$		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$I_{\text{O}} = 0 \text{ mA}$		2		
	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$		$I_{\text{O}} = 0 \text{ mA}$		1			
$\overline{\text{RAS}}$ only refresh current		I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		100	mA	1, 2, 3, 4
				$t_{\text{RAC}} = 60 \text{ ns}$		90		
				$t_{\text{RAC}} = 70 \text{ ns}$		80		
				$t_{\text{RAC}} = 80 \text{ ns}$		70		
Operating current (Fast page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ $\overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		80	mA	1, 2, 5
				$t_{\text{RAC}} = 60 \text{ ns}$		70		
				$t_{\text{RAC}} = 70 \text{ ns}$		60		
				$t_{\text{RAC}} = 80 \text{ ns}$		50		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		100	mA	1, 2
				$t_{\text{RAC}} = 60 \text{ ns}$		90		
				$t_{\text{RAC}} = 70 \text{ ns}$		80		
				$t_{\text{RAC}} = 80 \text{ ns}$		70		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (4 096 cycles / 128 ms, only for $\mu\text{PD42S16100}$)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : 4 096 cycles/128 ms $\overline{\text{RAS}}, \overline{\text{CAS}} : 0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{H}} \leq V_{\text{HMAX}}$ Standby : $\overline{\text{RAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : Don't care $\overline{\text{WE}} : V_{\text{IH}}$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAS}} \leq 300 \text{ ns}$		450	μA	1, 2
				$t_{\text{RAS}} \leq 1 \mu\text{s}$		600		
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for $\mu\text{PD42S16100}$)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}} : 0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $I_{\text{O}} = 0 \text{ mA}$			250	μA	2
Input leakage current		I _{I(L)}	$V_{\text{I}} = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA		
Output leakage current		I _{O(L)}	$V_{\text{O}} = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10	μA		
High level output voltage		V _{OH}	$I_{\text{O}} = -5.0 \text{ mA}$	2.4		V		
Low level output voltage		V _{OL}	$I_{\text{O}} = +4.2 \text{ mA}$		0.4	V		

[μ PD42S17100, 4217100]

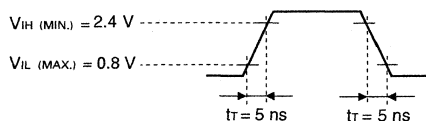
Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		120	mA	1, 2, 3
				$\text{trac} = 60 \text{ ns}$		110		
				$\text{trac} = 70 \text{ ns}$		100		
				$\text{trac} = 80 \text{ ns}$		90		
Standby current	$\mu\text{PD42S17100}$	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$	$I_o = 0 \text{ mA}$		2	mA	
	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$		$I_o = 0 \text{ mA}$		0.25			
	$\mu\text{PD4217100}$		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$	$I_o = 0 \text{ mA}$		2		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$	$I_o = 0 \text{ mA}$		1		
$\overline{\text{RAS}}$ only refresh current		I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		120	mA	1, 2, 3, 4
				$\text{trac} = 60 \text{ ns}$		110		
				$\text{trac} = 70 \text{ ns}$		100		
				$\text{trac} = 80 \text{ ns}$		90		
Operating current (Fast page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{IL}(\text{MAX.})$ $\overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		80	mA	1, 2, 5
				$\text{trac} = 60 \text{ ns}$		70		
				$\text{trac} = 70 \text{ ns}$		60		
				$\text{trac} = 80 \text{ ns}$		50		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		120	mA	1, 2
				$\text{trac} = 60 \text{ ns}$		110		
				$\text{trac} = 70 \text{ ns}$		100		
				$\text{trac} = 80 \text{ ns}$		90		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (2 048 cycles/128 ms, only for $\mu\text{PD42S17100}$)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : 2 048 cycles/128 ms $\overline{\text{RAS}}, \overline{\text{CAS}} : 0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(\text{MAX.})}$ Standby : $\overline{\text{RAS}} \geq V_{CC} - 0.2 \text{ V}$ Address : Don't care $\overline{\text{WE}} : V_{IH}$ $I_o = 0 \text{ mA}$	$\text{tras} \leq 300 \text{ ns}$		400	μA	1, 2
				$\text{tras} \leq 1 \mu\text{s}$		500		
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for $\mu\text{PD42S17100}$)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}} : 0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH}(\text{MAX.})$ $I_o = 0 \text{ mA}$			250	μA	2
Input leakage current		I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V		-10	+10	μA	
Output leakage current		I _{O(L)}	$V_o = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)		-10	+10	μA	
High level output voltage		V _{OH}	$I_o = -5.0 \text{ mA}$		2.4		V	
Low level output voltage		V _{OL}	$I_o = +4.2 \text{ mA}$			0.4	V	

- Notes**
1. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC5} , I_{CC6} and I_{CC7} depend on cycle rates (t_{RC} and t_{PC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \equiv V_{IL} (MAX.)$ and $\overline{CAS} \equiv V_{IH} (MIN.)$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

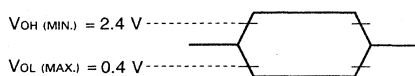
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t _{TRAC} = 50 ns		t _{TRAC} = 60 ns		t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{RC}	90	–	110	–	130	–	150	–	ns	
RAS Precharge Time	t _{RP}	30	–	40	–	50	–	60	–	ns	
CAS Precharge Time	t _{CPN}	8	–	10	–	10	–	10	–	ns	
RAS Pulse Width	t _{RA}	50	10 000	60	10 000	70	10 000	80	10 000	ns	
CAS Pulse Width	t _{CA}	13	10 000	15	10 000	18	10 000	20	10 000	ns	
RAS Hold Time	t _{RSH}	13	–	15	–	18	–	20	–	ns	
CAS Hold Time	t _{CSH}	50	–	60	–	70	–	80	–	ns	
RAS to CAS Delay Time	t _{RC}	18	32	20	40	20	50	25	60	ns	1
RAS to Column Address Delay Time	t _{RA}	13	25	15	30	15	35	17	40	ns	1
CAS to RAS Precharge Time	t _{CRP}	5	–	5	–	5	–	5	–	ns	2
Row Address Setup Time	t _{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t _{RAH}	8	–	10	–	10	–	12	–	ns	
Column Address Setup Time	t _{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t _{CAH}	13	–	15	–	15	–	15	–	ns	
CAS to Data Setup Time	t _{CLZ}	0	–	0	–	0	–	0	–	ns	
Transition Time (Rise and Fall)	t _r	3	50	3	50	3	50	3	50	ns	
Refresh Time	μ PD42S16100, 42S17100	t _{REF}	–	128	–	128	–	128	–	ms	3
	μ PD4216100		–	64	–	64	–	64	–		
	μ PD4217100		–	32	–	32	–	32	–		

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
t _{RA} ≤ t _{RA} (MAX.) and t _{RC} ≤ t _{RC} (MAX.)	t _{TRAC} (MAX.)	t _{TRAC} (MAX.)
t _{RA} > t _{RA} (MAX.) and t _{RC} ≤ t _{RC} (MAX.)	t _{TAA} (MAX.)	t _{RA} + t _{TAA} (MAX.)
t _{RC} > t _{RC} (MAX.)	t _{TCAC} (MAX.)	t _{RC} + t _{TCAC} (MAX.)

t_{RA}(MAX.) and t_{RC}(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{TRAC}, t_{TAA} or t_{TCAC}) is to be used for finding out when output data will be available. Therefore, the input conditions t_{RA} ≥ t_{RA} (MAX.) and t_{RC} ≥ t_{RC} (MAX.) will not cause any operation problems.

2. t_{CRP}(MIN.) requirement is applied to RAS, CAS cycles preceded by any cycle.

3. This specification is applied only to the μ PD42S16100, 42S17100.

Read Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from RAS	t _{RAC}	–	50	–	60	–	70	–	80	ns	1
Access Time from CAS	t _{CAC}	–	13	–	15	–	18	–	20	ns	1
Access Time from Column Address	t _{AA}	–	25	–	30	–	35	–	40	ns	1
Column Address Lead Time Referenced to RAS	t _{RAL}	25	–	30	–	35	–	40	–	ns	
Read Command Setup Time	t _{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	0	–	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to CAS	t _{RCH}	0	–	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from CAS	t _{OFF}	0	10	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
t _{RAD} $\leq$ t _{RAD} (MAX.) and t _{RC} $\leq$ t _{RC} (MAX.)	t _{RAC} (MAX.)	t _{RAC} (MAX.)
t _{RAD} > t _{RAD} (MAX.) and t _{RC} $\leq$ t _{RC} (MAX.)	t _{AA} (MAX.)	t _{RAD} + t _{AA} (MAX.)
t _{RC} > t _{RC} (MAX.)	t _{CAC} (MAX.)	t _{RC} + t _{CAC} (MAX.)

t_{RAD}(MAX.) and t_{RC}(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions t_{RAD} $\geq$ t_{RAD}(MAX.) and t_{RC} $\geq$ t_{RC}(MAX.) will not cause any operation problems.

2. Either t_{RRH}(MIN.) or t_{RRH}(MIN.) should be met in read cycles.
3. t_{OFF}(MAX.) defines the time when the output achieves the condition of Hi - Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
WE Hold Time Referenced to $\overline{\text{CAS}}$	twch	8	–	10	–	10	–	15	–	ns	1
WE Pulse Width	twp	8	–	10	–	10	–	15	–	ns	1
WE Lead Time Referenced to $\overline{\text{RAS}}$	trwl	18	–	20	–	20	–	20	–	ns	
WE Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	13	–	15	–	15	–	15	–	ns	
WE Setup Time	twcs	0	–	0	–	0	–	0	–	ns	2
Data-in Setup Time	tds	0	–	0	–	0	–	0	–	ns	3
Data-in Hold Time	tdh	10	–	10	–	15	–	15	–	ns	3

- Notes**
1. $t_{wp}(\text{MIN.})$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{wch}(\text{MIN.})$ should be met.
 2. If $t_{wcs} \geq t_{wcs}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle.
 3. $t_{ds}(\text{MIN.})$ and $t_{dh}(\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	113	–	135	–	155	–	175	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	50	–	60	–	70	–	80	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	13	–	15	–	18	–	20	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	25	–	30	–	35	–	40	–	ns	1

- Note**
1. If $t_{wcs} \geq t_{wcs}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{rwd} \geq t_{rwd}(\text{MIN.})$, $t_{cwd} \geq t_{cwd}(\text{MIN.})$, $t_{awd} \geq t_{awd}(\text{MIN.})$ and $t_{cpwd} \geq t_{cpwd}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	35	–	40	–	45	–	50	–	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	–	30	–	35	–	40	–	45	ns	
RAS Pulse Width	t _{RASP}	50	125 000	60	125 000	70	125 000	80	125 000	ns	
CAS Precharge Time	t _{CP}	8	–	10	–	10	–	10	–	ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	–	35	–	40	–	45	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	55	–	60	–	65	–	75	–	ns	
CAS Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	50	–	58	–	65	–	70	–	ns	1

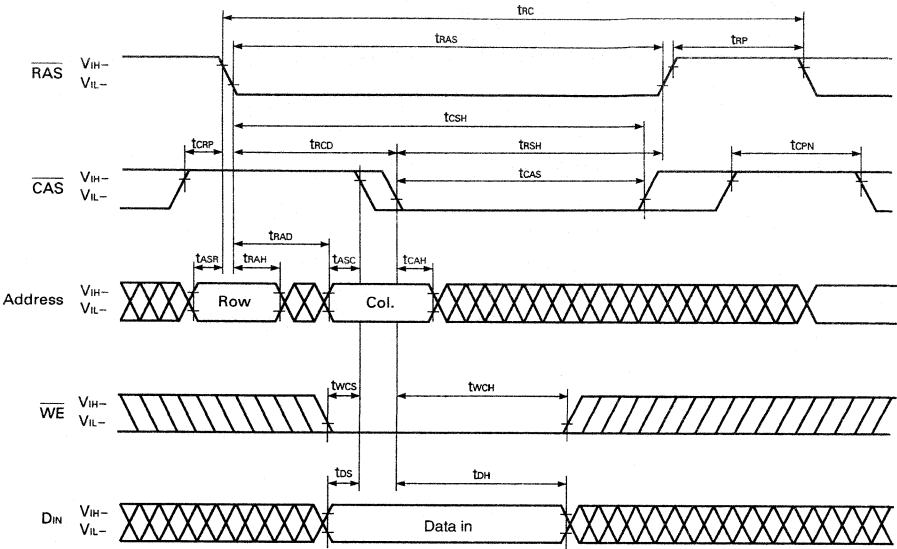
Note 1. If $t_{\text{WCS}} \geq t_{\text{WCS(MIN.)}}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD(MIN.)}}$, $t_{\text{CWD}} \geq t_{\text{CWD(MIN.)}}$, $t_{\text{AWD}} \geq t_{\text{AWD(MIN.)}}$ and $t_{\text{CPWD}} \geq t_{\text{CPWD(MIN.)}}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

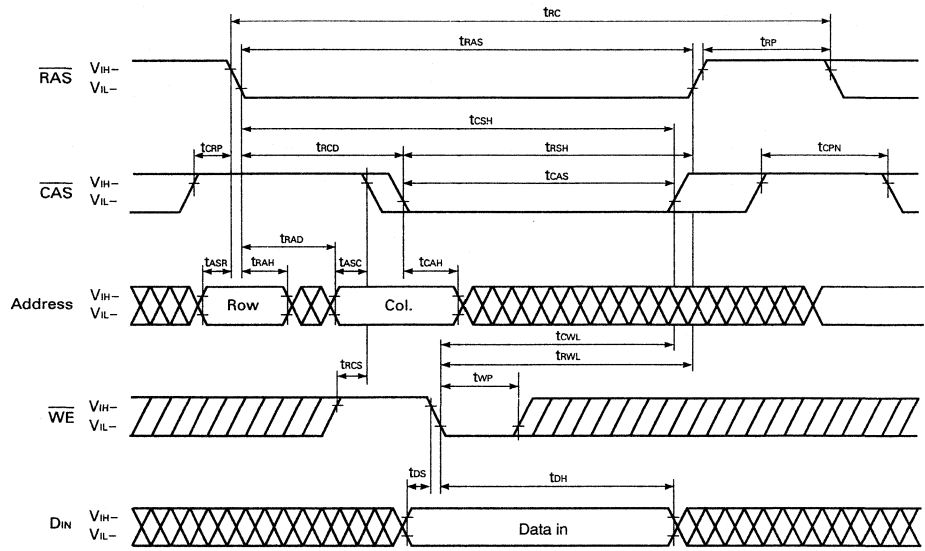
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	–	5	–	5	–	5	–	ns	
CAS Hold Time ($\overline{\text{CAS}}$ before RAS Refresh)	t _{CHR}	10	–	10	–	10	–	10	–	ns	
RAS Precharge CAS Hold Time	t _{RPC}	5	–	5	–	5	–	5	–	ns	
RAS Pulse Width ($\overline{\text{CAS}}$ before RAS Self Refresh Cycle)	t _{RASS}	100	–	100	–	100	–	100	–	μ s	1
RAS Precharge Time ($\overline{\text{CAS}}$ before RAS Self Refresh Cycle)	t _{RPS}	90	–	110	–	130	–	150	–	ns	1
CAS Hold Time ($\overline{\text{CAS}}$ before RAS Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15	–	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μ PD42S16100, 42S17100.

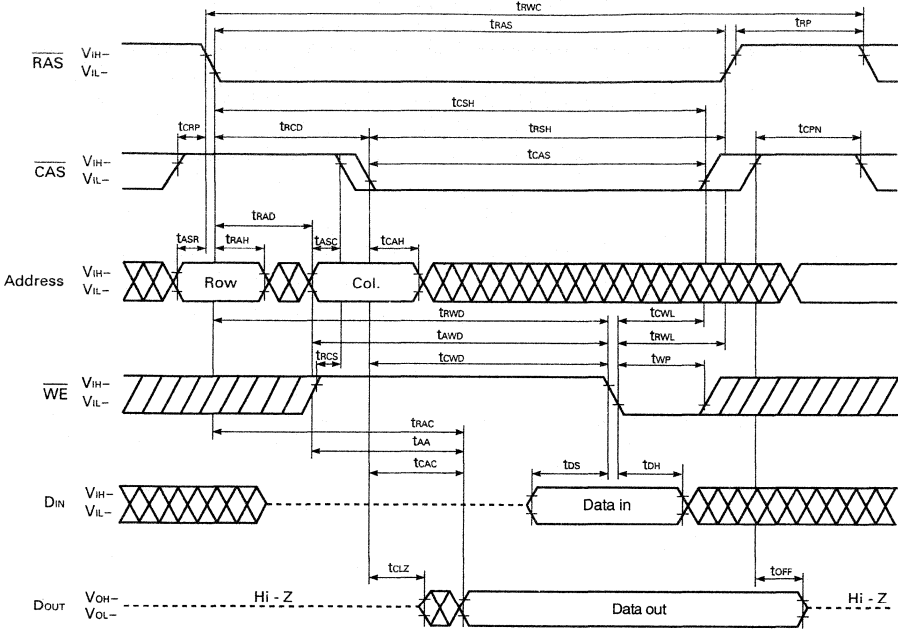
Early Write Cycle



Late Write Cycle



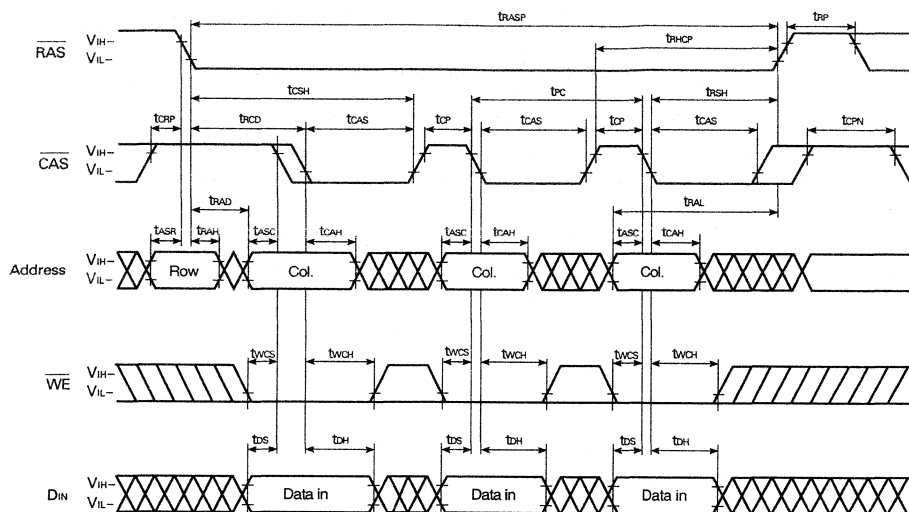
Read Modify Write Cycle



[illegible]

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Fast Page Mode Early Write Cycle

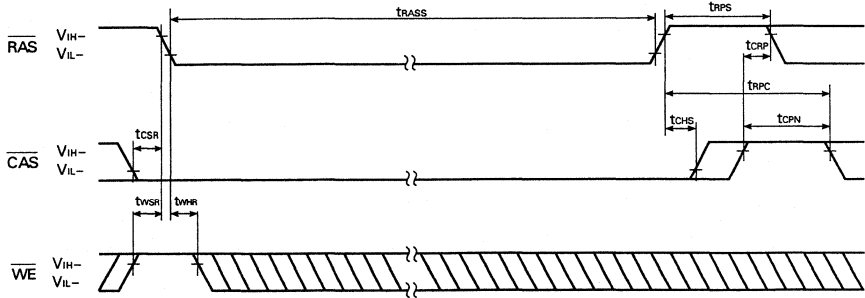


Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

[illegible]

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CAS Before RAS Self Refresh Cycle (Only for the μ PD42S16100, 42S17100)



Remark Address, D_{IN} : Don't care D_{OUT} : Hi-Z

★ **Cautions on Use of CAS Before RAS Self Refresh**

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16100 : 4 096 times within a 64 ms interval

μ PD42S17100 : 2 048 times within a 32 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

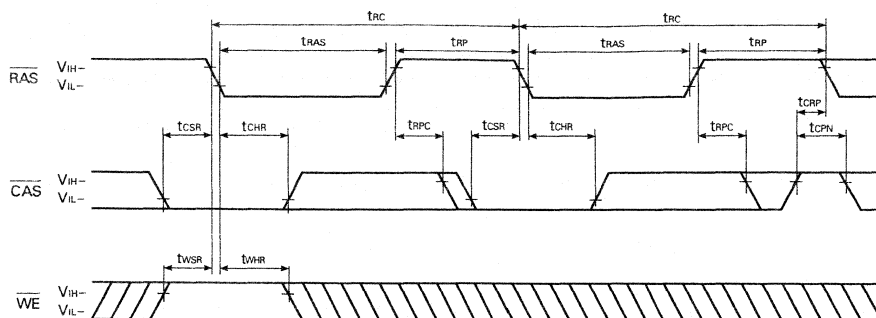
When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16100 : 4 096 times within a 64 ms interval

μ PD42S17100 : 2 048 times within a 32 ms interval

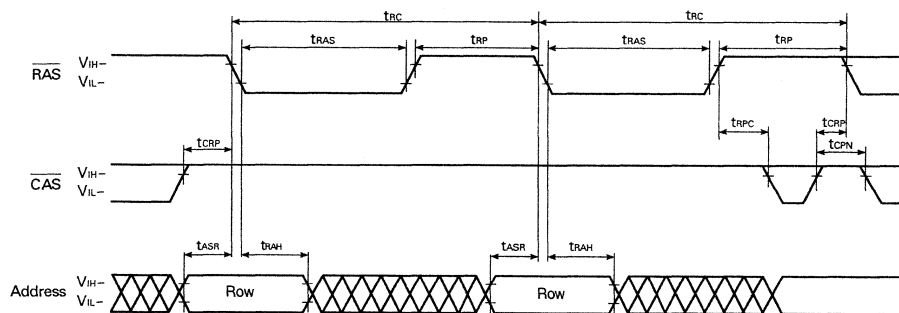
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



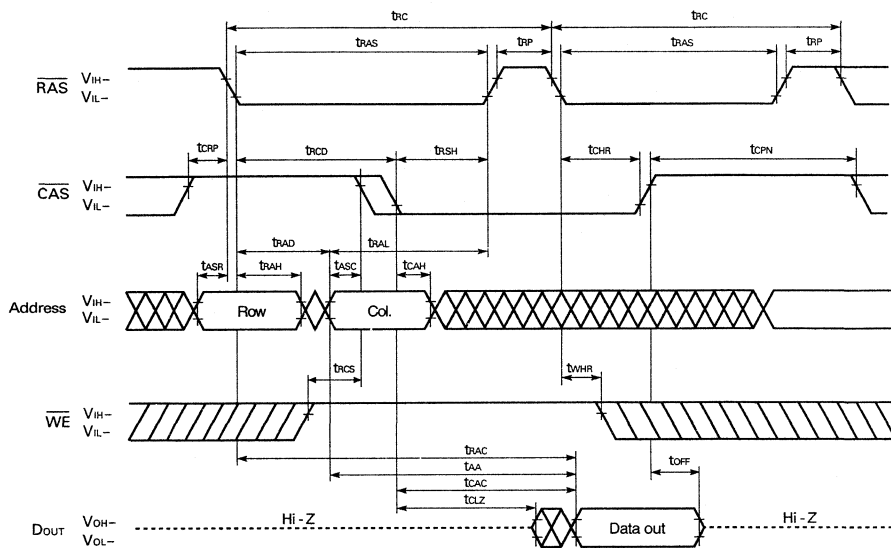
Remark Address, D_{IN} : Don't care D_{OUT} : Hi - Z

RAS Only Refresh Cycle



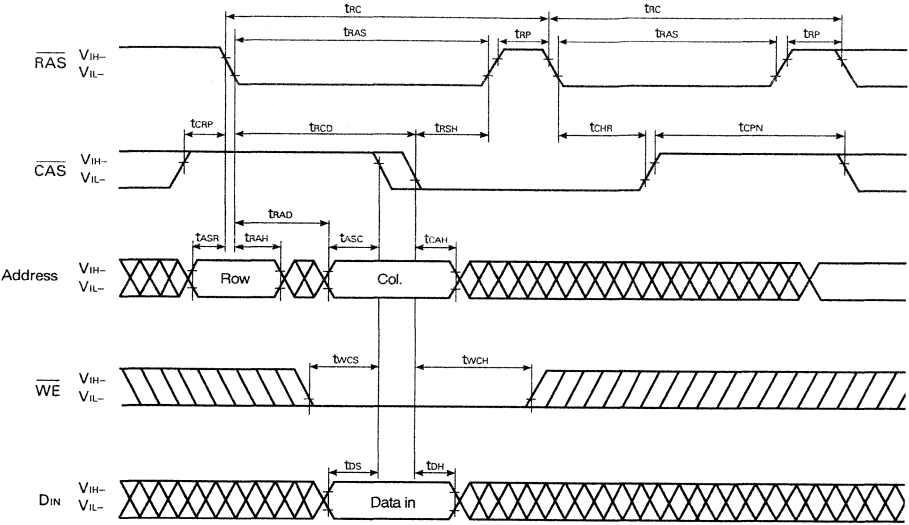
Remark $\overline{\text{WE}}$, D_{IN} : Don't care D_{OUT} : Hi - Z

★ Hidden Refresh Cycle (Read)



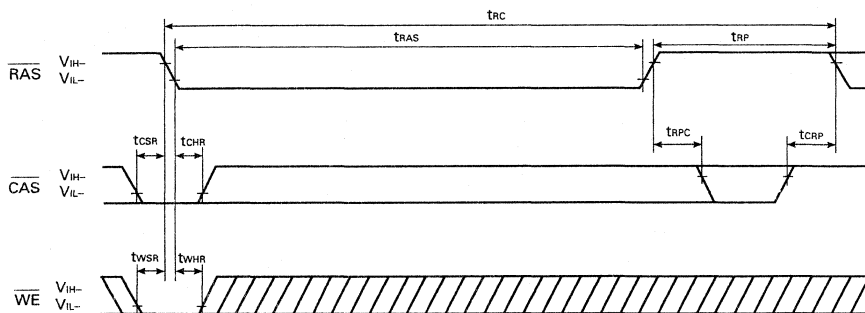
Remark D_{IN} : Don't care

Hidden Refresh Cycle (Write)



Remark D_{OUT} : Hi-Z

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)



Remark Address, D_{IN} : Don't care D_{OUT} : Hi - Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 16$ -bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1" : Normal write (all memory cells)

Output = "0" : Abnormal write

(3) Refresh

Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

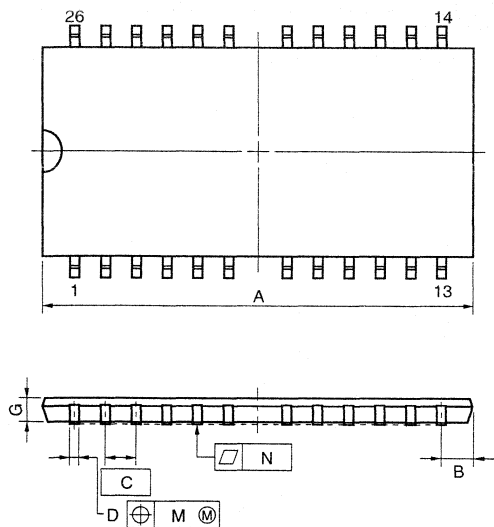
(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

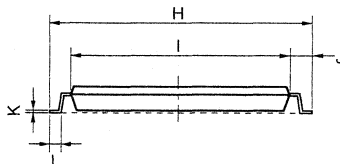
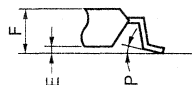
Package Drawings



26PIN PLASTIC TSOP(II) (300 mil)



detail of lead end



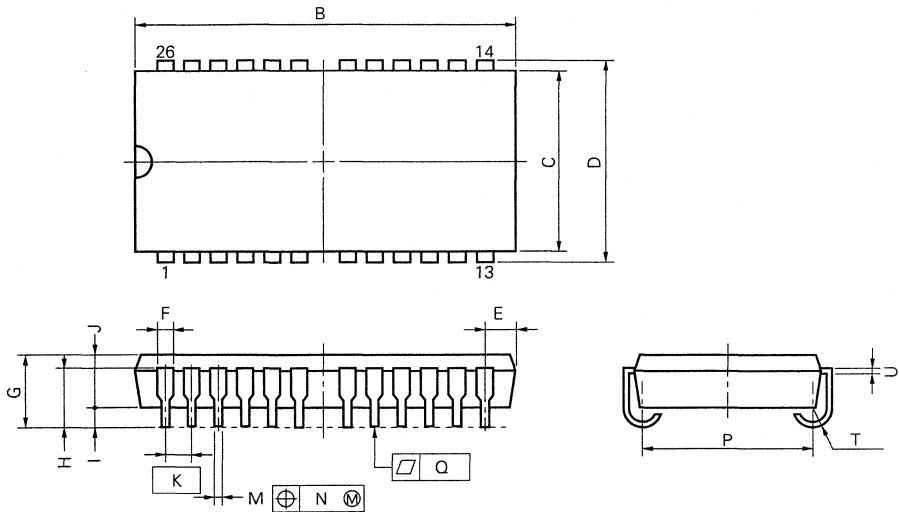
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.42 ^{+0.08} _{-0.07}	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S26LA-300A

ITEM	MILLIMETERS	INCHES
B	17.1 ^{+0.25} _{-0.05}	0.673 ^{+0.010} _{-0.002}
C	7.62	0.300
D	8.47±0.2	0.333 ^{+0.009} _{-0.008}
E	1.03±0.15	0.041 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

Recommended Soldering Conditions



The following conditions (see table below) must be met for soldering conditions of the μPD42S16100, 4216100, 42S17100, 4217100.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Type of Surface Mount Device

μPD42S16100G3, 4216100G3, 42S17100G3, 4217100G3 : 26-pin Plastic TSOP (II) (300 mil)

Please consult with our sales offices.

μPD42S16100LA, 4216100LA, 42S17100LA, 4217100LA

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

MOS INTEGRATED CIRCUIT

μ PD42S16400, 4216400, 42S17400, 4217400

16 M-BIT DYNAMIC RAM

4 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μ PD42S16400, 4216400, 42S17400, 4217400 are 4 194 304 words by 4 bits dynamic CMOS RAMs.

These differ in refresh cycle and the μ PD42S16400, 42S17400 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (see the table below).

These are packed in 26-pin plastic TSOP (II) and 26-pin plastic SOJ.



Features

- 4 194 304 words by 4 bits organization
- Single +5.0 V $\pm$ 10 % power supply
- Fast page mode
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S16400-50, 4216400-50	550 mW	50 ns	90 ns	35 ns
μ PD42S17400-50, 4217400-50	660 mW			
μ PD42S16400-60, 4216400-60	495 mW	60 ns	110 ns	40 ns
μ PD42S17400-60, 4217400-60	605 mW			
μ PD42S16400-70, 4216400-70	440 mW	70 ns	130 ns	45 ns
μ PD42S17400-70, 4217400-70	550 mW			
μ PD42S16400-80, 4216400-80	385 mW	80 ns	150 ns	50 ns
μ PD42S17400-80, 4217400-80	495 mW			

- The μ PD42S16400, 42S17400 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S16400	4 096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μ PD42S17400	2 048 cycles/128 ms		
μ PD4216400	4 096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)
μ PD4217400	2 048 cycles/32 ms		

The information in this document is subject to change without notice.

The mark ★ shows revised points.



Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD42S16400G3-50-7JD	50 ns	26-pin Plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S17400G3-50-7JD			
μ PD42S16400G3-60-7JD	60 ns		
μ PD42S17400G3-60-7JD			
μ PD42S16400G3-70-7JD	70 ns		
μ PD42S17400G3-70-7JD			
μ PD42S16400G3-80-7JD	80 ns		
μ PD42S17400G3-80-7JD			
μ PD42S16400LA-50	50 ns	26-pin Plastic SOJ (300 mil)	
μ PD42S17400LA-50			
μ PD42S16400LA-60	60 ns		
μ PD42S17400LA-60			
μ PD42S16400LA-70	70 ns		
μ PD42S17400LA-70			
μ PD42S16400LA-80	80 ns		
μ PD42S17400LA-80			
μ PD4216400G3-50-7JD	50 ns	26-pin Plastic TSOP (II) (300 mil)	
μ PD4217400G3-50-7JD			
μ PD4216400G3-60-7JD	60 ns		
μ PD4217400G3-60-7JD			
μ PD4216400G3-70-7JD	70 ns		
μ PD4217400G3-70-7JD			
μ PD4216400G3-80-7JD	80 ns		
μ PD4217400G3-80-7JD			
μ PD4216400LA-50	50 ns	26-pin Plastic SOJ (300 mil)	
μ PD4217400LA-50			
μ PD4216400LA-60	60 ns		
μ PD4217400LA-60			
μ PD4216400LA-70	70 ns		
μ PD4217400LA-70			
μ PD4216400LA-80	80 ns		
μ PD4217400LA-80			

Quality Grade

Standard

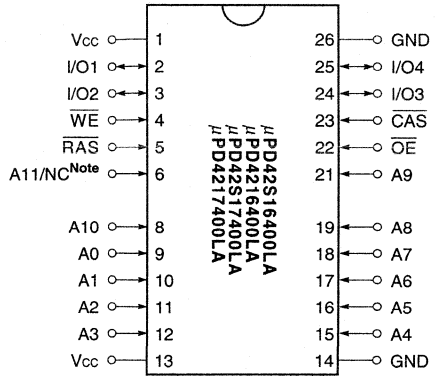
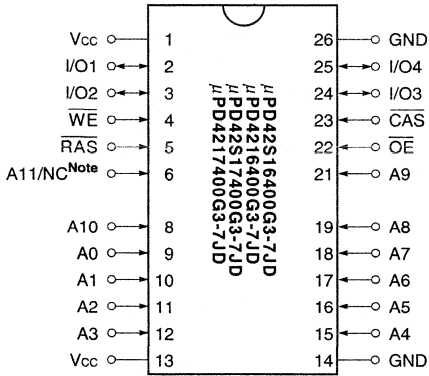
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking Side)



26-pin Plastic TSOP (II) (300 mil)

26-pin Plastic SOJ (300 mil)

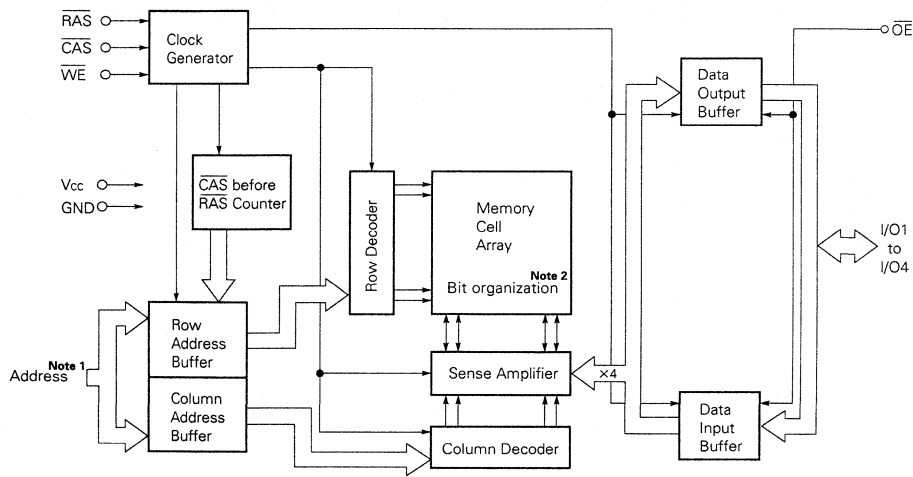


Note A11 ... μPD42S16400, 4216400

NC ... μPD42S17400, 4217400

- A0 to A11 : Address Inputs
- I/O1 to I/O4 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μ PD42S16400, 4216400	A0 to A11	A0 to A9
μ PD42S17400, 4217400	A0 to A10	A0 to A10

2. μ PD42S16400, 4216400...4 096 $\times$ 1 024 $\times$ 4 μ PD42S17400, 4217400...2 048 $\times$ 2 048 $\times$ 4

Input/Output Pin Functions

The μ PD42S16400, 4216400, 42S17400, 4217400 have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11/A10^{Note1} and input/output pins I/O1 to I/O4.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11/A10 ^{Note1} (Address inputs)		Address bus. Input total 22-bit of address signal, upper 12/11^{Note2}-bit and lower 10/11^{Note3}-bit in sequence (address multiplex method). Therefore, one word is selected from 4 194 304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (tASR, tASC) and hold time (tRAH, tCAH) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/ Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Notes 1. A11 ... μ PD42S16400, 4216400 A10 ... μ PD42S17400, 4217400
 2. 12 ... μ PD42S16400, 4216400 11 ... μ PD42S17400, 4217400
 3. 10 ... μ PD42S16400, 4216400 11 ... μ PD42S17400, 4217400

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

★

Capacitance ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)[μ PD42S16400, 4216400]

Parameter		Symbol	Test Condition		MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{cc1}	RAS, $\overline{\text{CAS}}$ Cycling trc = trc (MIN.) Io = 0 mA	trac = 50 ns			100	mA	1, 2, 3
				trac = 60 ns			90		
				trac = 70 ns			80		
				trac = 80 ns			70		
Standby current	μ PD42S16400	I _{cc2}	RAS, $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.), Io = 0 mA				2	mA	
	RAS, $\overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$, Io = 0 mA					0.25			
	RAS, $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.), Io = 0 mA					2			
	RAS, $\overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$, Io = 0 mA					1			
RAS only refresh current		I _{cc3}	RAS Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.) trc = trc (MIN.), Io = 0 mA	trac = 50 ns			100	mA	1,2,3,4
				trac = 60 ns			90		
				trac = 70 ns			80		
				trac = 80 ns			70		
Operating current (Fast page mode)		I _{cc4}	RAS $\leq V_{\text{IL}}$ (MAX.), $\overline{\text{CAS}}$ Cycling tpc = tpc (MIN.), Io = 0 mA	trac = 50 ns			80	mA	1, 2, 5
				trac = 60 ns			70		
				trac = 70 ns			60		
				trac = 80 ns			50		
CAS before RAS refresh current		I _{cc5}	RAS Cycling trc = trc (MIN.) Io = 0 mA	trac = 50 ns			100	mA	1, 2
				trac = 60 ns			90		
				trac = 70 ns			80		
				trac = 80 ns			70		
CAS before RAS long refresh current (4 096 Cycles/128 ms, only for the μ PD42S16400)		I _{cc6}	CAS before RAS refresh : 4 096 Cycles / 128 ms RAS, $\overline{\text{CAS}}$: $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}$ (MAX.) $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby : RAS $\geq V_{\text{CC}} - 0.2 \text{ V}$ Address : Don't care $\overline{\text{WE}}, \overline{\text{OE}} : V_{\text{IH}}$ Io = 0 mA	tras $\leq$ 300 ns			450	μA	1, 2
				tras $\leq$ 1 μs			600		
Self refresh current (CAS before RAS self refresh, only for the μ PD42S16400)		I _{cc7}	RAS, $\overline{\text{CAS}}$: $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}$ (MAX.) $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Io = 0 mA				250	μA	2
Input leakage current		I _I (L)	V _I = 0 to 5.5 V All other pins not under test = 0 V		-10		+10	μA	
Output leakage current		I _O (L)	V _O = 0 to 5.5 V Output is disabled (Hi-Z)		-10		+10	μA	
High level output voltage		V _{OH}	Io = -5.0 mA		2.4			V	
Low level output voltage		V _{OL}	Io = +4.2 mA				0.4	V	

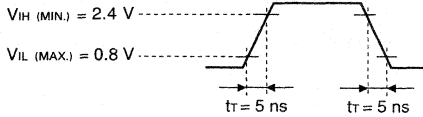
[μ PD42S17400, 4217400]

Parameter		Symbol	Test Condition		MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	RAS, $\overline{\text{CAS}}$ Cycling	t _{RAC} = 50 ns			120	mA	1, 2, 3
			t _{RC} = t _{RC} (MIN.)	t _{RAC} = 60 ns			110		
			I _O = 0 mA	t _{RAC} = 70 ns			100		
				t _{RAC} = 80 ns			90		
Standby current	μ PD42S17400	I _{CC2}	RAS, $\overline{\text{CAS}} \geq V_{IH}$ (MIN.), I _O = 0 mA				2	mA	
	RAS, $\overline{\text{CAS}} \geq V_{CC} - 0.2$ V, I _O = 0 mA					0.25			
	μ PD4217400		RAS, $\overline{\text{CAS}} \geq V_{IH}$ (MIN.), I _O = 0 mA				2		
			RAS, $\overline{\text{CAS}} \geq V_{CC} - 0.2$ V, I _O = 0 mA				1		
RAS only refresh current		I _{CC3}	RAS Cycling, $\overline{\text{CAS}} \geq V_{IH}$ (MIN.) t _{RC} = t _{RC} (MIN.), I _O = 0 mA	t _{RAC} = 50 ns			120	mA	1,2,3,4
				t _{RAC} = 60 ns			110		
				t _{RAC} = 70 ns			100		
				t _{RAC} = 80 ns			90		
Operating current (Fast page mode)		I _{CC4}	RAS $\leq V_{IL}$ (MAX.), $\overline{\text{CAS}}$ Cycling t _{PC} = t _{PC} (MIN.), I _O = 0 mA	t _{RAC} = 50 ns			80	mA	1, 2, 5
				t _{RAC} = 60 ns			70		
				t _{RAC} = 70 ns			60		
				t _{RAC} = 80 ns			50		
CAS before RAS refresh current		I _{CC5}	RAS Cycling t _{RC} = t _{RC} (MIN.) I _O = 0 mA	t _{RAC} = 50 ns			120	mA	1, 2
				t _{RAC} = 60 ns			110		
				t _{RAC} = 70 ns			100		
				t _{RAC} = 80 ns			90		
CAS before RAS long refresh current (2 048 Cycles / 128 ms, only for the μ PD42S17400)		I _{CC6}	$\overline{\text{CAS}}$ before RAS refresh : 2 048 Cycles / 128 ms RAS, $\overline{\text{CAS}}$: V _{CC} -0.2 V $\leq V_{IH} \leq V_{IH}$ (MAX.) 0 V $\leq V_{IL} \leq 0.2$ V Standby : RAS $\geq V_{CC}$ -0.2 V Address : Don't care WE, OE : V _{IH} I _O = 0 mA	t _{RAS} $\leq$ 300 ns			400	μ A	1, 2
				t _{RAS} $\leq$ 1 μ s			500		
Self refresh current (CAS before RAS self refresh, only for the μ PD42S17400)		I _{CC7}	RAS, $\overline{\text{CAS}}$: V _{CC} -0.2 V $\leq V_{IH} \leq V_{IH}$ (MAX.) 0 V $\leq V_{IL} \leq 0.2$ V I _O = 0 mA				250	μ A	2
Input leakage current		I _I (L)	V _I = 0 to 5.5 V All other pins not under test = 0 V		-10		+10	μ A	
Output leakage current		I _O (L)	V _O = 0 to 5.5 V Output is disabled (Hi-Z)		-10		+10	μ A	
High level output voltage		V _{OH}	I _O = -5.0 mA		2.4			V	
Low level output voltage		V _{OL}	I _O = +4.2 mA				0.4	V	

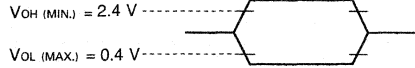
- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
 2. Selected values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during RAS $\leq V_{IL}$ (MAX.) and CAS $\geq V_{IH}$ (MIN.).
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)**AC Characteristics Test Conditions**

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	trac = 50 ns		trac = 60 ns		trac = 70 ns		trac = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	trc	90	–	110	–	130	–	150	–	ns	
RAS Precharge Time	trp	30	–	40	–	50	–	60	–	ns	
CAS Precharge Time	tcpn	8	–	10	–	10	–	10	–	ns	
RAS Pulse Width	trās	50	10 000	60	10 000	70	10 000	80	10 000	ns	
CAS Pulse Width	tcās	13	10 000	15	10 000	18	10 000	20	10 000	ns	
RAS Hold Time	trsh	13	–	15	–	18	–	20	–	ns	
CAS Hold Time	tcsh	50	–	60	–	70	–	80	–	ns	
RAS to CAS Delay Time	trcd	18	32	20	40	20	50	25	60	ns	1
RAS to Column Address Delay Time	trād	13	25	15	30	15	35	17	40	ns	1
CAS to RAS Precharge Time	tcrp	5	–	5	–	5	–	5	–	ns	2
Row Address Setup Time	tasr	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	trah	8	–	10	–	10	–	12	–	ns	
Column Address Setup Time	tasc	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	tcah	13	–	15	–	15	–	15	–	ns	
OE Lead Time Referenced to RAS	toes	0	–	0	–	0	–	0	–	ns	
CAS to Data Setup Time	tclz	0	–	0	–	0	–	0	–	ns	
OE to Data Setup Time	tolz	0	–	0	–	0	–	0	–	ns	
OE to Data Delay Time	toed	10	–	15	–	15	–	20	–	ns	
Transition Time (Rise and Fall)	tr	3	50	3	50	3	50	3	50	ns	
Refresh Time	μ PD42S16400, 42S17400	tr _{EF}	–	128	–	128	–	128	–	ms	3
	μ PD4216400		–	64	–	64	–	64	–		
	μ PD4217400		–	32	–	32	–	32	–		

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$tr_{AD} \leq tr_{AD} (\text{MAX.})$ and $tr_{CD} \leq tr_{CD} (\text{MAX.})$	$tr_{AC} (\text{MAX.})$	$tr_{AC} (\text{MAX.})$
$tr_{AD} > tr_{AD} (\text{MAX.})$ and $tr_{CD} \leq tr_{CD} (\text{MAX.})$	$t_{AA} (\text{MAX.})$	$tr_{AD} + t_{AA} (\text{MAX.})$
$tr_{CD} > tr_{CD} (\text{MAX.})$	$t_{CAC} (\text{MAX.})$	$tr_{CD} + t_{CAC} (\text{MAX.})$

$tr_{AD} (\text{MAX.})$ and $tr_{CD} (\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (tr_{AC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $tr_{AD} \geq tr_{AD} (\text{MAX.})$ and $tr_{CD} \geq tr_{CD} (\text{MAX.})$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.
3. This specification is applied only to the μ PD42S16400, 42S17400.

Read Cycle

Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		$t_{RAC} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	–	80	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	–	20	ns	1
Access Time from Column Address	t_{AA}	–	25	–	30	–	35	–	40	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	–	20	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	40	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	10	0	15	0	15	0	20	ns	3
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	10	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}(\text{MAX.})$ and $t_{RCD} \leq t_{RCD}(\text{MAX.})$	$t_{RAC}(\text{MAX.})$	$t_{RAC}(\text{MAX.})$
$t_{RAD} > t_{RAD}(\text{MAX.})$ and $t_{RCD} \leq t_{RCD}(\text{MAX.})$	$t_{AA}(\text{MAX.})$	$t_{RAD} + t_{AA}(\text{MAX.})$
$t_{RCD} > t_{RCD}(\text{MAX.})$	$t_{CAC}(\text{MAX.})$	$t_{RCD} + t_{CAC}(\text{MAX.})$

$t_{RAD}(\text{MAX.})$ and $t_{RCD}(\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}(\text{MAX.})$ and $t_{RCD} \geq t_{RCD}(\text{MAX.})$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OFF}(\text{MAX.})$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi - Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{WAC} = 50 ns		t _{WAC} = 60 ns		t _{WAC} = 70 ns		t _{WAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
WE Hold Time Referenced to $\overline{\text{CAS}}$	twch	8	–	10	–	10	–	15	–	ns	1
WE Pulse Width	twp	8	–	10	–	10	–	15	–	ns	1
WE Lead Time Referenced to $\overline{\text{RAS}}$	trwl	18	–	20	–	20	–	20	–	ns	
WE Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	13	–	15	–	15	–	15	–	ns	
WE Setup Time	twcs	0	–	0	–	0	–	0	–	ns	2
OE Hold Time	toeh	0	–	0	–	0	–	0	–	ns	
Data-in Setup Time	tds	0	–	0	–	0	–	0	–	ns	3
Data-in Hold Time	tdh	10	–	10	–	15	–	15	–	ns	3

- Notes**
1. t_{WAC} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch (MIN.) should be met.
 2. If twcs $\geq$ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle.
 3. tds (MIN.) and tdh (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the WE falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{WAC} = 50 ns		t _{WAC} = 60 ns		t _{WAC} = 70 ns		t _{WAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	140	–	160	–	180	–	205	–	ns	
RAS to WE Delay Time	trwd	70	–	85	–	95	–	110	–	ns	1
CAS to WE Delay Time	tcwd	33	–	40	–	43	–	50	–	ns	1
Column Address to WE Delay Time	tawd	45	–	55	–	60	–	70	–	ns	1

- Note**
1. If twcs $\geq$ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If trwd $\geq$ trwd (MIN.), tcwd $\geq$ tcwd (MIN.), tawd $\geq$ tawd (MIN.) and tcpwd $\geq$ tcpwd (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	35	–	40	–	45	–	50	–	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	–	30	–	35	–	40	–	45	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RASP}	50	125 000	60	125 000	70	125 000	80	125 000	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	8	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	–	35	–	40	–	45	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	80	–	85	–	90	–	105	–	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	50	–	58	–	65	–	70	–	ns	1

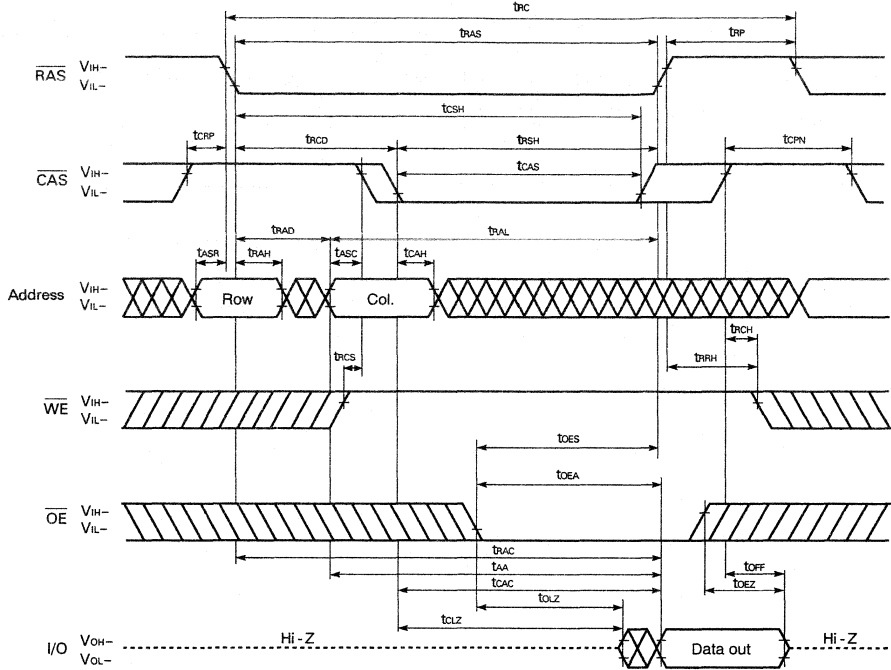
Note 1. If $\text{twcs} \geq \text{twcs}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $\text{trwd} \geq \text{trwd}(\text{MIN.})$, $\text{tcwd} \geq \text{tcwd}(\text{MIN.})$, $\text{tawd} \geq \text{tawd}(\text{MIN.})$ and $\text{tcpwd} \geq \text{tcpwd}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

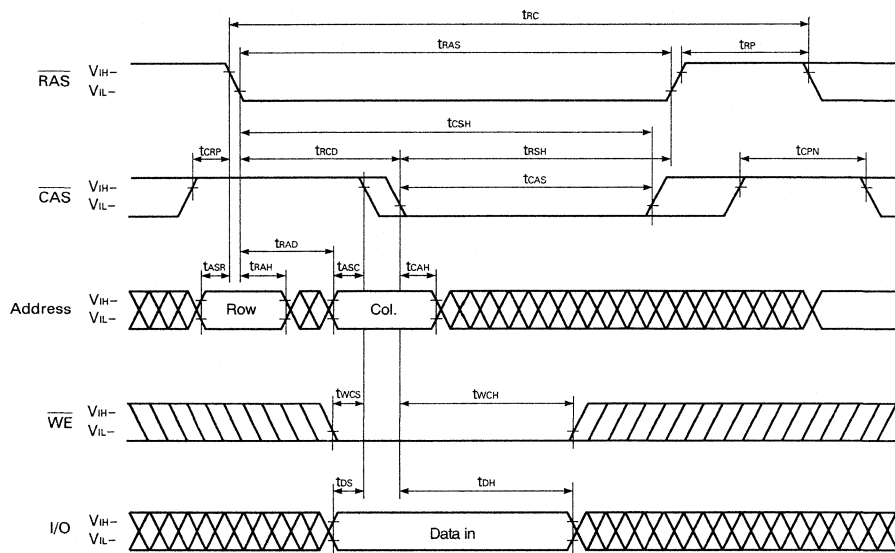
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ Setup Time	t _{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RASS}	100	–	100	–	100	–	100	–	μs	1
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RPS}	90	–	110	–	130	–	150	–	ns	1
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15	–	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S16400, 42S17400.

Read Cycle

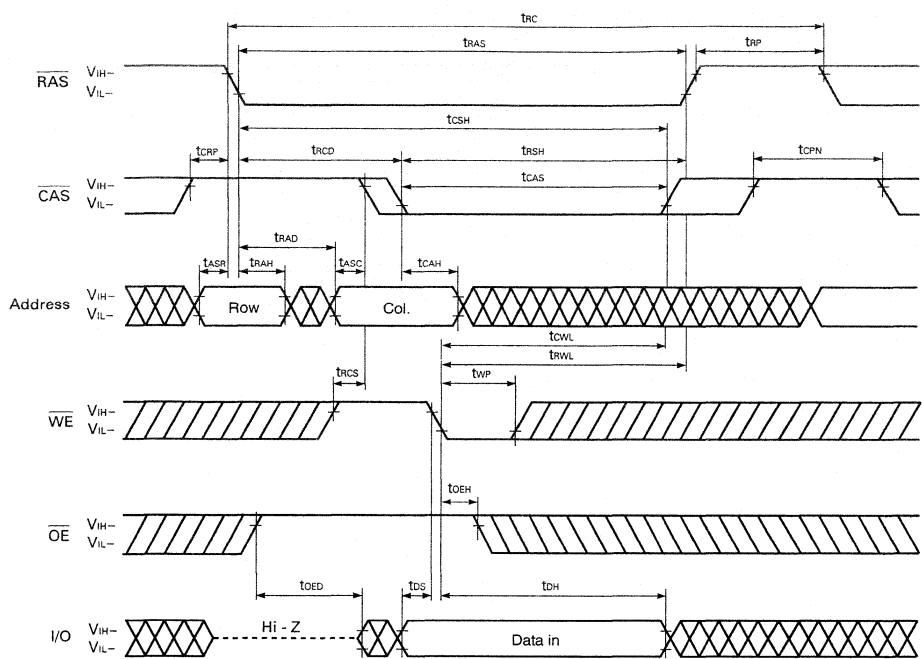


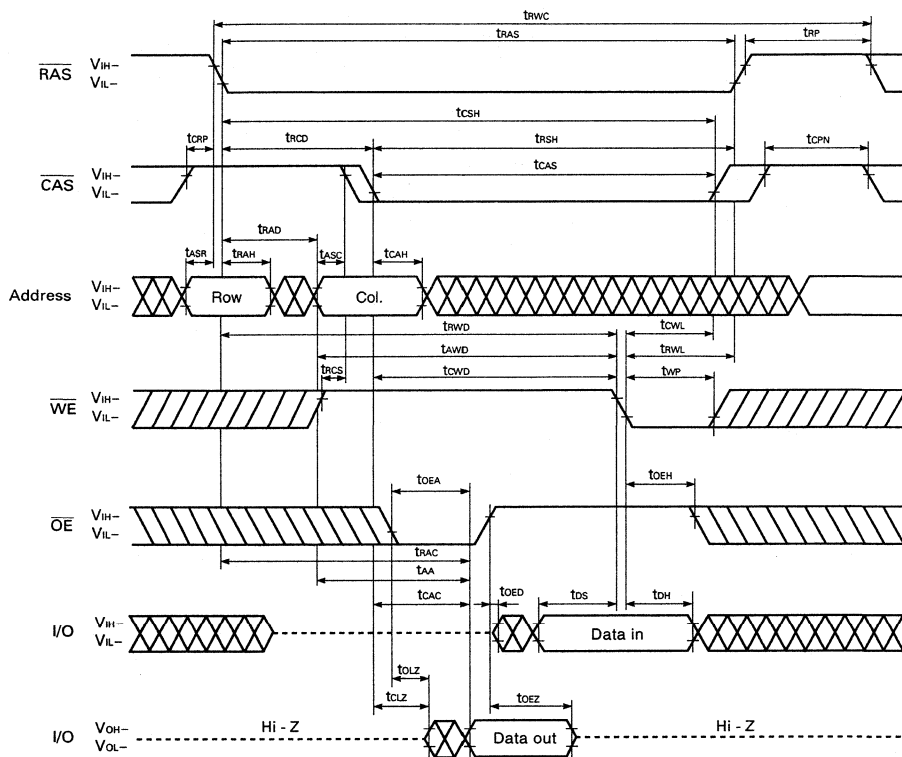
Early Write Cycle



Remark $\overline{\text{OE}}$: Don't care

Late Write Cycle

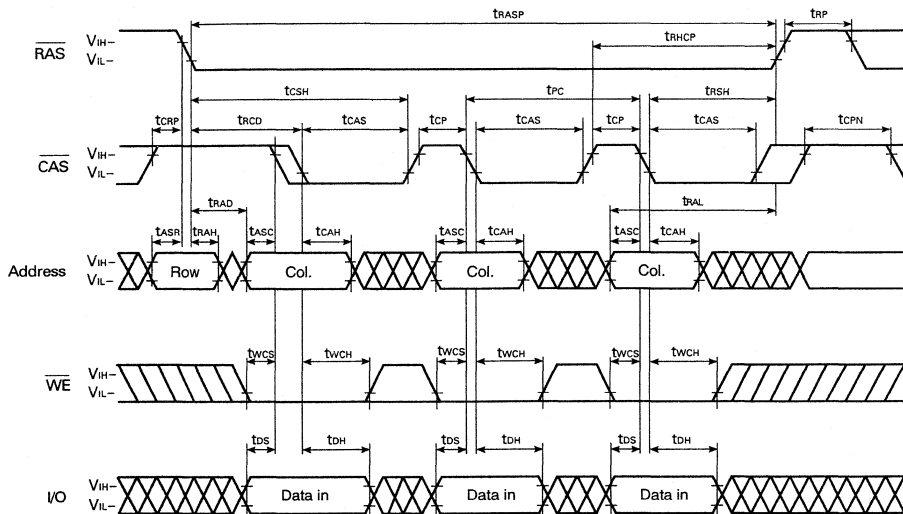




[illegible]

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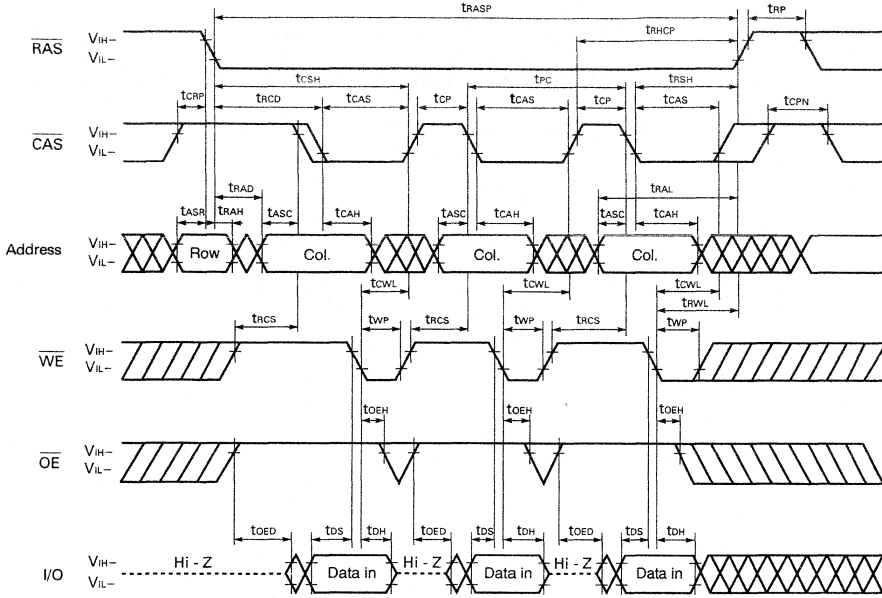
Fast Page Mode Early Write Cycle



Remark $\overline{\text{OE}}$: Don't care

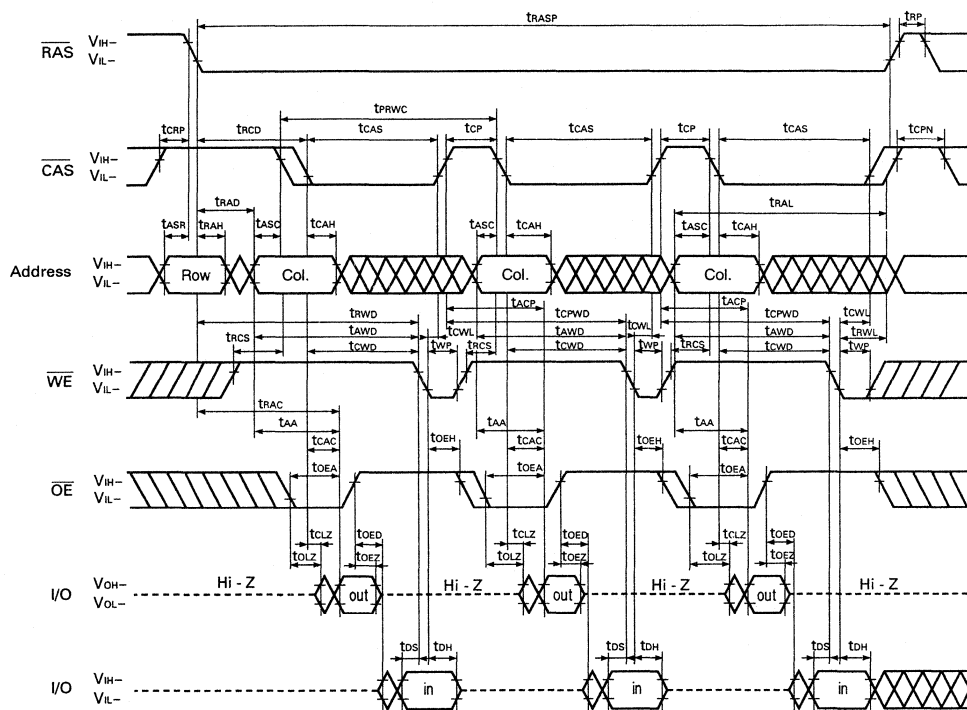
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

The timing diagram illustrates the relationship between the RAS, CAS, and WE signals and their respective timing parameters. The signals are shown as voltage levels over time, with the RAS and CAS signals being active-low and the WE signal being active-low. The timing parameters are defined as follows:

- trass**: RAS access time, the time from the falling edge of RAS to the start of data output.
- trps**: RAS pulse width, the time from the falling edge of RAS to the rising edge of RAS.
- tcsr**: CAS setup time, the time from the falling edge of CAS to the start of data output.
- twsr**: CAS setup time, the time from the falling edge of CAS to the start of data output.
- twhr**: CAS hold time, the time from the rising edge of CAS to the end of data output.
- tcpr**: CAS pulse width, the time from the falling edge of CAS to the rising edge of CAS.
- trpc**: RAS pulse width, the time from the falling edge of RAS to the rising edge of RAS.
- tcps**: CAS pulse width, the time from the falling edge of CAS to the rising edge of CAS.
- tcprn**: CAS pulse width, the time from the falling edge of CAS to the rising edge of CAS.
- tcpsn**: CAS pulse width, the time from the falling edge of CAS to the rising edge of CAS.

Cautions on Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh can be used independently when used in combination with distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh; However, when used in combination with burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh or with burst long $\overline{\text{RAS}}$ only refresh, the following cautions must be observed.

When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh are used in combination, please perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh as follows just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

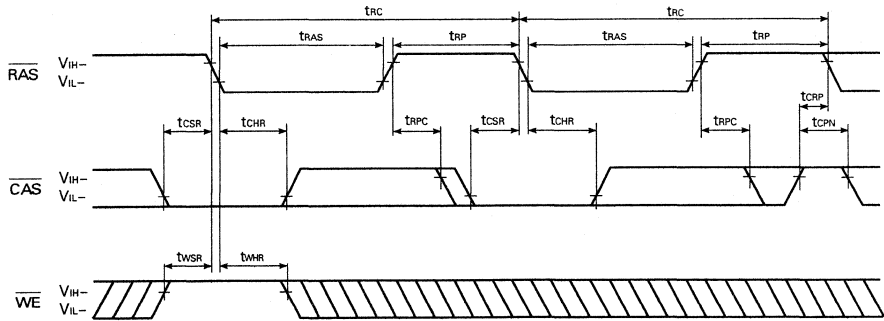
μ PD42S17400 : 2 048 times within a 32 ms interval

When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{RAS}}$ only refresh are used in combination, please perform $\overline{\text{RAS}}$ only refresh as follows just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

μ PD42S17400 : 2 048 times within a 32 ms interval

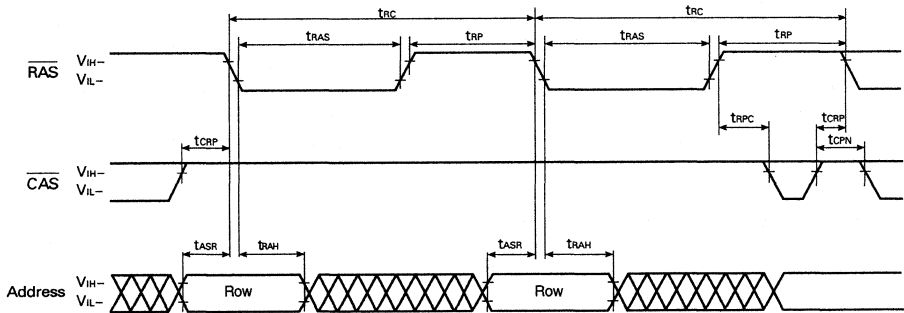
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



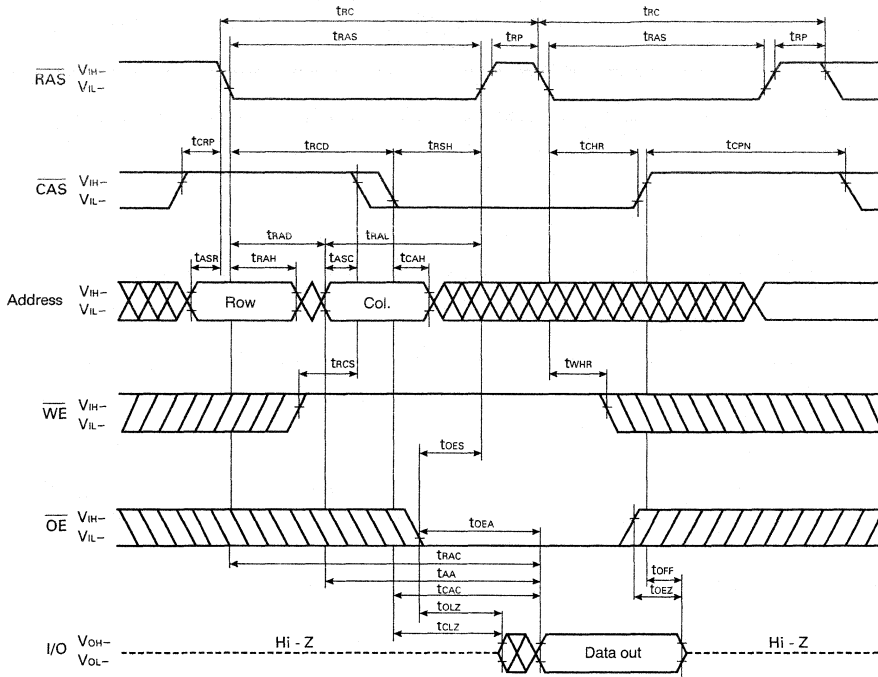
Remark Address, $\overline{OE}$: Don't care I/O : Hi - Z

RAS Only Refresh Cycle

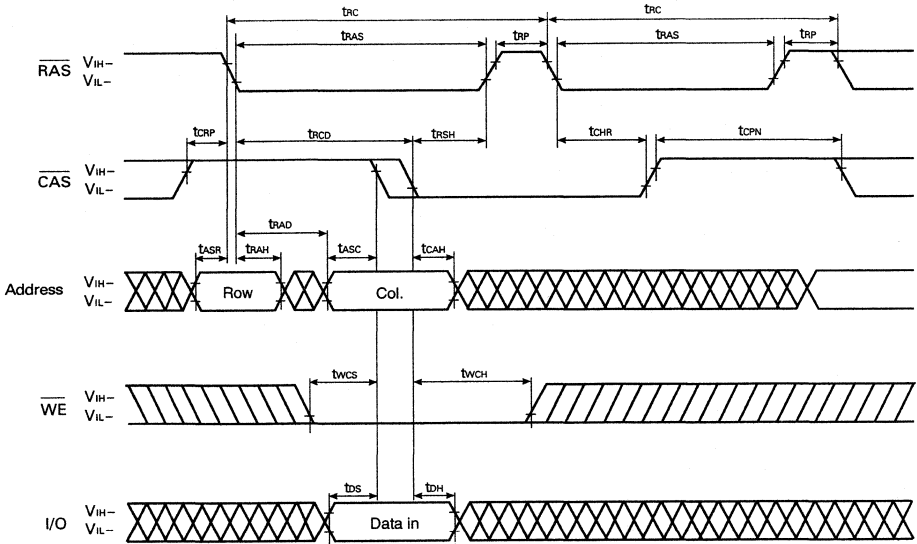


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi - Z

★

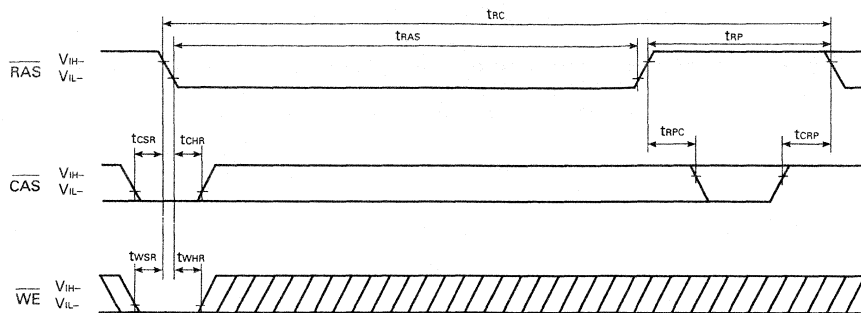


★ Hidden Refresh Cycle (Write)



Remark $\overline{\text{OE}}$: Don't care

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)



Remark Address, $\overline{\text{OE}}$: Don't care I/O : Hi - Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 16$ -bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1" : Normal write (all memory cells)

Output = "0" : Abnormal write

(3) Refresh

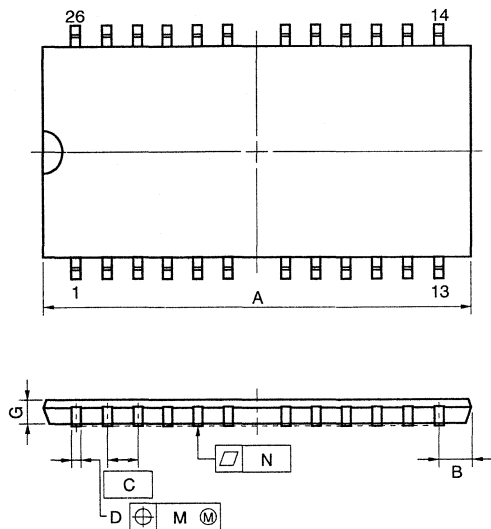
Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

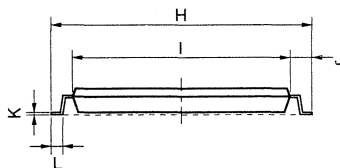
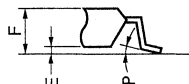
The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

★ Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



detail of lead end



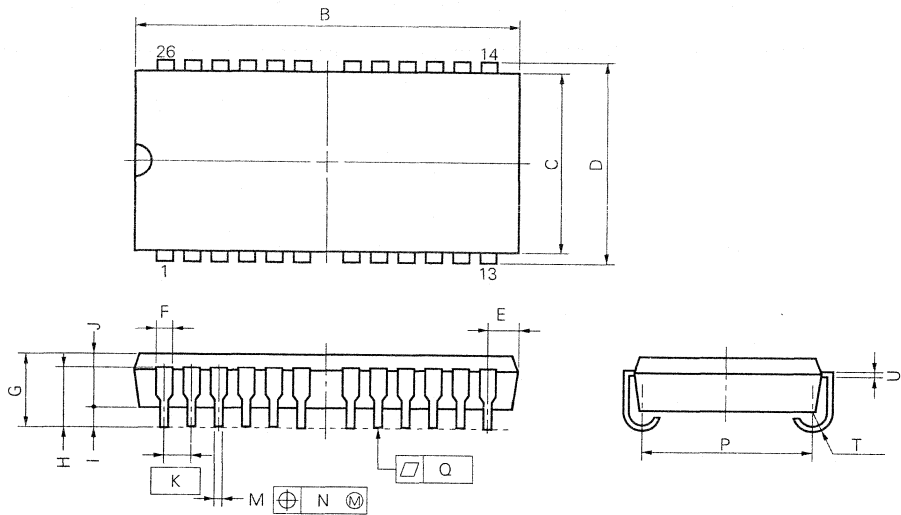
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.42 ^{+0.08} _{-0.07}	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004
P	3°+7° -3°	3°+7° -3°

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S26LA-300A

ITEM	MILLIMETERS	INCHES
B	17.1 ^{+0.25} _{-0.05}	0.673 ^{+0.010} _{-0.002}
C	7.62	0.300
D	8.47±0.2	0.333 ^{+0.009} _{-0.008}
E	1.03±0.15	0.041 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

★ Recommended Soldering Conditions

The following conditions (see table below) must be met for soldering conditions of the μPD42S16400, 4216400, 42S17400, 4217400.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16400G3, 4216400G3, 42S17400G3, 4217400G3 : 26-pin plastic TSOP (II) (300 mil)

Please consult with our sales offices.

μPD42S16400LA, 4216400LA, 42S17400LA, 4217400LA : 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions : 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

16 M-BIT DYNAMIC RAM 4 M-WORD BY 4-BIT, HYPER PAGE MODE

DESCRIPTION

The μ PD4216405 is a 4 194 304 words by 4 bits dynamic CMOS RAM with optional hyper page mode.

Hyper page mode is a kind of the page mode and is useful for the read operation.

The μ PD4216405 is packed in 26-pin plastic TSOP(III) and 26-pin plastic SOJ.

FEATURES

- Hyper page mode
- 4 194 304 words by 4 bits organization
- Single +5.0 V $\pm$ 10 % power supply
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 4 096 refresh cycles/64 ms

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μ PD4216405-50	50 ns	84 ns	20 ns
μ PD4216405-60	60 ns	104 ns	25 ns
μ PD4216405-70	70 ns	124 ns	30 ns

ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μ PD4216405G3-50-7JD	50 ns	26-pin Plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4216405G3-60-7JD	60 ns		
μ PD4216405G3-70-7JD	70 ns		
μPD4216405G3-50-7KD	50 ns	26-pin Plastic TSOP (II)	
μPD4216405G3-60-7KD	60 ns	(300 mil)	
μPD4216405G3-70-7KD	70 ns	Reverse bent	
μ PD4216405LA-50	50 ns	26-pin Plastic SOJ (300 mil)	
μ PD4216405LA-60	60 ns		
μ PD4216405LA-70	70 ns		

QUALITY GRADE

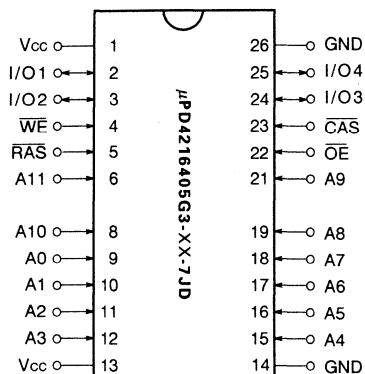
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

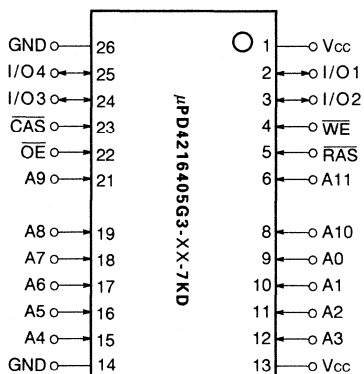
The information in this document is subject to change without notice.

PIN CONFIGURATIONS (Marking Side)

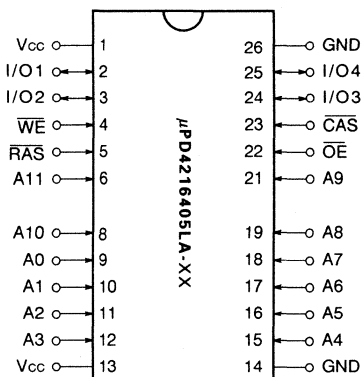
26-pin Plastic TSOP (II) (300 mil)



Reverse bent

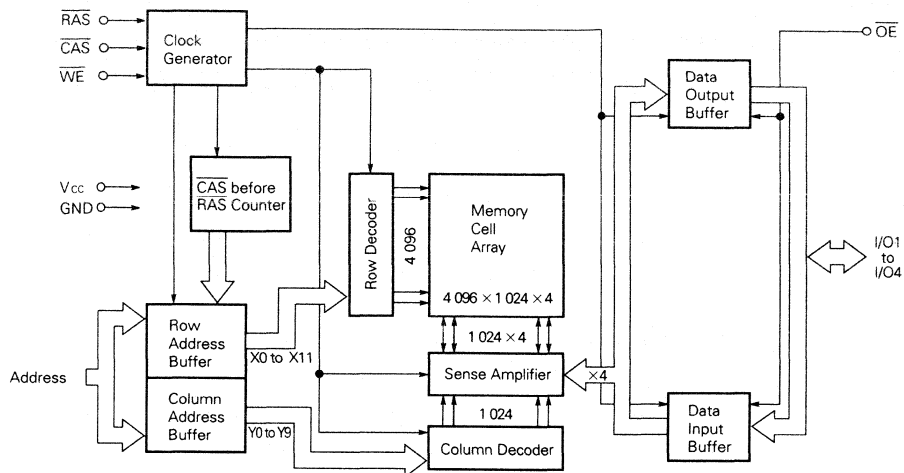


26-pin Plastic SOJ (300 mil)



- A0 to A11 : Address Inputs
- I/O1 to I/O4 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Supply Voltage
- GND : Ground

BLOCK DIAGRAM



INPUT/OUTPUT PIN FUNCTIONS

The μ PD4216405 has input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11 and input/output pins I/O1 to I/O4.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address input)		Address bus. Input total 22-bit of address signal, upper 12-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 4 194 304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data input/output)	Input/ Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

ELECTRICAL SPECIFICATIONS Notes1, 2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC}+1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

CAPACITANCE ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A11			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1 to I/O4			7	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling				
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 50 ns	100	mA	3,4,7
		I _O = 0 mA	t _{RAC} = 60 ns	90		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH}$ (MIN.)	I _O = 0 mA	2	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC}-0.2$ V	I _O = 0 mA	1		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling	t _{RAC} = 50 ns	100	mA	3,4,5,7
		$\overline{\text{CAS}} \geq V_{IH}$ (MIN.)	t _{RAC} = 60 ns	90		
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 70 ns	80		
Operating current (Hyper page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{IL}$ (MAX.)	t _{RAC} = 50 ns	100	mA	3,4,6
		$\overline{\text{CAS}}$ Cycling	t _{RAC} = 60 ns	90		
		t _{HPC} = t _{HPC} (MIN.)	t _{RAC} = 70 ns	80		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling	t _{RAC} = 50 ns	100	mA	3,4
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 60 ns	90		
		I _O = 0 mA	t _{RAC} = 70 ns	80		
Input leakage current	I _{I(L)}	V _I = 0 to 5.5 V all other pins not under test = 0 V	-10	+10	μ A	
Output leakage current	I _{O(L)}	V _O = 0 to 5.5 V Output is disabled (Hi-Z)	-10	+10	μ A	
High level output voltage	V _{OH}	I _O = -5.0 mA	2.4		V	
Low level output voltage	V _{OL}	I _O = +4.2 mA		0.4	V	

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted) Notes 8, 9 (1/2)

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{RC}	84		104		124		ns	
Read Modify Write Cycle Time	t _{RWC}	107		133		157		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		50		60		70	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		13		15		18	ns	10, 11
Access Time from Column Address	t _{AA}		25		30		35	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		27		35		40	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEA}		13		15		18	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	9	25	12	30	12	35	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0		0		0		ns	11
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	10		13		15		ns	
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OEZ}	0	10	0	13	0	15	ns	12, 18
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0		0		0		ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t _T	1	50	1	50	1	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30		40		50		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10 000	60	10 000	70	10 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	7		10		12		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	7	10 000	10	10 000	12	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	35		40		50		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	11	37	14	45	14	52	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	7		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	27		35		40		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	7		10		10		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	7		10		12		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	25		30		35		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	7		10		10		ns	15
$\overline{\text{WE}}$ Pulse Width	t _{WP}	7		10		10		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	7		10		10		ns	16
$\overline{\text{WE}}$ Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	27		32		37		ns	17
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	64		77		89		ns	17
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	39		47		54		ns	17

(2/2)

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t _{RWL}	7		10		12		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t _{CWL}	7		10		12		ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t _{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t _{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t _{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		64		64		64	ms	

HYPER PAGE MODE

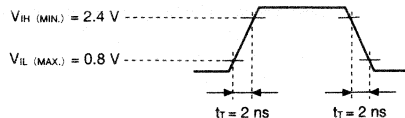
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{HPC}	20		25		30		ns	
$\overline{RAS}$ Pulse Width	t _{RASP}	50	125 000	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t _{HCAS}	7	10 000	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t _{CP}	7		10		10		ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t _{CPWD}	41		52		59		ns	17
Read Modify Write Cycle Time	t _{HPRWC}	52		66		75		ns	
Data Output Hold Time	t _{DHC}	5		5		5		ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t _{WEZ}	0	10	0	13	0	15	ns	12, 18
$\overline{WE}$ Pulse Width	t _{WPZ}	7		10		10		ns	18
Output Buffer Turn-off Delay from $\overline{RAS}$	t _{OFR}	0	10	0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from $\overline{CAS}$	t _{OFc}	0	10	0	13	0	15	ns	12, 18

Notes 1. All voltages are referenced to GND.

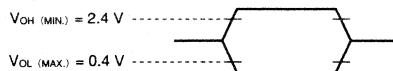
2. After power up, wait more than 100 μ s and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RAC} and t_{HPC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.

- Notes**
8. AC measurements assume $t_r = 2$ ns.
 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD} (MAX.)$, $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{RAC} (MAX.)$	$t_{RAC} (MAX.)$
$t_{RAD} > t_{RAD} (MAX.)$, $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{AA} (MAX.)$	$t_{RAD} + t_{AA} (MAX.)$
$t_{RCD} > t_{RCD} (MAX.)$	$t_{CAC} (MAX.)$	$t_{RCD} + t_{CAC} (MAX.)$

$t_{RAD} (MAX.)$ and $t_{RCD} (MAX.)$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD} (MAX.)$ and $t_{RCD} \geq t_{RCD} (MAX.)$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFC} (MAX.)$, $t_{OFR} (MAX.)$, $t_{WEZ} (MAX.)$ and $t_{OEZ} (MAX.)$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .
13. $t_{CRP} (MIN.)$ requirement is applied for $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycles.
14. Either $t_{RCH} (MIN.)$ or $t_{RRH} (MIN.)$ should be met in read cycles.
15. $t_{WP} (MIN.)$ is applied for late write cycles or read modify write cycles. In early write cycles, $t_{WCH} (MIN.)$ should be met.
16. $t_{DS} (MIN.)$ and $t_{DH} (MIN.)$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS} (MIN.)$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD} (MIN.)$, $t_{CWD} \geq t_{CWD} (MIN.)$, $t_{AWD} \geq t_{AWD} (MIN.)$ and $t_{CPWD} \geq t_{CPWD} (MIN.)$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
18. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

- (1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)

$\overline{WE}$: inactive, $\overline{OE}$: active

t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

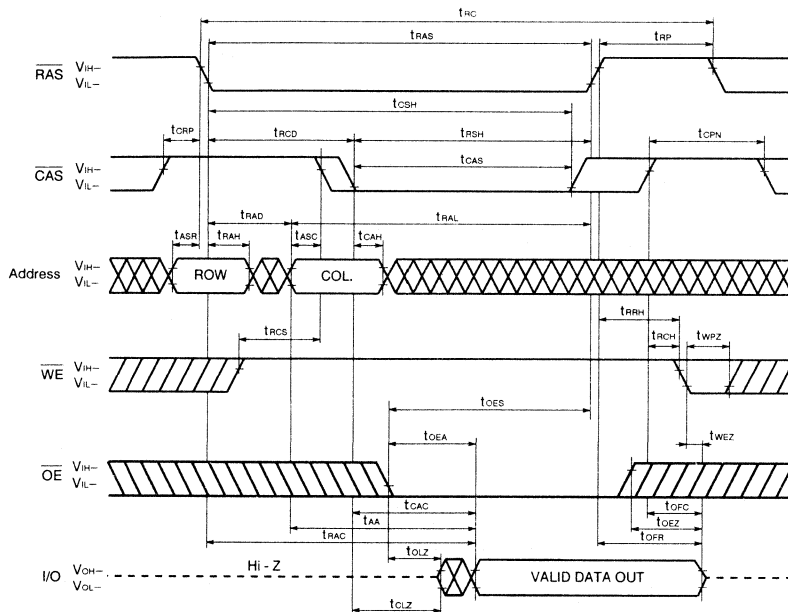
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

- (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)

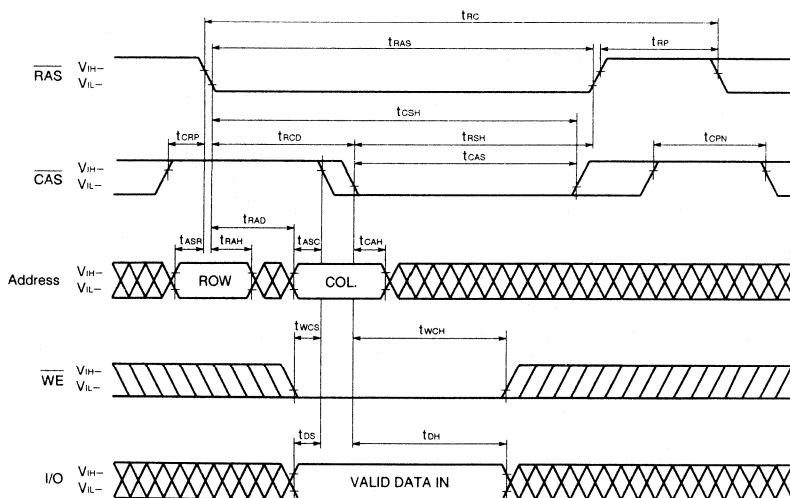
$\overline{WE}$: active, $\overline{OE}$: active... t_{WEZ} , t_{WPZ} are effective.

$\overline{WE}$: inactive, $\overline{OE}$: inactive... t_{OEZ} is effective.

READ CYCLE

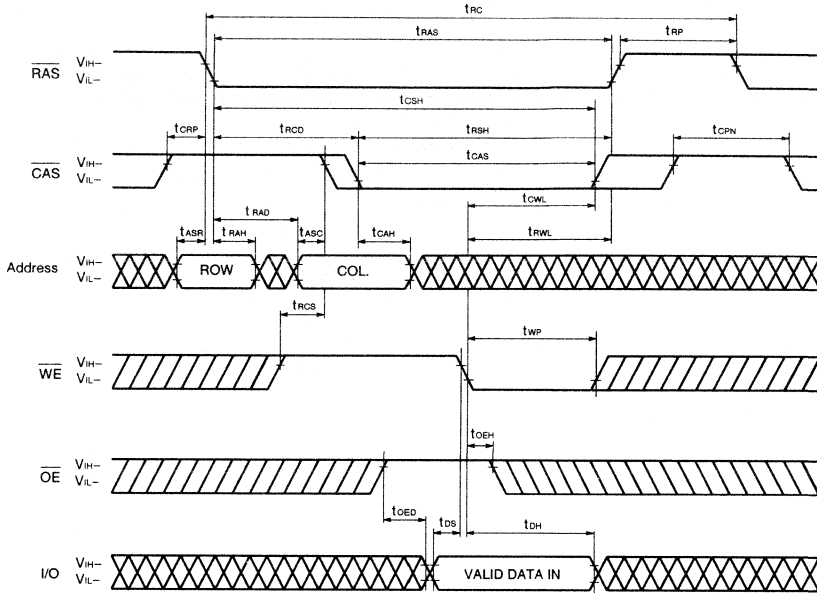


EARLY WRITE CYCLE

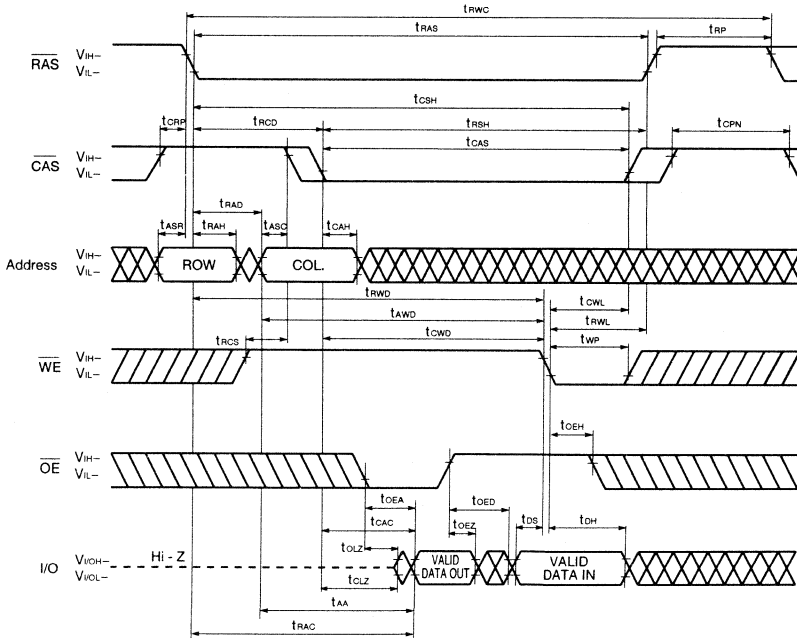


Remark $\overline{OE} = \text{Don't Care}$

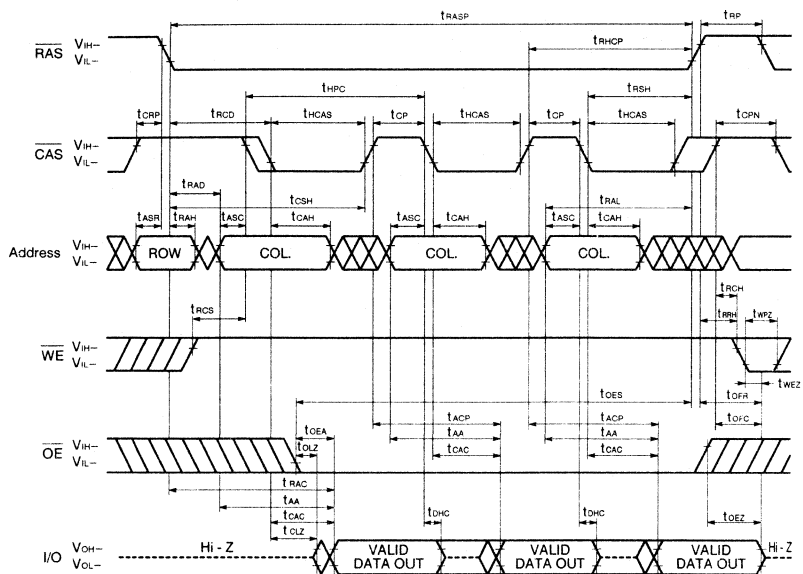
LATE WRITE CYCLE



READ MODIFY WRITE CYCLE



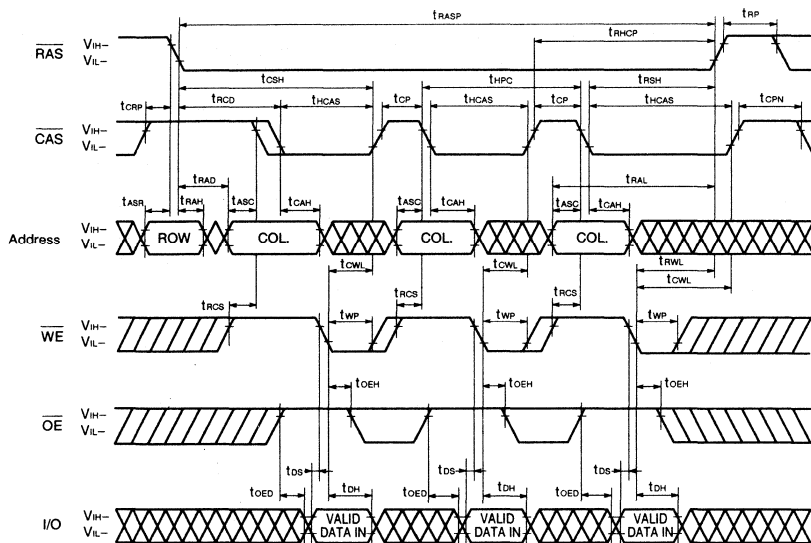
HYPER PAGE MODE READ CYCLE



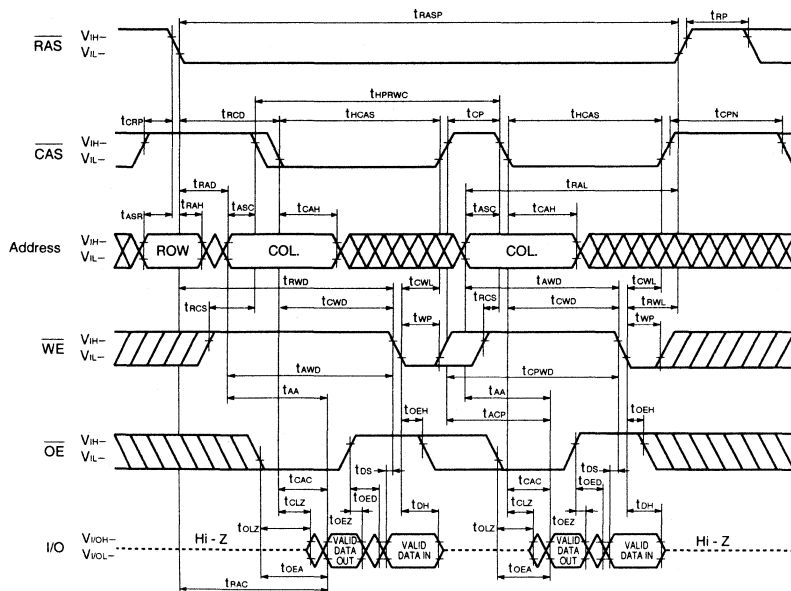
[illegible]

Remark $\overline{OE} = \text{Don't Care}$

HYPER PAGE MODE LATE WRITE CYCLE

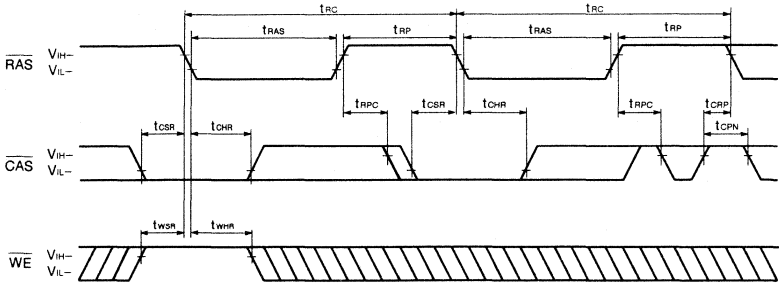


HYPER PAGE MODE READ MODIFY WRITE CYCLE



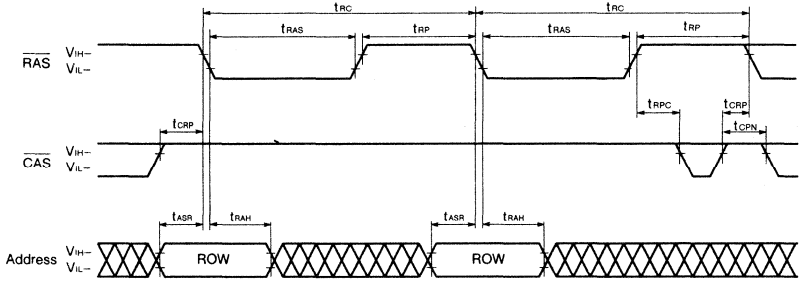
[illegible]

CAS BEFORE RAS REFRESH CYCLE



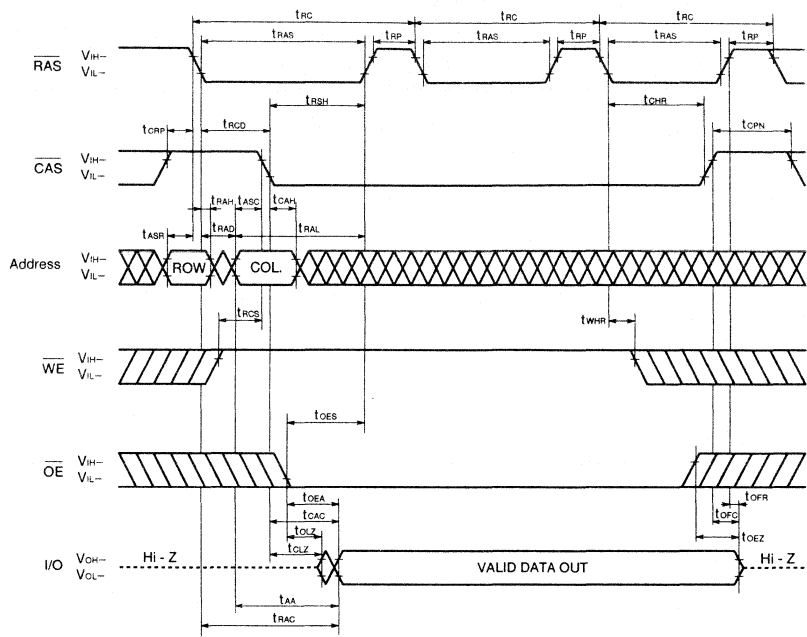
Remark Address, $\overline{OE}$ = Don't care I/O = Hi - Z

RAS ONLY REFRESH CYCLE

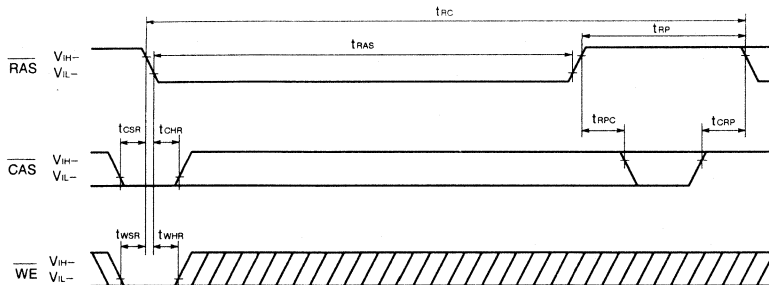


Remark $\overline{WE}$, $\overline{OE}$ = Don't care I/O = Hi - Z

HIDDEN REFRESH CYCLE



TEST MODE SET CYCLE ($\overline{WE}$, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE)



Remark Address, $\overline{OE}$ = Don't care I/O = Hi - Z

TEST MODE

TEST MODE is fast test function. On using this mode, test time is reduced to 1/4. In this TEST MODE, internal organization is 1 M words by 16 bits apparently. Don't care about the input levels of the column address input A0, A1.

1. How to enter TEST MODE

Through TEST MODE SET CYCLE ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle), the device enters TEST MODE.

2. Write / Read in TEST MODE

Write data of "1" or "0" through I/O1 to I/O4 by controlling address except for above-mentioned address. Each input data through each I/O write 4 bits at once. And read through I/O1 to I/O4 to check written data. In case of writing each 4 bits rightly, each I/O data is "1". But wrong, the data is "0".

3. Refresh in TEST MODE

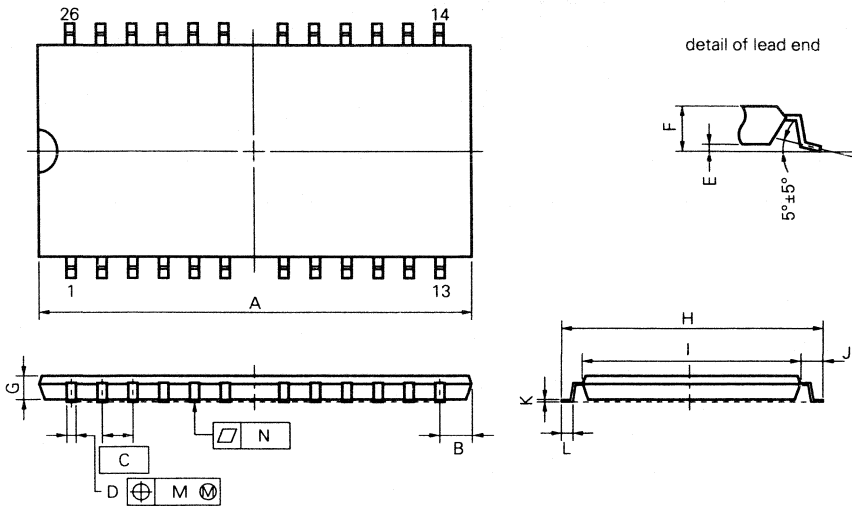
Use normal read cycle or $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

4. How to exit from TEST MODE

Through RAS only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, the device exits from TEST MODE.

PACKAGE DRAWINGS

26 PIN PLASTIC TSOP(III) (300 mil)



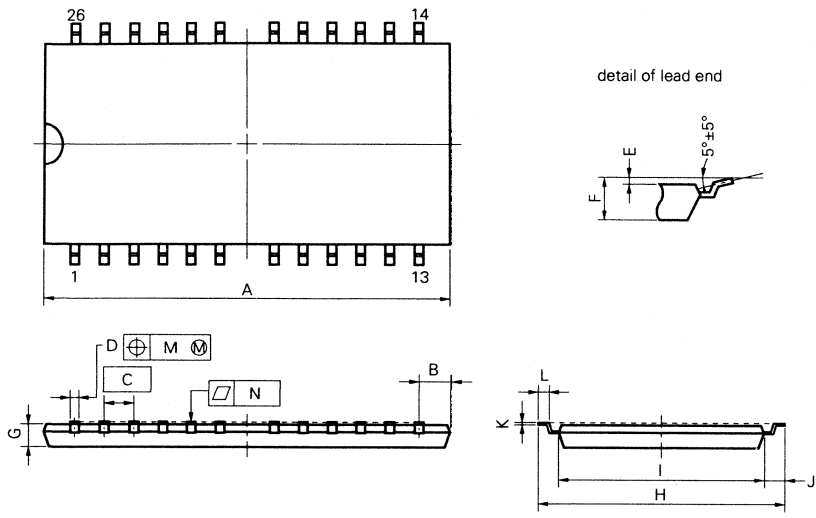
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S26G3-50-7JD-1

ITEM	MILLIMETERS	INCHES
A	17.40 MAX.	0.685 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

26 PIN PLASTIC TSOP(III) (300 mil)



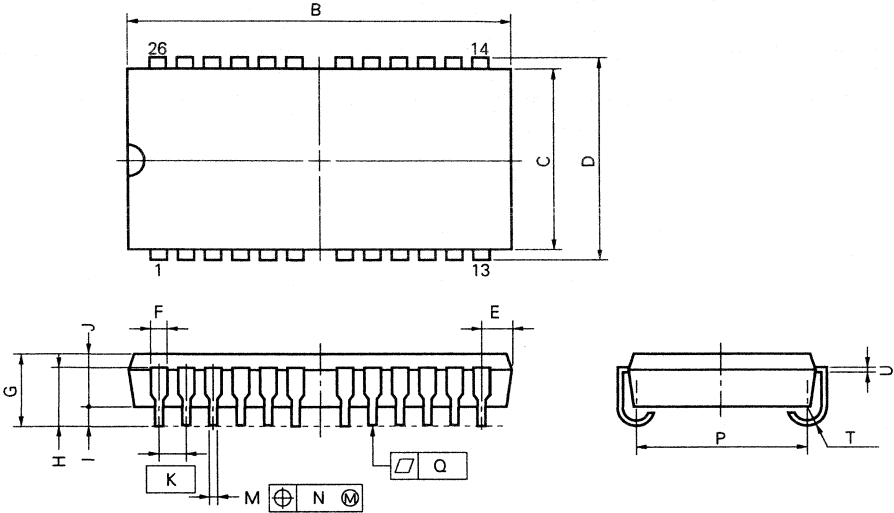
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S26G3-50-7KD-1

ITEM	MILLIMETERS	INCHES
A	17.40 MAX.	0.685 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S26LA-300A

ITEM	MILLIMETERS	INCHES
B	17.1 ^{+0.25} _{-0.05}	0.673 ^{+0.010} _{-0.002}
C	7.62	0.300
D	8.47±0.2	0.333 ^{+0.009} _{-0.008}
E	1.03±0.15	0.041 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μPD4216405.

TYPE OF SURFACE MOUNT DEVICE

μPD4216405G3 : 26-pin Plastic TSOP (II) (300 mil)

μPD4216405LA : 26-pin Plastic SOJ (300 mil)

MOS INTEGRATED CIRCUIT

μ PD42S16800, 4216800, 42S17800, 4217800

16 M-BIT DYNAMIC RAM

2 M-WORD BY 8-BIT, FAST PAGE MODE

Description

The μ PD42S16800, 4216800, 42S17800, 4217800 are 2 097 152 words by 8 bits dynamic CMOS RAMs.

These differ in refresh cycle and the μ PD42S16800, 42S17800 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

These are packed in 28-pin plastic TSOP (II) and 28-pin plastic SOJ.

Features

- 2 097 152 words by 8 bits organization
- Single +5.0 V $\pm$ 10 % power supply
- Fast page mode
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S16800-50, 4216800-50	550 mW	50 ns	90 ns	35 ns
μ PD42S17800-50, 4217800-50	660 mW			
μ PD42S16800-60, 4216800-60	495 mW	60 ns	110 ns	40 ns
μ PD42S17800-60, 4217800-60	605 mW			
μ PD42S16800-70, 4216800-70	440 mW	70 ns	130 ns	45 ns
μ PD42S17800-70, 4217800-70	550 mW			
μ PD42S16800-80, 4216800-80	385 mW	80 ns	150 ns	50 ns
μ PD42S17800-80, 4217800-80	495 mW			

- The μ PD42S16800, 42S17800 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S16800	4 096 cycles / 128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μ PD42S17800	2 048 cycles / 128 ms		
μ PD4216800	4 096 cycles / 64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)
μ PD4217800	2 048 cycles / 32 ms		

The information in this document is subject to change without notice.

★ Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD42S16800G5-50-7JD	50 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S17800G5-50-7JD			
μ PD42S16800G5-60-7JD	60 ns		
μ PD42S17800G5-60-7JD			
μ PD42S16800G5-70-7JD	70 ns		
μ PD42S17800G5-70-7JD			
μ PD42S16800G5-80-7JD	80 ns		
μ PD42S17800G5-80-7JD			
μ PD42S16800LE-50	50 ns	28-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S17800LE-50			
μ PD42S16800LE-60	60 ns		
μ PD42S17800LE-60			
μ PD42S16800LE-70	70 ns		
μ PD42S17800LE-70			
μ PD42S16800LE-80	80 ns		
μ PD42S17800LE-80			
μ PD4216800G5-50-7JD	50 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4217800G5-50-7JD			
μ PD4216800G5-60-7JD	60 ns		
μ PD4217800G5-60-7JD			
μ PD4216800G5-70-7JD	70 ns		
μ PD4217800G5-70-7JD			
μ PD4216800G5-80-7JD	80 ns		
μ PD4217800G5-80-7JD			
μ PD4216800LE-50	50 ns	28-pin Plastic SOJ (400 mil)	
μ PD4217800LE-50			
μ PD4216800LE-60	60 ns		
μ PD4217800LE-60			
μ PD4216800LE-70	70 ns		
μ PD4217800LE-70			
μ PD4216800LE-80	80 ns		
μ PD4217800LE-80			

Quality Grade

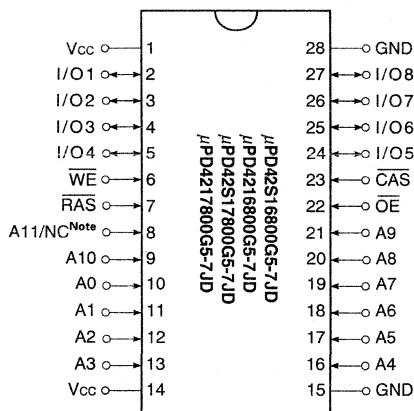
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

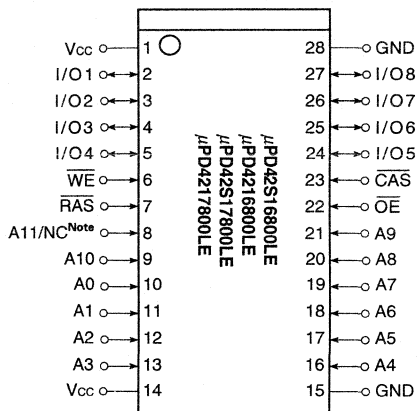
Pin Configurations (Marking Side)



28-pin Plastic TSOP (III)



28-pin Plastic SOJ



Note A11 ...μPD42S16800, 4216800
NC ...μPD42S17800, 4217800

- A0 to A11 : Address inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row address strobe
- CAS : Column address strobe
- WE : Write enable
- OE : Output enable
- Vcc : Power Supply
- GND : Ground
- NC : No connection

Input/Output Pin Functions

The μPD42S16800, 4216800, 42S17800, 4217800 have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11/A10 ^{Note1} and input/output pins I/O1 to I/O8.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11/A10 ^{Note1} (Address inputs)		Address bus. Input total 21-bit of address signal, upper 12/11 ^{Note2} -bit and lower 9/10 ^{Note2} -bit in sequence (address multiplex method). Therefore, one word is selected from 2 097 152-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t _{ASR} , t _{ASC}) and hold time (t _{RAH} , t _{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/ Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

- Notes**
- | | |
|---------------------------------|------------------------------|
| 1. A11 ... μPD42S16800, 4216800 | A10 ... μPD42S17800, 4217800 |
| 2. 12 ... μPD42S16800, 4216800 | 11 ... μPD42S17800, 4217800 |
| 3. 9 ... μPD42S16800, 4216800 | 10 ... μPD42S17800, 4217800 |

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[μ PD42S16800, 4216800]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	RAS, CAS Cycling trC = trC(MIN.) Io = 0 mA	trAC = 50 ns		100	mA	1,2,3
				trAC = 60 ns		90		
				trAC = 70 ns		80		
				trAC = 80 ns		70		
Standby current	μPD42S16800	I _{CC2}	RAS, CAS ≥ VIH (MIN.)	Io = 0 mA		2	mA	
	μPD4216800		RAS, CAS ≥ VCC - 0.2 V	Io = 0 mA		0.25		
			RAS, CAS ≥ VIH (MIN.)	Io = 0 mA		2		
			RAS, CAS ≥ VCC - 0.2 V	Io = 0 mA		1		
RAS only refresh current		I _{CC3}	RAS Cycling CAS ≥ VIH (MIN.) trC = trC (MIN.) Io = 0 mA	trAC = 50 ns		100	mA	1,2,3,4
				trAC = 60 ns		90		
				trAC = 70 ns		80		
				trAC = 80 ns		70		
Operating current (Fast page mode)		I _{CC4}	RAS ≤ VIL (MAX.) CAS Cycling trC = trC (MIN.) Io = 0 mA	trAC = 50 ns		80	mA	1,2,5
				trAC = 60 ns		70		
				trAC = 70 ns		60		
				trAC = 80 ns		50		
CAS before RAS refresh current		I _{CC5}	RAS Cycling trC = trC (MIN.) Io = 0 mA	trAC = 50 ns		100	mA	1,2
				trAC = 60 ns		90		
				trAC = 70 ns		80		
				trAC = 80 ns		70		
CAS before RAS long refresh current (4 096 cycles / 128 ms, only for μPD42S16800)		I _{CC6}	CAS before RAS refresh : 4 096 cycles/128 ms RAS, CAS : 0 V ≤ VIL ≤ 0.2 V VCC-0.2 V ≤ VIH ≤ VIH(MAX.) Standby : RAS ≥ VCC-0.2 V Address : Don't care WE, OE : VIH Io = 0 mA	trAS ≤ 300 ns		450	μA	1,2
				trAS ≤ 1 μs		600		
Self refresh current (CAS before RAS self refresh, only for μPD42S16800)		I _{CC7}	RAS, CAS : 0 V ≤ VIL ≤ 0.2 V VCC-0.2 V ≤ VIH ≤ VIH (MAX.) Io = 0 mA			250	μA	2
Input leakage current		II (L)	VI = 0 to 5.5 V all other pins not under test = 0 V		-10	+10	μA	
Output leakage current		IO (L)	VO = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μA	
High level output voltage		VOH	Io = -5.0 mA		2.4		V	
Low level output voltage		VOL	Io = +4.2 mA			0.4	V	

[μ PD42S17800, 4217800]

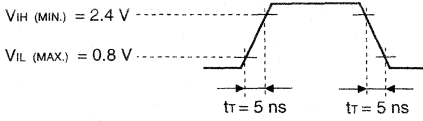
Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{Io} = 0 \text{ mA}$	$\text{trAC} = 50 \text{ ns}$		120	mA	1,2,3
				$\text{trAC} = 60 \text{ ns}$		110		
				$\text{trAC} = 70 \text{ ns}$		100		
				$\text{trAC} = 80 \text{ ns}$		90		
Standby current	$\mu\text{PD42S17800}$	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$\text{Io} = 0 \text{ mA}$		2	mA	
	$\mu\text{PD4217800}$		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$\text{Io} = 0 \text{ mA}$		0.25		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$\text{Io} = 0 \text{ mA}$		2		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$\text{Io} = 0 \text{ mA}$		1		
$\overline{\text{RAS}}$ only refresh current		I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.})$ $\text{Io} = 0 \text{ mA}$	$\text{trAC} = 50 \text{ ns}$		120	mA	1,2,3,4
				$\text{trAC} = 60 \text{ ns}$		110		
				$\text{trAC} = 70 \text{ ns}$		100		
				$\text{trAC} = 80 \text{ ns}$		90		
Operating current (Fast page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ $\overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.})$ $\text{Io} = 0 \text{ mA}$	$\text{trAC} = 50 \text{ ns}$		80	mA	1,2,5
				$\text{trAC} = 60 \text{ ns}$		70		
				$\text{trAC} = 70 \text{ ns}$		60		
				$\text{trAC} = 80 \text{ ns}$		50		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{Io} = 0 \text{ mA}$	$\text{trAC} = 50 \text{ ns}$		120	mA	1,2
				$\text{trAC} = 60 \text{ ns}$		110		
				$\text{trAC} = 70 \text{ ns}$		100		
				$\text{trAC} = 80 \text{ ns}$		90		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (2 048 cycles / 128 ms, only for $\mu\text{PD42S17800}$)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : 2 048 cycles/128 ms $\overline{\text{RAS}}, \overline{\text{CAS}} : 0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $V_{\text{CC}}-0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}(\text{MAX.})}$ Standby : $\overline{\text{RAS}} \geq V_{\text{CC}}-0.2 \text{ V}$ Address : Don't care $\overline{\text{WE}}, \overline{\text{OE}} : V_{\text{IH}}$ $\text{Io} = 0 \text{ mA}$	$\text{trAS} \leq 300 \text{ ns}$		400	μA	1,2
				$\text{trAS} \leq 1 \mu\text{s}$		500		
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for $\mu\text{PD42S17800}$)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}} : 0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $V_{\text{CC}}-0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $\text{Io} = 0 \text{ mA}$			250	μA	2
Input leakage current		I _{I (L)}	$V_{\text{I}} = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10		μA	
Output leakage current		I _{O (L)}	$V_{\text{O}} = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10		μA	
High level output voltage		V _{OH}	$\text{Io} = -5.0 \text{ mA}$		2.4		V	
Low level output voltage		V _{OL}	$\text{Io} = +4.2 \text{ mA}$			0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{TRC} and t_{TPC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during RAS $\leq V_{IL(MAX.)}$ and CAS $\geq V_{IH(MIN.)}$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

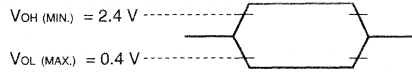
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	trac = 50 ns		trac = 60 ns		trac = 70 ns		trac = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		trc	90	–	110	–	130	–	150	–	ns	
RAS Precharge Time		trp	30	–	40	–	50	–	60	–	ns	
CAS Precharge Time		tcpn	8	–	10	–	10	–	10	–	ns	
RAS Pulse Width		tras	50	10 000	60	10 000	70	10 000	80	10 000	ns	
CAS Pulse Width		tcas	13	10 000	15	10 000	18	10 000	20	10 000	ns	
RAS Hold Time		trsh	13	–	15	–	18	–	20	–	ns	
CAS Hold Time		tcsH	50	–	60	–	70	–	80	–	ns	
RAS to CAS Delay Time		trcd	18	32	20	45	20	50	25	60	ns	1
RAS to Column Address Delay Time		trad	13	25	15	30	15	35	17	40	ns	1
CAS to RAS Precharge Time		tcrp	5	–	5	–	5	–	5	–	ns	2
Row Address Setup Time		tasr	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time		trah	8	–	10	–	10	–	12	–	ns	
Column Address Setup Time		tasc	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time		tcaH	13	–	15	–	15	–	15	–	ns	
OE Lead Time Referenced to RAS		toes	0	–	0	–	0	–	0	–	ns	
CAS to Data Setup Time		tclz	0	–	0	–	0	–	0	–	ns	
OE to Data Setup Time		tolz	0	–	0	–	0	–	0	–	ns	
OE to Data Delay Time		toed	10	–	13	–	15	–	15	–	ns	
Transition Time (Rise and Fall)		tt	3	50	3	50	3	50	3	50	ns	
Refresh Time	μPD42S16800, 42S17800	tREF	–	128	–	128	–	128	–	128	ms	3
	μPD4216800		–	64	–	64	–	64	–	64	ms	
	μPD4217800		–	32	–	32	–	32	–	32	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$\overline{\text{trAD}} \leq \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \leq \overline{\text{trCD}} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\overline{\text{trAD}} > \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \leq \overline{\text{trCD}} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$	$\text{trAD} + \text{tAA} (\text{MAX.})$
$\overline{\text{trCD}} > \overline{\text{trCD}} (\text{MAX.})$	$\text{tCAC} (\text{MAX.})$	$\text{trCD} + \text{tCAC} (\text{MAX.})$

$\overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} (\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\overline{\text{trAD}} \geq \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \geq \overline{\text{trCD}} (\text{MAX.})$ will not cause any operation problems.

2. $\text{trCP} (\text{MIN.})$ requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
3. This specification is applied only to the μPD42S16800, 42S17800.

Read Cycle

Parameter	Symbol	$\text{trAC} = 50 \text{ ns}$		$\text{trAC} = 60 \text{ ns}$		$\text{trAC} = 70 \text{ ns}$		$\text{trAC} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	trAC	–	50	–	60	–	70	–	80	ns	1
Access Time from $\overline{\text{CAS}}$	tCAC	–	13	–	15	–	18	–	20	ns	1
Access Time from Column Address	tAA	–	25	–	30	–	35	–	40	ns	1
Access Time from $\overline{\text{OE}}$	tOEA	–	13	–	15	–	18	–	20	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	trAL	25	–	30	–	35	–	40	–	ns	
Read Command Setup Time	trCS	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	trRH	0	–	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	trCH	0	–	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	tOEZ	0	10	0	13	0	15	0	15	ns	3
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	tOFF	0	10	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$\overline{\text{trAD}} \leq \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \leq \overline{\text{trCD}} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\overline{\text{trAD}} > \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \leq \overline{\text{trCD}} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$	$\text{trAD} + \text{tAA} (\text{MAX.})$
$\overline{\text{trCD}} > \overline{\text{trCD}} (\text{MAX.})$	$\text{tCAC} (\text{MAX.})$	$\text{trCD} + \text{tCAC} (\text{MAX.})$

$\overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} (\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\overline{\text{trAD}} \geq \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \geq \overline{\text{trCD}} (\text{MAX.})$ will not cause any operation problems.

2. Either $\text{trCH} (\text{MIN.})$ or $\text{trRH} (\text{MIN.})$ should be met in read cycles.
3. $\text{tOFF} (\text{MAX.})$ and $\text{tOEZ} (\text{MAX.})$ define the time when the output achieves the condition of Hi - Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
WE Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	8	–	10	–	10	–	15	–	ns	1
WE Pulse Width	t _{WP}	8	–	10	–	10	–	15	–	ns	1
WE Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	18	–	20	–	20	–	20	–	ns	
WE Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	13	–	15	–	15	–	15	–	ns	
WE Setup Time	t _{WCS}	0	–	0	–	0	–	0	–	ns	2
OE Hold Time	t _{OEH}	0	–	0	–	0	–	0	–	ns	
Data-in Setup Time	t _{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in Hold Time	t _{DH}	10	–	10	–	15	–	15	–	ns	3

- Notes**
1. t_{WP(MIN.)} is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH(MIN.)} should be met.
 2. If t_{WCS} $\geq$ t_{WCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle.
 3. t_{DS(MIN.)} and t_{DH(MIN.)} are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the WE falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t _{RWC}	140	–	160	–	180	–	200	–	ns	
$\overline{\text{RAS}}$ to WE Delay Time	t _{RWD}	70	–	83	–	95	–	105	–	ns	1
$\overline{\text{CAS}}$ to WE Delay Time	t _{CWD}	33	–	38	–	43	–	45	–	ns	1
Column Address to WE Delay Time	t _{AWD}	45	–	53	–	60	–	65	–	ns	1

- Note 1.** If t_{WCS} $\geq$ t_{WCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If t_{RWD} $\geq$ t_{RWD(MIN.)}, t_{CWD} $\geq$ t_{CWD(MIN.)}, t_{AWD} $\geq$ t_{AWD(MIN.)} and t_{CPWD} $\geq$ t_{CPWD(MIN.)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	35	–	40	–	45	–	50	–	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	–	30	–	35	–	40	–	45	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RASP}	50	125 000	60	125 000	70	125 000	80	125 000	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	8	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	–	35	–	40	–	45	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	80	–	85	–	90	–	100	–	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	50	–	58	–	65	–	70	–	ns	1

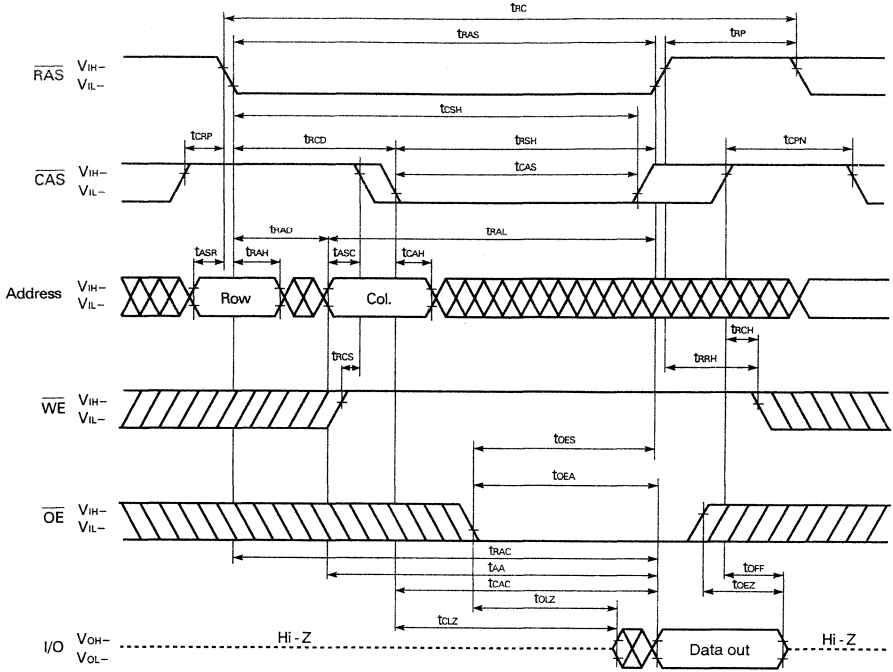
Note 1. If $\text{twcs} \geq \text{twcs}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $\text{trwd} \geq \text{trwd}(\text{MIN.})$, $\text{tcwd} \geq \text{tcwd}(\text{MIN.})$, $\text{tawd} \geq \text{tawd}(\text{MIN.})$ and $\text{tcpwd} \geq \text{tcpwd}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

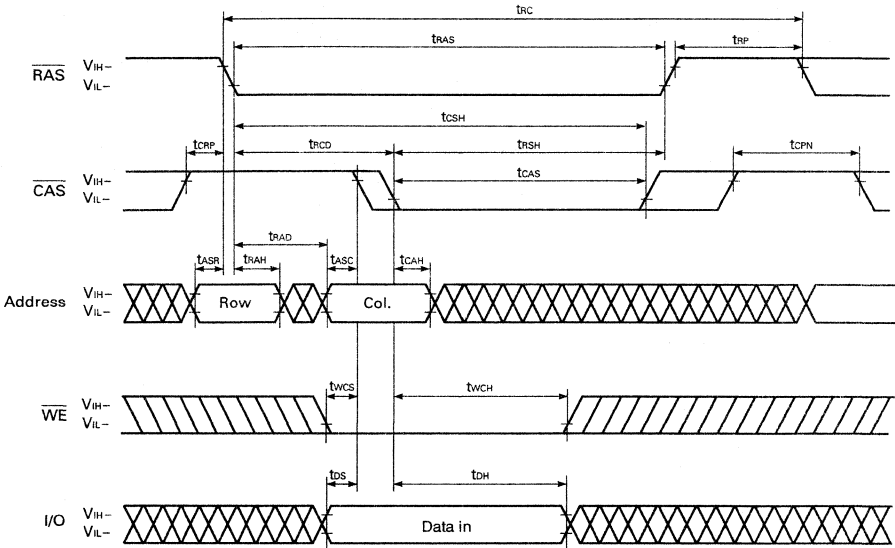
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ Setup Time	t _{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RASS}	100	–	100	–	100	–	100	–	μ s	1
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RPS}	90	–	110	–	130	–	150	–	ns	1
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15	–	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μ PD42S16800, 42S17800.

Read Cycle

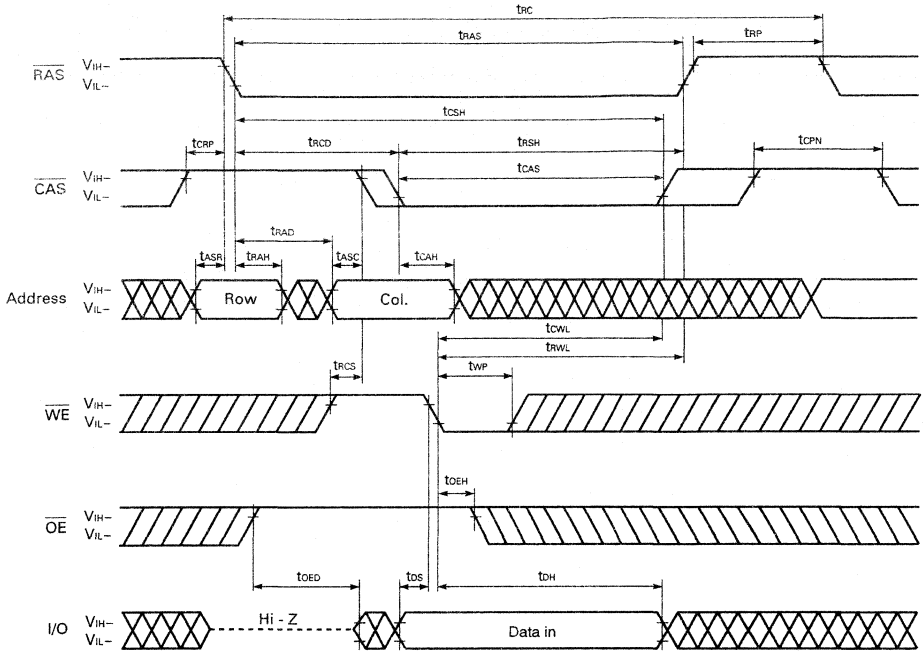


Early Write Cycle

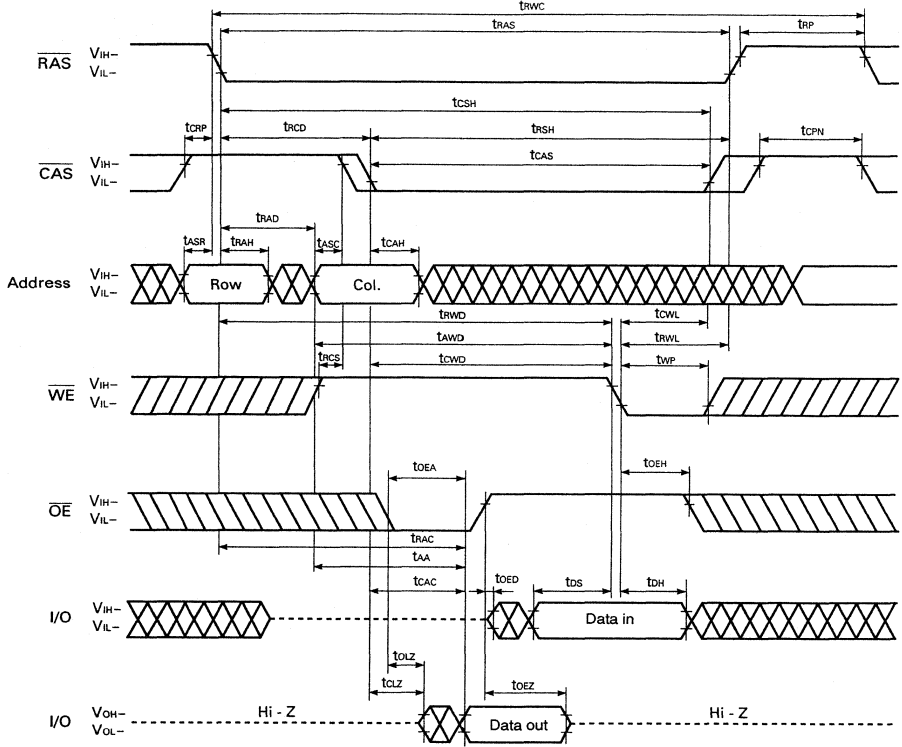


Remark $\overline{\text{OE}}$: Don't care

Late Write Cycle



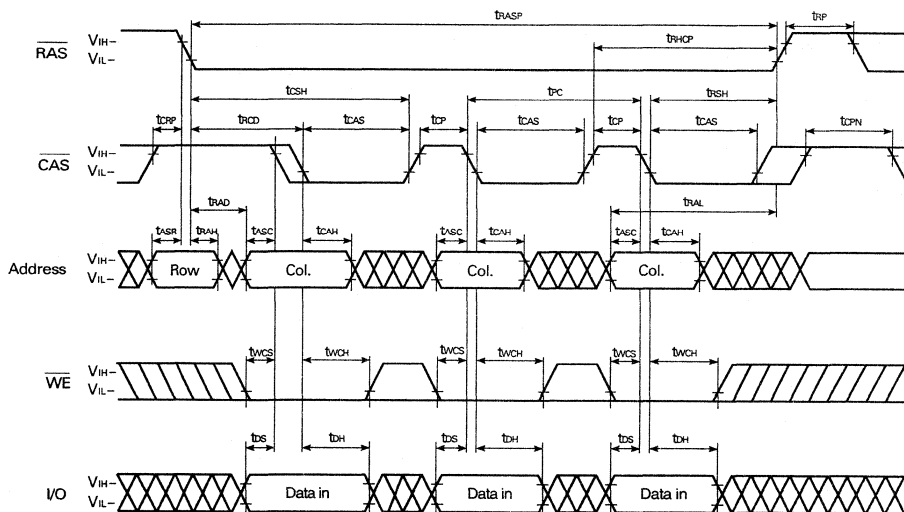
★ Read Modify Write Cycle



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Fast Page Mode Early Write Cycle



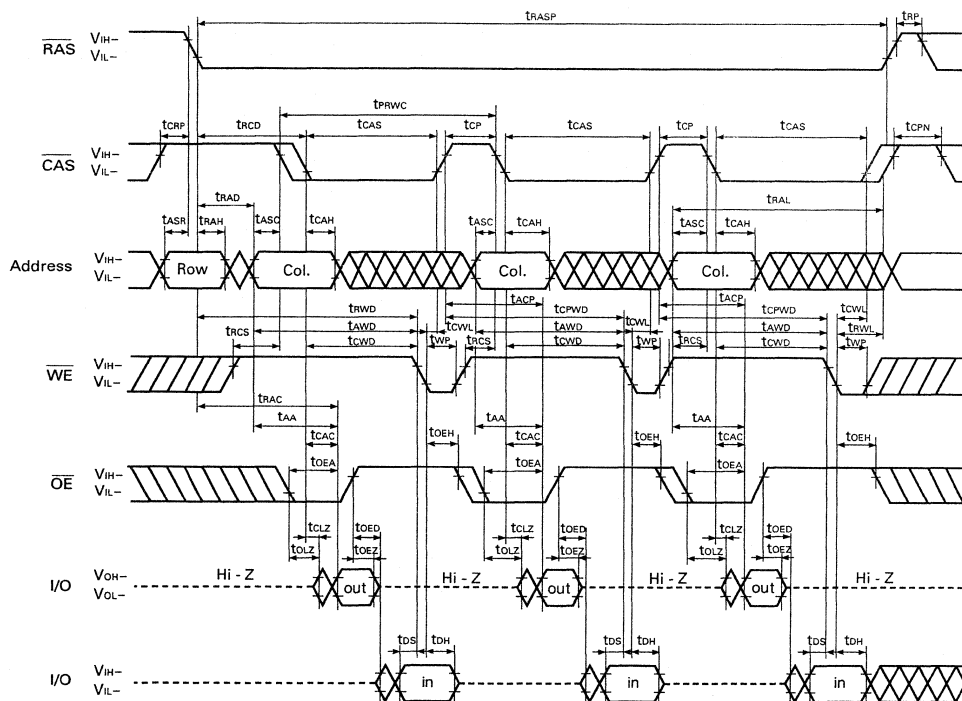
Remark $\overline{OE}$: Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

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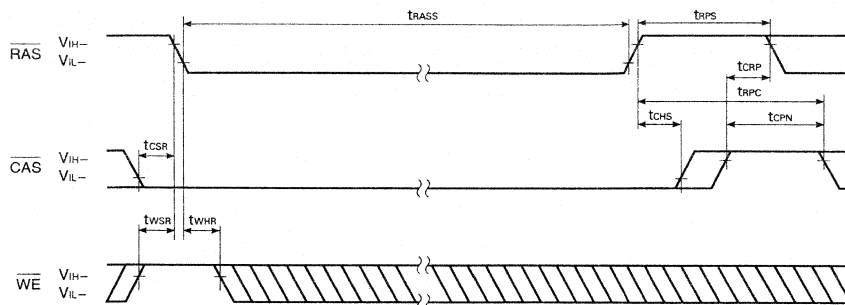
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★ **Fast Page Mode Read Modify Write Cycle**



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle (Only for the μ PD42S16800, 42S17800)



Remark Address, $\overline{OE}$: Don't care I/O : Hi - Z

Cautions on Use of CAS Before RAS Self Refresh



CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16800 : 4 096 times within a 64 ms interval

μ PD42S17800 : 2 048 times within a 32 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

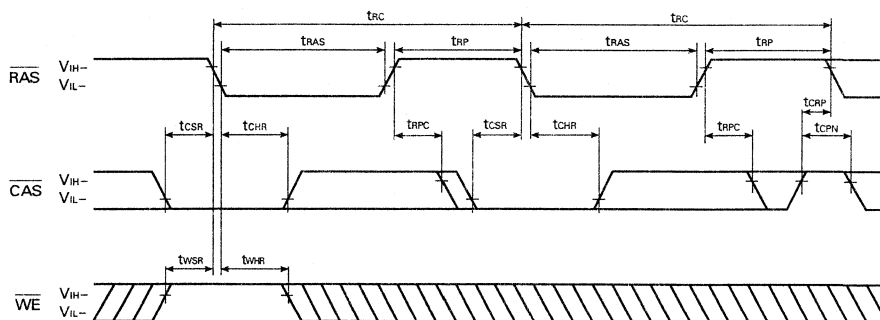
When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16800 : 4 096 times within a 64 ms interval

μ PD42S17800 : 2 048 times within a 32 ms interval

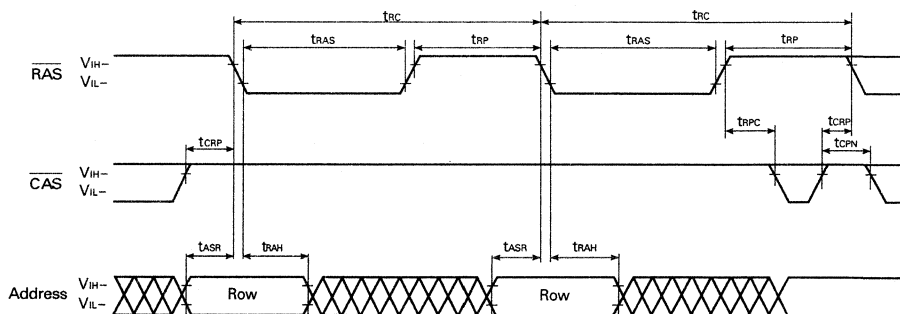
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



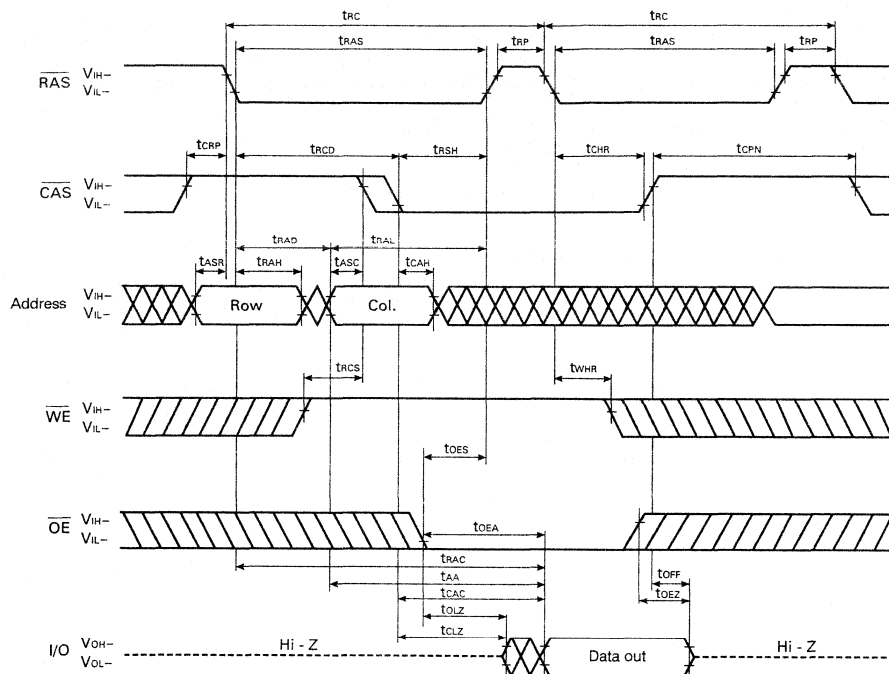
Remark Address, $\overline{\text{OE}}$: Don't care I/O : Hi - Z

RAS Only Refresh Cycle

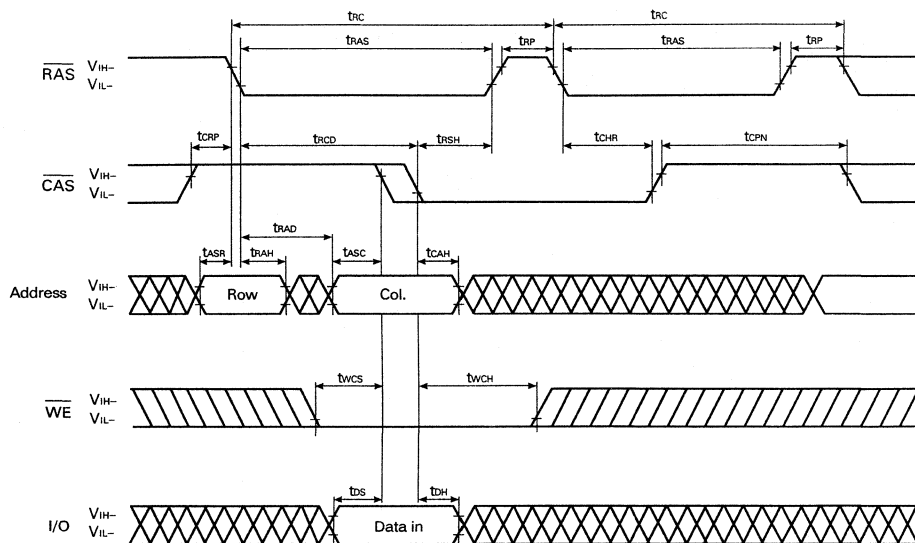


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O : Hi - Z

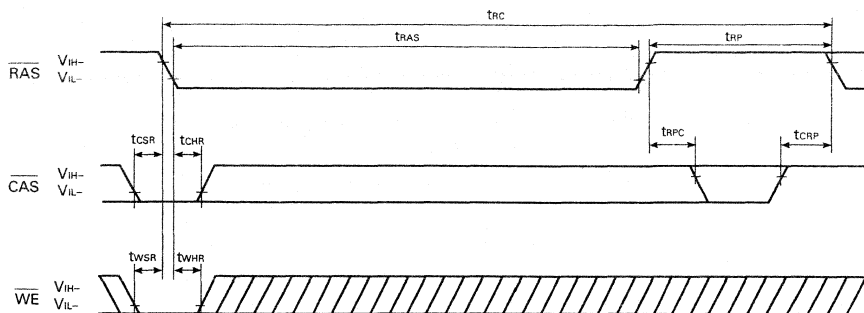
★



★ Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)

Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 16$ -bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1" : Normal write (all memory cells)

Output = "0" : Abnormal write

(3) Refresh

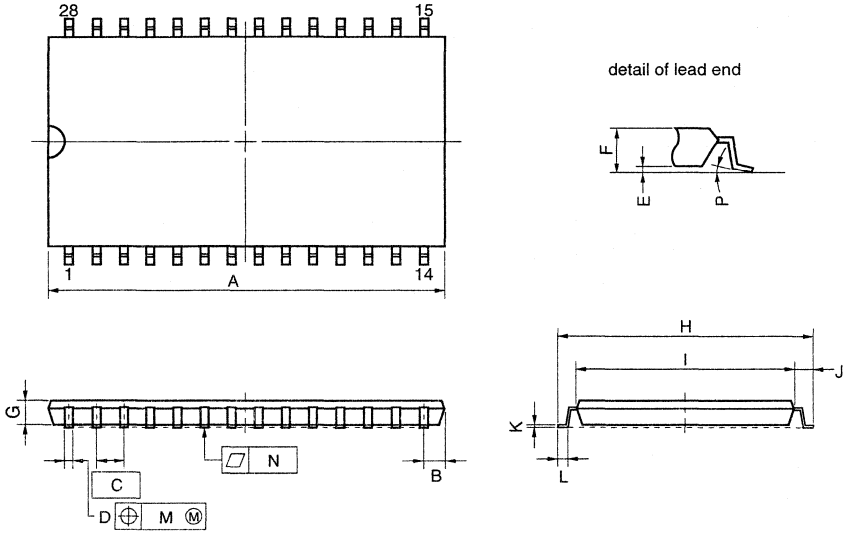
Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

★ Package Drawings

28 PIN PLASTIC TSOP (II) (400 mil)



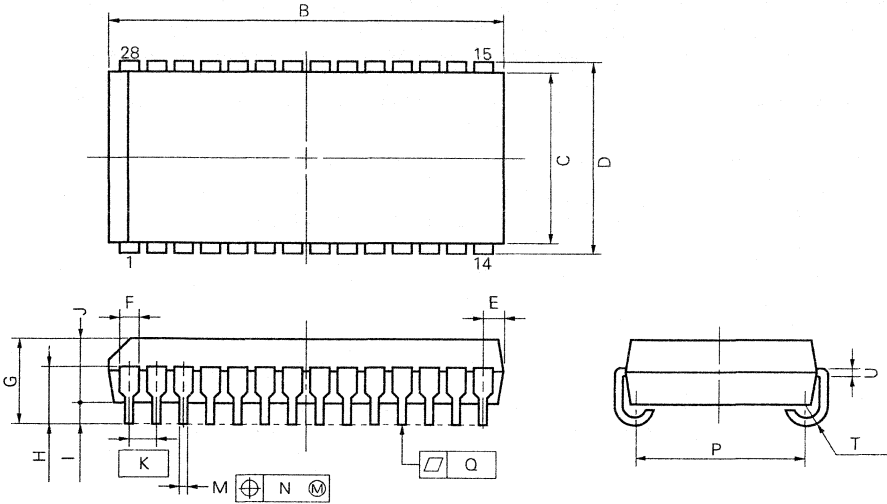
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.42 ^{+0.08} _{-0.07}	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S28G5-50-7JD3

28 PIN PLASTIC SOJ (400 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LE-400A1		
ITEM	MILLIMETERS	INCHES
B	18.67 ^{+0.2} _{-0.35}	0.735 ^{+0.008} _{-0.013}
C	10.16	0.400
D	11.18±0.2	0.440 ^{+0.008} _{-0.007}
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138 ^{+0.008} _{-0.007}
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.40±0.20	0.370 ^{+0.008} _{-0.007}
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

★ **Recommended Soldering Conditions**

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S16800, 4216800, 42S17800, 4217800.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16800G5, 4216800G5, 42S17800G5, 4217800G5 : 28-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-107-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S16800LE, 4216800LE, 42S17800LE, 4217800LE : 28-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

16 M-BIT DYNAMIC RAM

2 M-WORD BY 8-BIT, HYPER PAGE MODE

DESCRIPTION

The μ PD4216805 is a 2 097 152 words by 8 bits dynamic CMOS RAM with optional hyper page mode.

Hyper page mode is a kind of the page mode and is useful for the read operation.

The μ PD4216805 is packed in 28-pin plastic TSOP(II) and 28-pin plastic SOJ.

FEATURES

- Hyper page mode
- 2 097 152 words by 8 bits organization
- Single +5.0 V $\pm$ 10 % power supply
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 4 096 refresh cycles /64 ms

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μ PD4216805-50	50 ns	84 ns	20 ns
μ PD4216805-60	60 ns	104 ns	25 ns
μ PD4216805-70	70 ns	124 ns	30 ns

ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μ PD4216805G5-50-7JD	50 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4216805G5-60-7JD	60 ns		
μ PD4216805G5-70-7JD	70 ns		
μPD4216805G5-50-7KD	50 ns	28-pin Plastic TSOP (II) (400 mil)	
μPD4216805G5-60-7KD	60 ns	(400 mil)	
μPD4216805G5-70-7KD	70 ns	Reverse bent	
μ PD4216805LE-50	50 ns	28-pin Plastic SOJ (400 mil)	
μ PD4216805LE-60	60 ns		
μ PD4216805LE-70	70 ns		

QUALITY GRADE

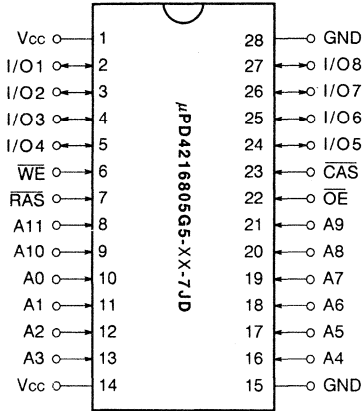
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

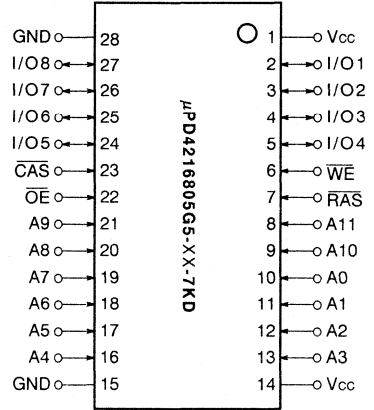
The information in this document is subject to change without notice.

PIN CONFIGURATIONS (Marking side)

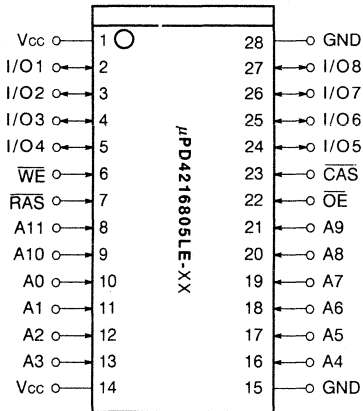
28-pin Plastic TSOP (II) (400 mil)



Reverse bent

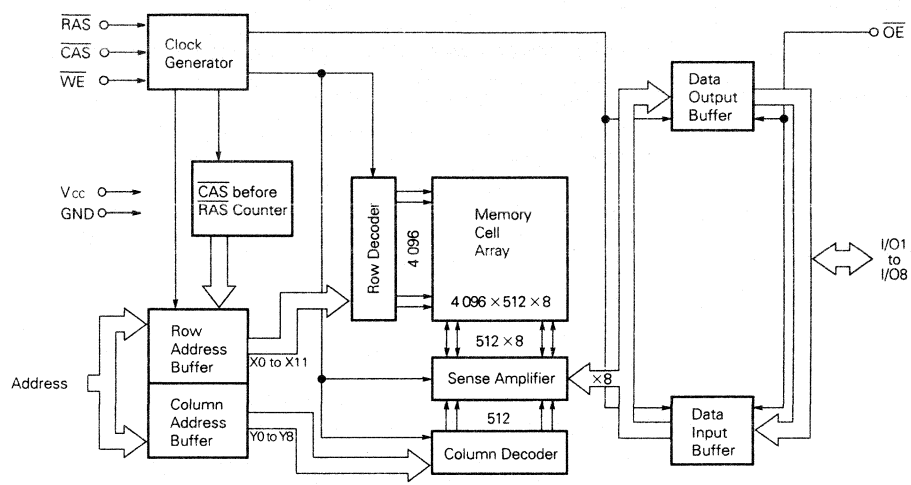


28-pin Plastic SOJ (400 mil)



- A0 to A11 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground

BLOCK DIAGRAM



INPUT/OUTPUT PIN FUNCTIONS

The μPD4216805 has input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11 and input/output pins I/O1 to I/O8.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)		Address bus. Input total 21-bit of address signal, upper 12-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 2 097 152-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/ Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

ELECTRICAL SPECIFICATIONS Notes1, 2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_I		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC}+1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

CAPACITANCE ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A11			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1 to I/O8			7	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling	t _{RAC} = 50 ns	100	mA	3,4,7
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 60 ns	90		
		I _O = 0 mA	t _{RAC} = 70 ns	80		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH} \text{ (MIN.)}$	I _O = 0 mA	2	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC}-0.2 \text{ V}$	I _O = 0 mA	1		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling	t _{RAC} = 50 ns	100	mA	3,4,5,7
		$\overline{\text{CAS}} \geq V_{IH} \text{ (MIN.)}$	t _{RAC} = 60 ns	90		
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 70 ns	80		
Operating current (Hyper page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{IL} \text{ (MAX.)}$	t _{RAC} = 50 ns	100	mA	3,4,6
		$\overline{\text{CAS}}$ Cycling	t _{RAC} = 60 ns	90		
		t _{HPC} = t _{HPC} (MIN.)	t _{RAC} = 70 ns	80		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling	t _{RAC} = 50 ns	100	mA	3,4
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 60 ns	90		
		I _O = 0 mA	t _{RAC} = 70 ns	80		
Input leakage current	I _{I(L)}	V _I = 0 to 5.5 V all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	V _O = 0 to 5.5 V Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage	V _{OH}	I _O = -5.0 mA	2.4		V	
Low level output voltage	V _{OL}	I _O = +4.2 mA		0.4	V	

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted) Notes 8, 9 (1/2)

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{RC}	84		104		124		ns	
Read Modify Write Cycle Time	t _{RWC}	107		133		157		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		50		60		70	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		13		15		18	ns	10, 11
Access Time from Column Address	t _{AA}		25		30		35	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		27		35		40	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEA}		13		15		18	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	9	25	12	30	12	35	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0		0		0		ns	11
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	10		13		15		ns	
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OEZ}	0	10	0	13	0	15	ns	12, 18
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0		0		0		ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t _T	1	50	1	50	1	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30		40		50		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10 000	60	10 000	70	10 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	7		10		12		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	7	10 000	10	10 000	12	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	35		40		50		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCd}	11	37	14	45	14	52	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	7		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	27		35		40		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	7		10		10		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	7		10		12		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	25		30		35		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	7		10		10		ns	15
$\overline{\text{WE}}$ Pulse Width	t _{WP}	7		10		10		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	7		10		10		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	27		32		37		ns	17
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	64		77		89		ns	17
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	39		47		54		ns	17

(2/2)

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
WE Lead Time Referenced to RAS	t _{RWL}	7		10		12		ns	
WE Lead Time Referenced to CAS	t _{CWL}	7		10		12		ns	
CAS Setup Time for CAS before RAS Refresh	t _{CSR}	5		5		5		ns	
CAS Hold Time for CAS before RAS Refresh	t _{CHR}	10		10		10		ns	
WE Setup Time	t _{WSR}	10		10		10		ns	
WE Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		64		64		64	ms	

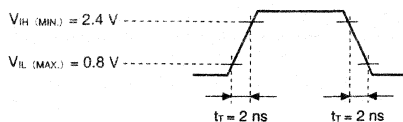
HYPER PAGE MODE

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{HPC}	20		25		30		ns	
RAS Pulse Width	t _{RASP}	50	125 000	60	125 000	70	125 000	ns	
CAS Pulse Width	t _{HCAS}	7	10 000	10	10 000	12	10 000	ns	
CAS Precharge Time	t _{CP}	7		10		10		ns	
CAS Precharge to WE Delay Time	t _{CPWD}	41		52		59		ns	17
Read Modify Write Cycle Time	t _{HPRWC}	52		66		75		ns	
Data Output Hold Time	t _{DHC}	5		5		5		ns	
Output Buffer Turn-off Delay from WE	t _{WEZ}	0	10	0	13	0	15	ns	12, 18
WE Pulse Width	t _{WPZ}	7		10		10		ns	18
Output Buffer Turn-off Delay from RAS	t _{OFR}	0	10	0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from CAS	t _{OFC}	0	10	0	13	0	15	ns	12, 18

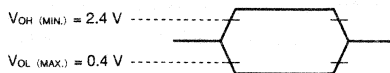
- Notes**
1. All voltages are referenced to GND.
 2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
 3. Icc1 , Icc3 , Icc4 and Icc5 depend on cycle rates (t_{AC} and t_{HPC}).
 4. Specified values are obtained with outputs unloaded.
 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
 6. Icc4 is measured assuming that all column address inputs are switched only once during each hyper page cycle.
 7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL(MAX.)}}$ and $\overline{\text{CAS}} \geq V_{\text{IH(MIN.)}}$.

- Notes** 8. AC measurements assume $t_r = 2$ ns.
 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{RAC} (MAX.)$	$t_{RAC} (MAX.)$
$t_{RAD} > t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{AA} (MAX.)$	$t_{RAD} + t_{AA} (MAX.)$
$t_{RCD} > t_{RCD} (MAX.)$	$t_{CAC} (MAX.)$	$t_{RCD} + t_{CAC} (MAX.)$

$t_{RAD} (MAX.)$ and $t_{RCD} (MAX.)$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD} (MAX.)$ and $t_{RCD} \geq t_{RCD} (MAX.)$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFC} (MAX.)$, $t_{OFR} (MAX.)$, $t_{WEZ} (MAX.)$, and $t_{OEZ} (MAX.)$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .
13. $t_{CRP} (MIN.)$ requirement is applied for $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycles.
14. Either $t_{RCH} (MIN.)$ or $t_{RRH} (MIN.)$ should be met in read cycles.
15. $t_{WP} (MIN.)$ is applied for late write cycles or read modify write cycles. In early write cycles, $t_{WCH} (MIN.)$ should be met.
16. $t_{DS} (MIN.)$ and $t_{DH} (MIN.)$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS} (MIN.)$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD} (MIN.)$, $t_{OWD} \geq t_{OWD} (MIN.)$, $t_{AWD} \geq t_{AWD} (MIN.)$ and $t_{CPWD} \geq t_{CPWD} (MIN.)$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
18. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)

$\overline{WE}$: inactive, $\overline{OE}$: active

t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)

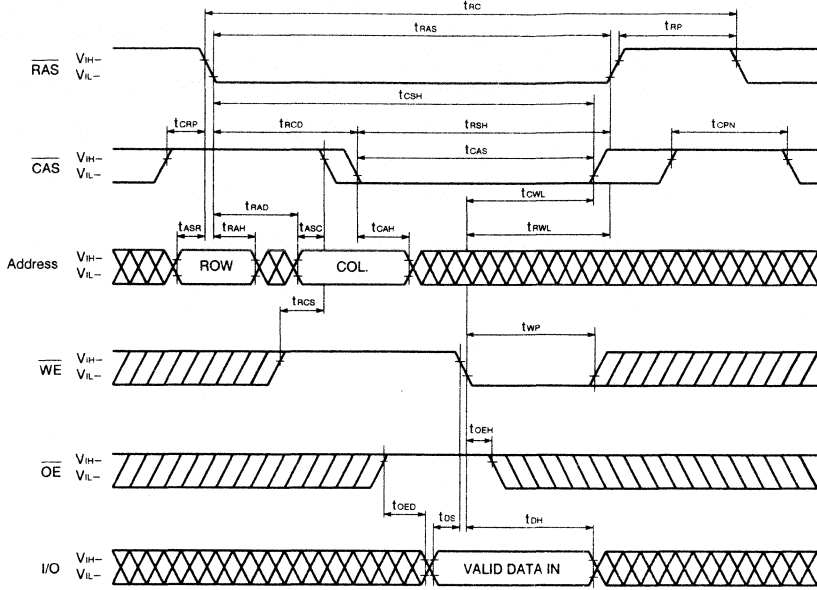
$\overline{WE}$: active, $\overline{OE}$: active... t_{WEZ} , t_{WPZ} are effective.

$\overline{WE}$: inactive, $\overline{OE}$: inactive... t_{OEZ} is effective.

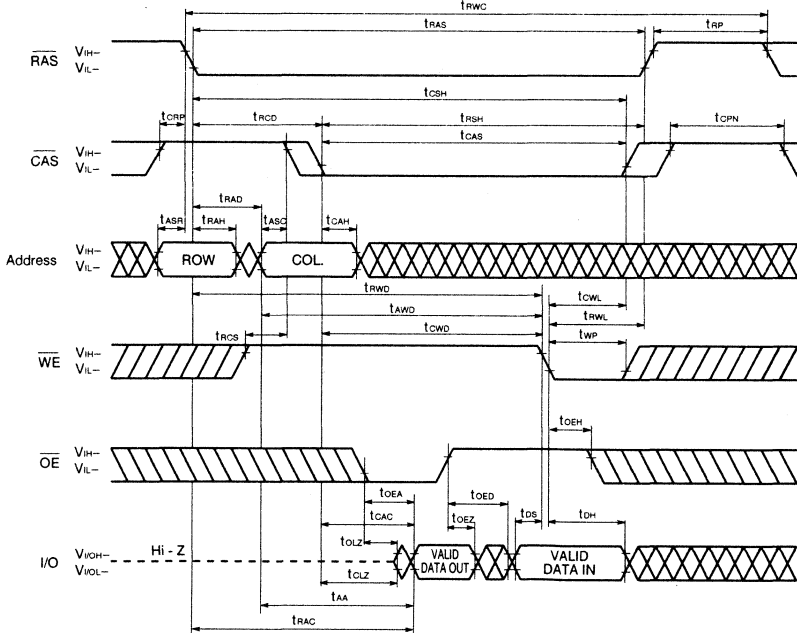
[illegible]

Remark $\overline{OE} = \text{Don't Care}$

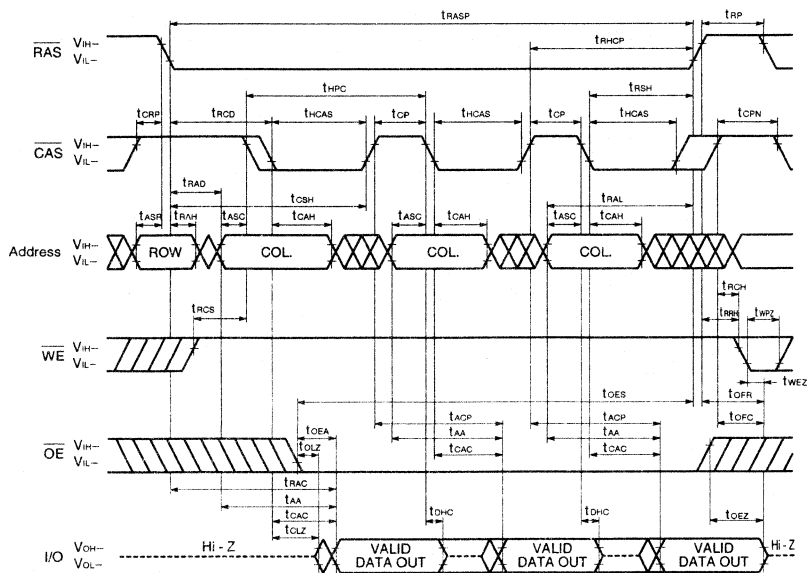
LATE WRITE CYCLE



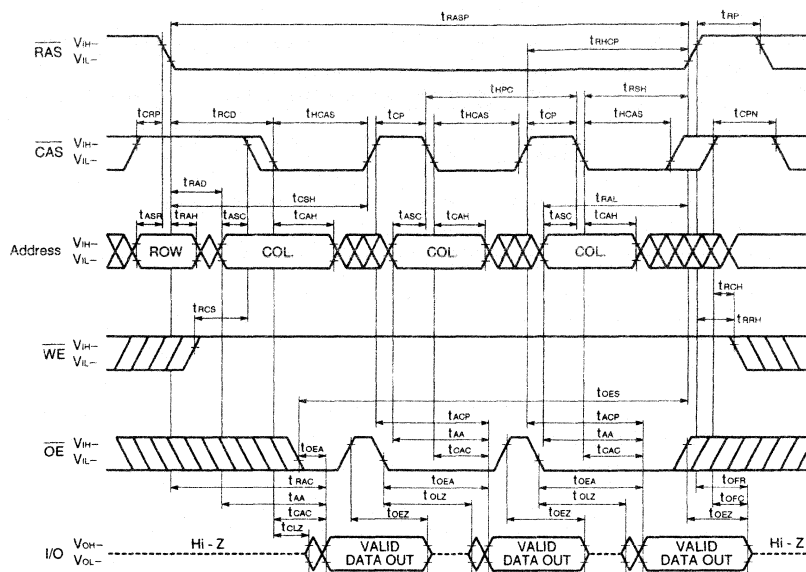
READ MODIFY WRITE CYCLE



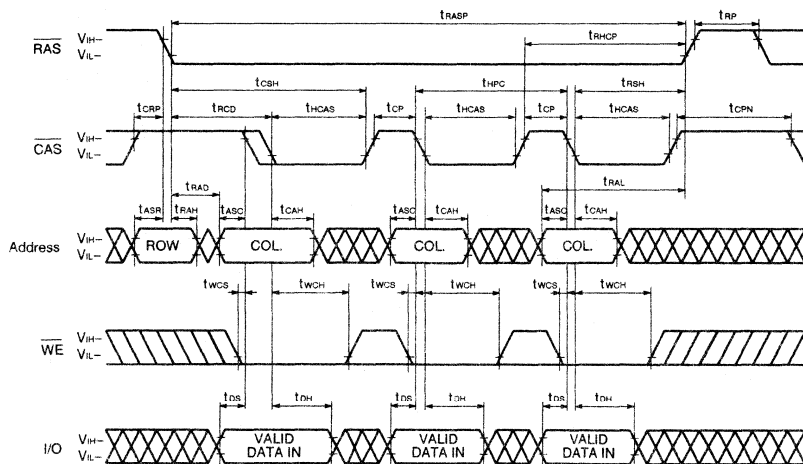
HYPER PAGE MODE READ CYCLE



HYPER PAGE MODE READ CYCLE ($\overline{\text{OE}}$ CONTROL)

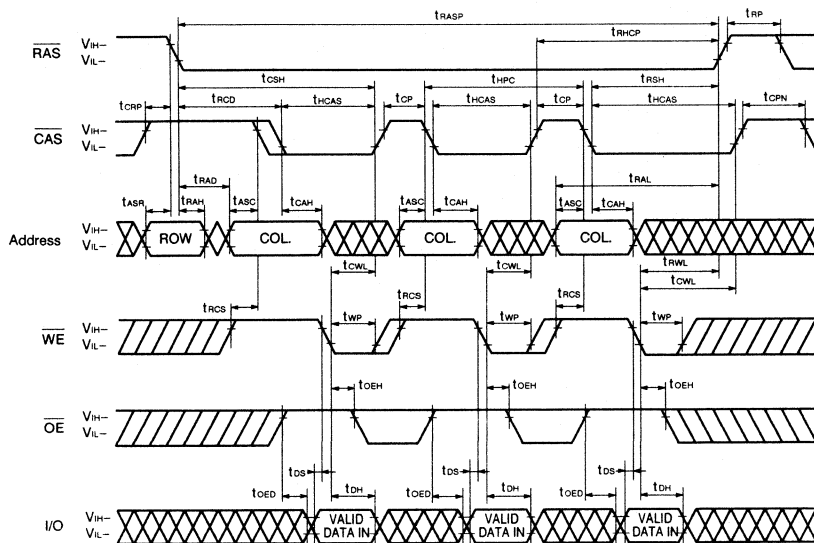


HYPER PAGE MODE EARLY WRITE CYCLE

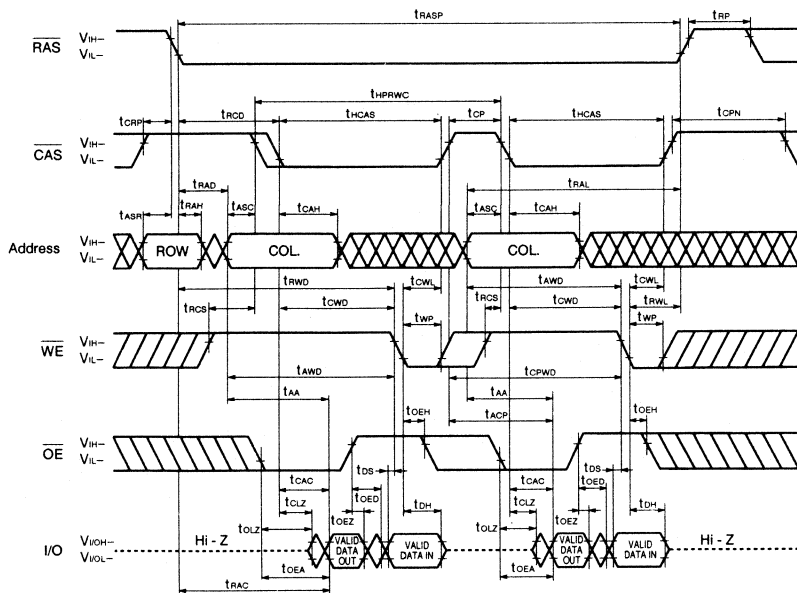


Remark $\overline{OE} = \text{Don't Care}$

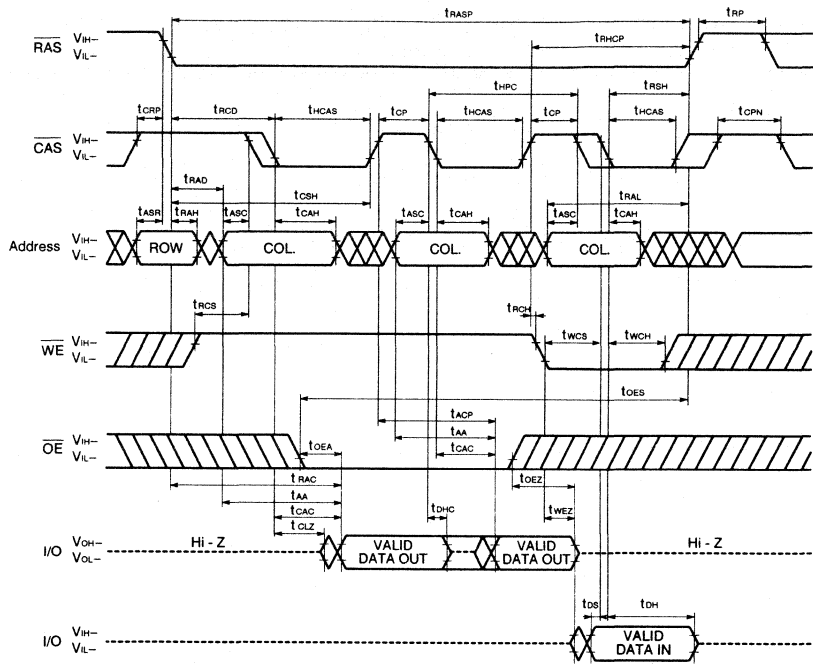
HYPER PAGE MODE LATE WRITE CYCLE



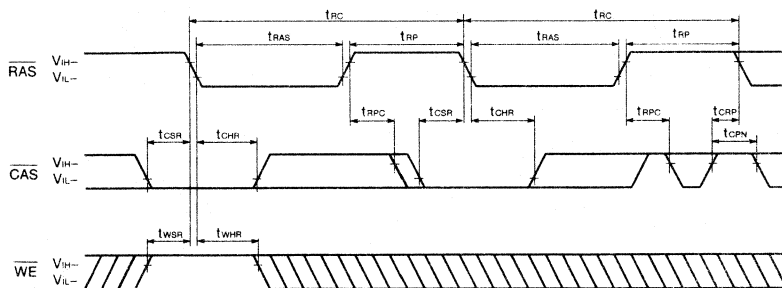
HYPER PAGE MODE READ MODIFY WRITE CYCLE



HYPER PAGE MODE READ AND WRITE CYCLE

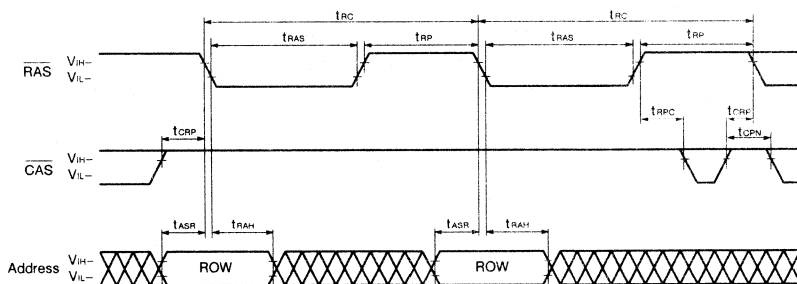


CAS BEFORE RAS REFRESH CYCLE



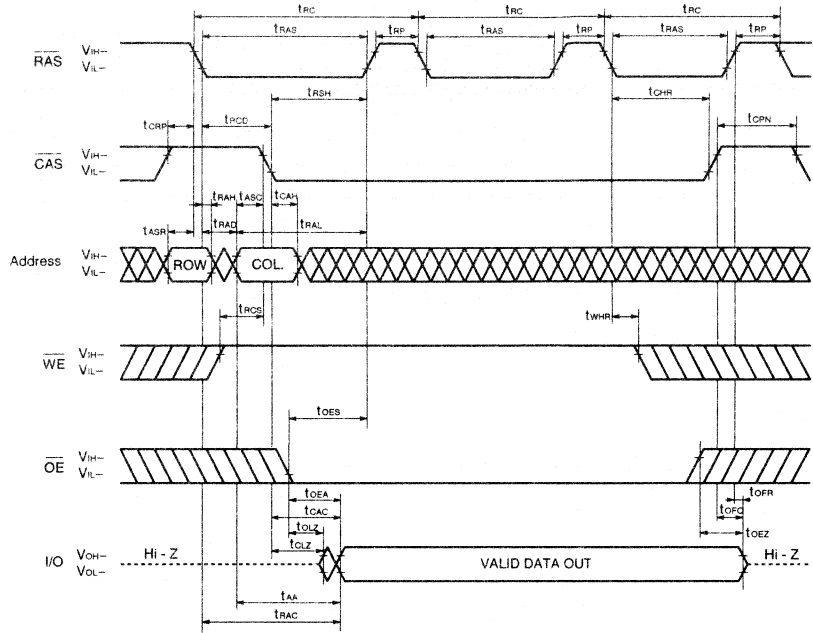
Remark Address, $\overline{OE}$ = Don't care I/O = Hi - Z

RAS ONLY REFRESH CYCLE

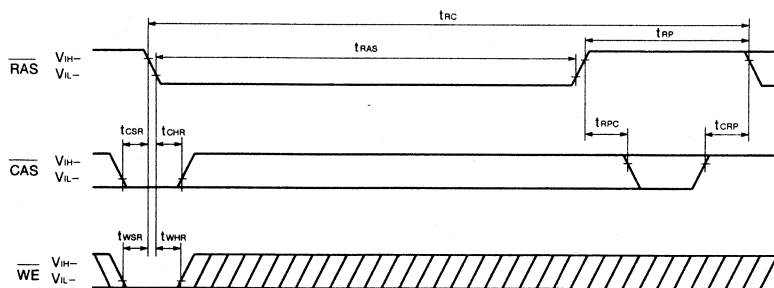


Remark $\overline{WE}$, $\overline{OE}$ = Don't care I/O = Hi - Z

HIDDEN REFRESH CYCLE



TEST MODE SET CYCLE ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE)



Remark Address, $\overline{\text{OE}}$ = Don't care I/O = Hi - Z

TEST MODE

TEST MODE is fast test function. On using this mode, test time is reduced to 1/2. In this TEST MODE, internal organization is 1 M words by 16 bits apparently. Don't care about the input levels of the column address input A0.

1. How to enter TEST MODE

Through TEST MODE SET CYCLE ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle), the device enters TEST MODE.

2. Write / Read in TEST MODE

Write data of "1" or "0" through I/O1 to I/O8 by controlling address except for above-mentioned address. Each input data through each I/O write 2 bits at once. And read through I/O1 to I/O8 to check written data. In case of writing each 2 bits rightly, each I/O data is "1". But wrong, the data is "0".

3. Refresh in TEST MODE

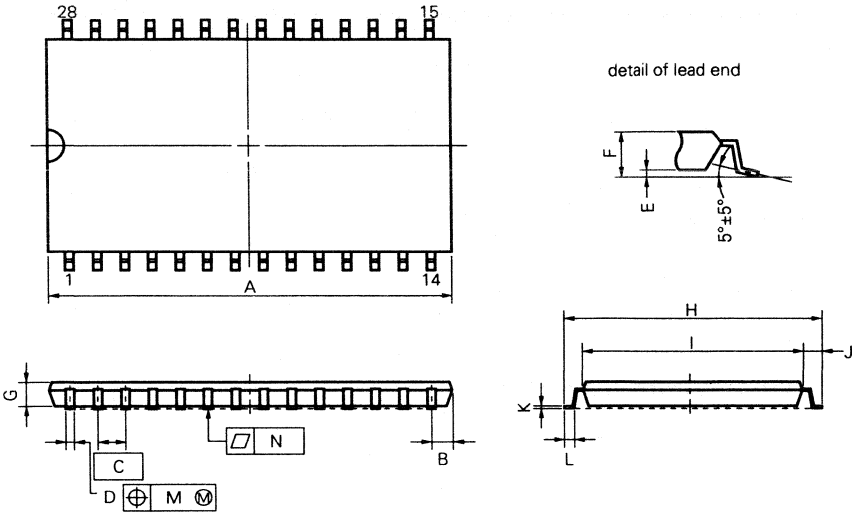
Use normal read cycle or $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

4. How to exit from TEST MODE

Through $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle, the device exits from TEST MODE.

PACKAGE DRAWINGS

28 PIN PLASTIC TSOP(III) (400 mil)



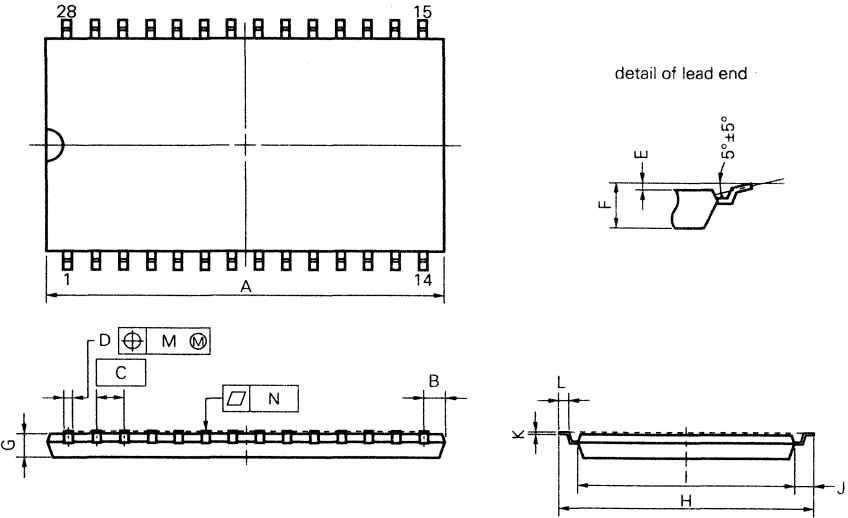
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD2-1

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP(II) (400 mil)

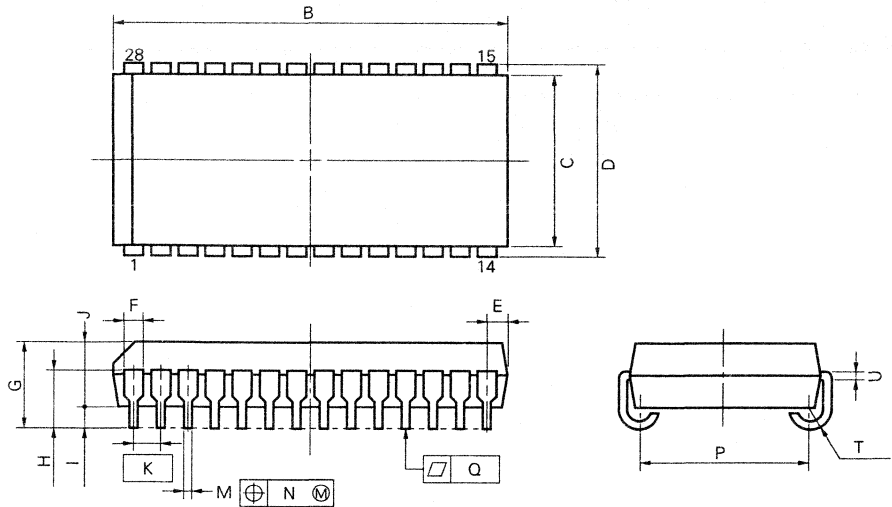


NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7KD2-1		
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LE-400A1

ITEM	MILLIMETERS	INCHES
B	18.67 ^{+0.2} _{-0.35}	0.735 ^{+0.008} _{-0.013}
C	10.16	0.400
D	11.18±0.2	0.440 ^{+0.008} _{-0.007}
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138 ^{+0.008} _{-0.007}
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.40±0.20	0.370 ^{+0.008} _{-0.007}
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μPD4216805.

TYPE OF SURFACE MOUNT DEVICE

μPD4216805G5 : 28-pin Plastic TSOP(II) (400 mil)

μPD4216805LE : 28-pin Plastic SOJ (400 mil)

μ PD42S16160, 4216160, 42S18160, 4218160**16 M-BIT DYNAMIC RAM****1 M-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE****Description**

The μ PD42S16160, 4216160, 42S18160, 4218160 are 1 048 576 words by 16 bits dynamic CMOS RAMs.

These differ in refresh cycle and the μ PD42S16160, 42S18160 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (see the table below).

These are packed in 50-pin plastic TSOP(II) and 42-pin plastic SOJ.

Features

- 1 048 576 words by 16 bits organization
- Fast page mode
- Fast access and cycle time
- Single +5.0 V ± 10 % power supply
- Byte read/write mode

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S16160-50, 4216160-50	605 mW	50 ns	90 ns	35 ns
μ PD42S18160-50, 4218160-50	935 mW			
μ PD42S16160-60, 4216160-60	550 mW	60 ns	110 ns	40 ns
μ PD42S18160-60, 4218160-60	880 mW			
μ PD42S16160-70, 4216160-70	495 mW	70 ns	130 ns	45 ns
μ PD42S18160-70, 4218160-70	825 mW			
μ PD42S16160-80, 4216160-80	440 mW	80 ns	150 ns	50 ns
μ PD42S18160-80, 4218160-80	770 mW			

- The μ PD42S16160, 42S18160 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S16160	4 096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μ PD42S18160	1 024 cycles/128 ms		
μ PD4216160	4 096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)
μ PD4218160	1 024 cycles/16 ms		

The information in this document is subject to change without notice.

★ Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD42S16160G5-50-7JF	50 ns	50-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S18160G5-50-7JF			
μ PD42S16160G5-60-7JF	60 ns		
μ PD42S18160G5-60-7JF			
μ PD42S16160G5-70-7JF	70 ns		
μ PD42S18160G5-70-7JF			
μ PD42S16160G5-80-7JF	80 ns		
μ PD42S18160G5-80-7JF			
μ PD42S16160LE-50	50 ns	42-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S18160LE-50			
μ PD42S16160LE-60	60 ns		
μ PD42S18160LE-60			
μ PD42S16160LE-70	70 ns		
μ PD42S18160LE-70			
μ PD42S16160LE-80	80 ns		
μ PD42S18160LE-80			
μ PD4216160G5-50-7JF	50 ns	50-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4218160G5-50-7JF			
μ PD4216160G5-60-7JF	60 ns		
μ PD4218160G5-60-7JF			
μ PD4216160G5-70-7JF	70 ns		
μ PD4218160G5-70-7JF			
μ PD4216160G5-80-7JF	80 ns		
μ PD4218160G5-80-7JF			
μ PD4216160LE-50	50 ns	42-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4218160LE-50			
μ PD4216160LE-60	60 ns		
μ PD4218160LE-60			
μ PD4216160LE-70	70 ns		
μ PD4218160LE-70			
μ PD4216160LE-80	80 ns		
μ PD4218160LE-80			

Quality Grade

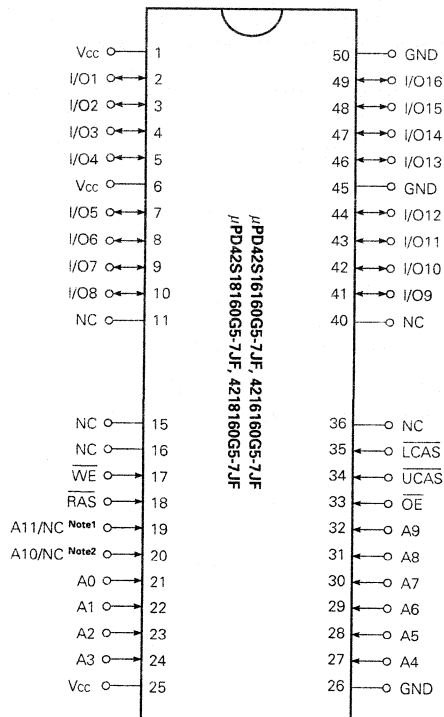
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

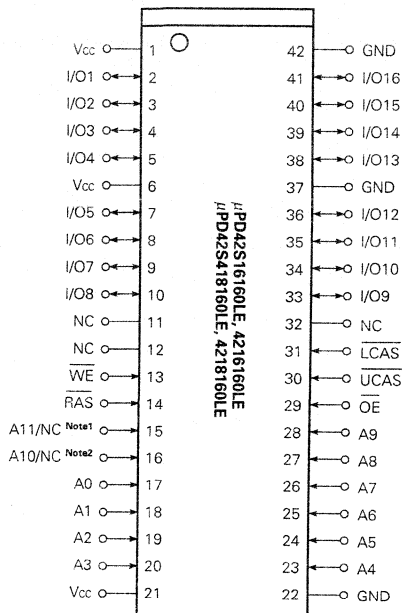
Pin Configurations (Marking Side)



50-pin Plastic TSOP (II) (400 mil)



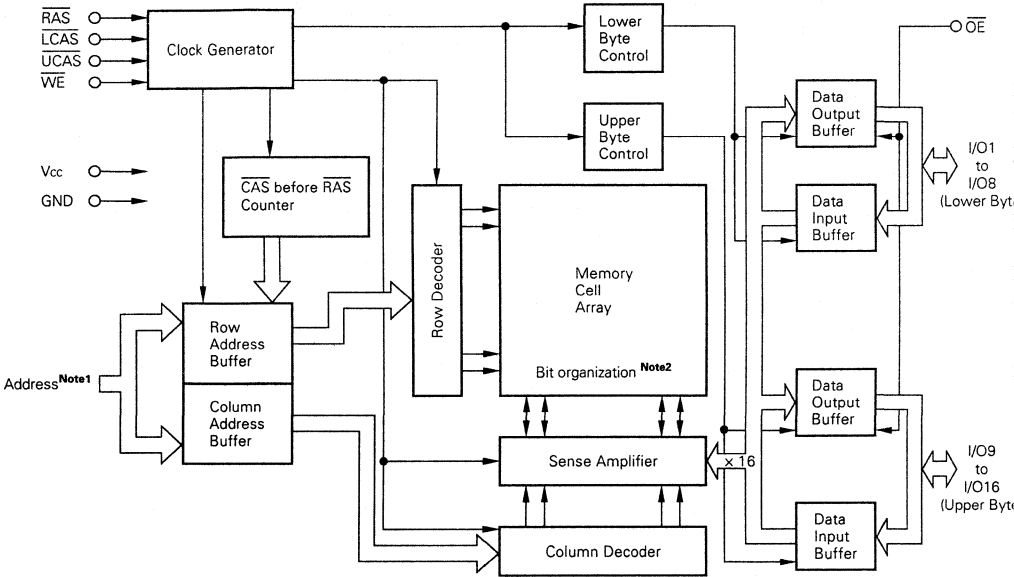
42-pin Plastic SOJ (400 mil)



- Notes** 1. A11...μPD42S16160, 4216160 NC...μPD42S18160, 4218160
2. A10...μPD42S16160, 4216160 NC...μPD42S18160, 4218160

A0 to A11 : Address Inputs
I/O1 to I/O16 : Data Inputs/Outputs
RAS : Row Address Strobe
UCAS : Column Address Strobe (upper)
LCAS : Column Address Strobe (lower)
WE : Write Enable
OE : Output Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S16160, 4216160	A0 to A11	A0 to A7
μPD42S18160, 4218160	A0 to A9	A0 to A9

2. μPD42S16160...4 096 × 256 × 16 μPD42S18160...1 024 × 1 024 × 16

Input/Output Pin Functions

The μPD42S16160, 4216160, 42S18160, 4218160 have input pins $\overline{RAS}$, $\overline{CAS}$ ^{Note1}, $\overline{WE}$, $\overline{OE}$, A0 to A11/A9 ^{Note2} and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11/A9 ^{Note2} (Address inputs)		Address bus. Input total 20-bit of address signal, upper 12/10 ^{Note3} -bit and lower 8/10 ^{Note4} -bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input/ Output	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)		16-bit data bus. I/O1 to I/O16 are used to input/output data.

Notes 1. $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

2. A11 ... μPD42S16160, 4216160 A9 ... μPD42S18160, 4218160

3. 12 ... μPD42S16160, 4216160 10 ... μPD42S18160, 4218160

4. 8 ... μPD42S16160, 4216160 10 ... μPD42S18160, 4218160

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^{\circ}\text{C}$

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	$^{\circ}\text{C}$

Capacitance ($T_a = +25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A11			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1 to I/O16			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[μ PD42S16160, 4216160]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	RAS, CAS Cycling trc = trc(MIN.) Io = 0 mA	trac = 50 ns		110	mA	1,2,3
				trac = 60 ns		100		
				trac = 70 ns		90		
				trac = 80 ns		80		
Standby current	μPD42S16160	I _{CC2}	RAS, CAS ≥ VIH(MIN.) Io = 0 mA			2	mA	
	μPD4216160		RAS, CAS ≥ Vcc - 0.2 V Io = 0 mA			0.25		
			RAS, CAS ≥ VIH(MIN.) Io = 0 mA			2		
			RAS, CAS ≥ Vcc - 0.2 V Io = 0 mA			1		
RAS only refresh current		I _{CC3}	RAS Cycling CAS ≥ VIH(MIN.) trc = trc(MIN.) Io = 0 mA	trac = 50 ns		110	mA	1,2,3,4
				trac = 60 ns		100		
				trac = 70 ns		90		
				trac = 80 ns		80		
Operating current (Fast page mode)		I _{CC4}	RAS ≤ VIL(MAX.) CAS Cycling tpc = tpc(MIN.) Io = 0 mA	trac = 50 ns		100	mA	1,2,5
				trac = 60 ns		90		
				trac = 70 ns		80		
				trac = 80 ns		70		
CAS before RAS refresh current		I _{CC5}	RAS Cycling trc = trc(MIN.) Io = 0 mA	trac = 50 ns		110	mA	1,2
				trac = 60 ns		100		
				trac = 70 ns		90		
				trac = 80 ns		80		
CAS before RAS long refresh current (4 096 cycles/128 ms, only for μPD42S16160)		I _{CC6}	CAS before RAS Refresh : 4 096 cycles/128 ms RAS, CAS : Vcc -0.2 V ≤ VIH ≤ VIH(MAX.) 0 V ≤ VIL ≤ 0.2 V Standby : RAS ≥ Vcc - 0.2 V Address : Don't care WE, OE : VIH Io = 0 mA	tras ≤ 300 ns		450	μA	1,2
				tras ≤ 1 μs		600		
Self refresh current (CAS before RAS self refresh, only for μPD42S16160)		I _{CC7}	RAS, CAS : Vcc -0.2 V ≤ VIH ≤ VIH(MAX.) 0 V ≤ VIL ≤ 0.2 V Io = 0 mA			250	μA	2
Input leakage current		II (L)	VI = 0 to 5.5 V all other pins not under test = 0 V		-10	+10	μA	
Output leakage current		IO (L)	Output is disabled (Hi-Z) VO = 0 to 5.5 V		-10	+10	μA	
High level output voltage		VOH	Io = -2.5 mA		2.4		V	
Low level output voltage		VOL	Io = +2.1 mA			0.4	V	

[μ PD42S18160, 4218160]

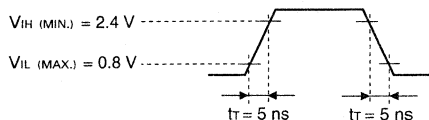
Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes	
Operating current		Icc1	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		170	mA	1,2,3	
				$\text{trac} = 60 \text{ ns}$		160			
				$\text{trac} = 70 \text{ ns}$		150			
				$\text{trac} = 80 \text{ ns}$		140			
Standby current	$\mu\text{PD42S18160}$	Icc2	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$I_o = 0 \text{ mA}$		2	mA		
	$\mu\text{PD4218160}$		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$I_o = 0 \text{ mA}$		0.25			
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$I_o = 0 \text{ mA}$		2			
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$I_o = 0 \text{ mA}$		1			
$\overline{\text{RAS}}$ only refresh current		Icc3	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		170	mA	1,2,3,4	
				$\text{trac} = 60 \text{ ns}$		160			
				$\text{trac} = 70 \text{ ns}$		150			
				$\text{trac} = 80 \text{ ns}$		140			
Operating current (Fast page mode)		Icc4	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ $\overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		100	mA	1,2,5	
				$\text{trac} = 60 \text{ ns}$		90			
				$\text{trac} = 70 \text{ ns}$		80			
				$\text{trac} = 80 \text{ ns}$		70			
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		Icc5	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		170	mA	1,2	
				$\text{trac} = 60 \text{ ns}$		160			
				$\text{trac} = 70 \text{ ns}$		150			
				$\text{trac} = 80 \text{ ns}$		140			
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (1 024 cycles/128 ms, only for $\mu\text{PD42S18160}$)		Icc6	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh : 1 024 cycles/128 ms $\overline{\text{RAS}}, \overline{\text{CAS}} : V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby : $\overline{\text{RAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : Don't care $\overline{\text{WE}}, \overline{\text{OE}} : V_{\text{IH}}$ $I_o = 0 \text{ mA}$	$\text{tras} \leq 300 \text{ ns}$		350	μA	1,2	
				$\text{tras} \leq 1 \mu\text{s}$		400			
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for $\mu\text{PD42S18160}$)		Icc7	$\overline{\text{RAS}}, \overline{\text{CAS}} : V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$			250	μA	2	
Input leakage current		$I_i (\text{IL})$	$V_i = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V		-10	+10	μA		
Output leakage current		$I_o (\text{LO})$	Output is disabled (Hi-Z) $V_o = 0 \text{ to } 5.5 \text{ V}$		-10	+10	μA		
High level output voltage		V_{OH}	$I_o = -2.5 \text{ mA}$		2.4		V		
Low level output voltage		V_{OL}	$I_o = +2.1 \text{ mA}$			0.4	V		

- Notes**
1. t_{CC1} , t_{CC3} , t_{CC4} , t_{CC5} and t_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
 2. Specified values are obtained with outputs unloaded.
 3. t_{CC1} and t_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.
 4. t_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. t_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

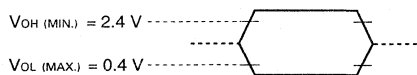
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write Read Modify Write Cycle

Parameter		Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		t _{RC}	90	–	110	–	130	–	150	–	ns	
RAS Precharge Time		t _{RP}	30	–	40	–	50	–	60	–	ns	
CAS Precharge Time		t _{CPN}	8	–	10	–	10	–	10	–	ns	
RAS Pulse Width		t _{RAS}	50	10 000	60	10 000	70	10 000	80	10 000	ns	
CAS Pulse Width		t _{CAS}	13	10 000	15	10 000	20	10 000	20	10 000	ns	
RAS Hold Time		t _{RSH}	13	–	15	–	18	–	20	–	ns	
CAS Hold Time		t _{CSH}	50	–	60	–	70	–	80	–	ns	
RAS to CAS Delay Time		t _{RCD}	18	32	20	45	20	50	25	60	ns	1
RAS to Column Address Delay Time		t _{RAD}	13	25	15	30	15	35	17	40	ns	1
CAS to RAS Precharge Time		t _{CRP}	5	–	5	–	5	–	5	–	ns	2
Row Address Setup Time		t _{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time		t _{RAH}	8	–	10	–	10	–	12	–	ns	
Column Address Setup Time		t _{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time		t _{CAH}	13	–	15	–	15	–	15	–	ns	
OE Lead Time Referenced to RAS		t _{OES}	0	–	0	–	0	–	0	–	ns	
CAS to Data Setup Time		t _{CLZ}	0	–	0	–	0	–	0	–	ns	
OE to Data Setup Time		t _{OLZ}	0	–	0	–	0	–	0	–	ns	
OE to Data Delay Time		t _{OED}	10	–	13	–	15	–	15	–	ns	
Masked Byte Write Hold Time Referenced to RAS		t _{MRH}	0	–	0	–	0	–	0	–	ns	
Transition Time (Rise and Fall)		t _T	3	50	3	50	3	50	3	50	ns	
Refresh Time	μPD42S16160, 42S18160	t _{REF}	–	128	–	128	–	128	–	128	ms	3
	μPD4216160		–	64	–	64	–	64	–	64		
	μPD4218160		–	16	–	16	–	16	–	16		

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD(MAX.) and trCD(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD(MAX.)}$ and $\text{trCD} \geq \text{trCD(MAX.)}$ will not cause any operation problems.

- tCRP(MIN.) requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
- This specification is applied only to the μ PD42S16160, 42S18160.

Read Cycle

Parameter	Symbol	$\text{trAC} = 50 \text{ ns}$		$\text{trAC} = 60 \text{ ns}$		$\text{trAC} = 70 \text{ ns}$		$\text{trAC} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	trAC	–	50	–	60	–	70	–	80	ns	1
Access Time from $\overline{\text{CAS}}$	tCAC	–	15	–	15	–	20	–	20	ns	1
Access Time from Column Address	tAA	–	25	–	30	–	35	–	40	ns	1
Access Time from $\overline{\text{OE}}$	tOEA	–	15	–	15	–	20	–	20	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	trAL	25	–	30	–	35	–	40	–	ns	
Read Command Setup Time	trCS	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	trRH	0	–	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	trCH	0	–	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	tOEZ	0	10	0	13	0	15	0	15	ns	3
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	tOFF	0	10	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD(MAX.) and trCD(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD(MAX.)}$ and $\text{trCD} \geq \text{trCD(MAX.)}$ will not cause any operation problems.

- Either trCH(MIN.) or trRH(MIN.) should be met in read cycles.
- tOFF(MAX.) and tOEZ(MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{WAC} = 50 ns		t _{WAC} = 60 ns		t _{WAC} = 70 ns		t _{WAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
WE Hold Time Referenced to $\overline{\text{CAS}}$	twch	8	–	10	–	10	–	15	–	ns	1
WE Pulse Width	twp	8	–	10	–	10	–	15	–	ns	1
WE Lead Time Referenced to $\overline{\text{RAS}}$	trwl	18	–	20	–	20	–	20	–	ns	
WE Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	13	–	15	–	15	–	15	–	ns	
WE Setup Time	twcs	0	–	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	–	0	–	0	–	0	–	ns	
Data-in Setup Time	t _{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in Hold Time	t _{DH}	10	–	10	–	15	–	15	–	ns	3

- Notes**
1. t_{WAC}(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch(MIN.) should be met.
 2. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS}(MIN.) and t_{DH}(MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the WE falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{WAC} = 50 ns		t _{WAC} = 60 ns		t _{WAC} = 70 ns		t _{WAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	140	–	160	–	180	–	200	–	ns	
$\overline{\text{RAS}}$ to WE Delay Time	trwd	70	–	83	–	95	–	105	–	ns	1
$\overline{\text{CAS}}$ to WE Delay Time	tcwd	33	–	38	–	40	–	45	–	ns	1
Column Address to WE Delay Time	tawd	45	–	53	–	60	–	65	–	ns	1

- Note**
1. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwd ≥ trwd(MIN.), tcwd ≥ tcwd(MIN.), tawd ≥ tawd(MIN.) and tcpwd ≥ tcpwd(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	35	–	40	–	45	–	50	–	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	–	30	–	35	–	40	–	45	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RASP}	50	125 000	60	125 000	70	125 000	80	125 000	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	8	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	–	35	–	40	–	45	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	80	–	85	–	90	–	105	–	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	55	–	60	–	65	–	70	–	ns	1

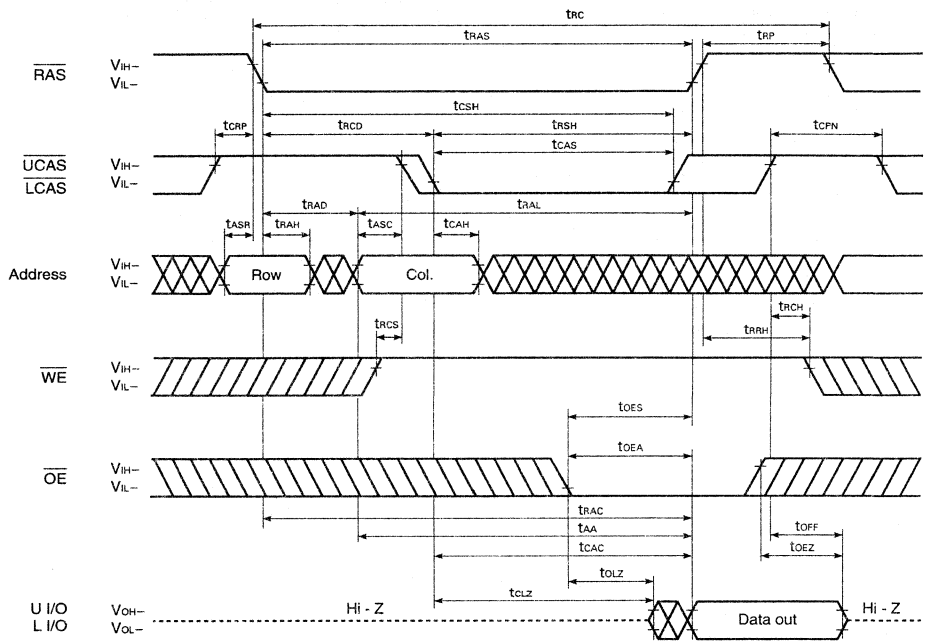
Note 1. If $\text{twcs} \geq \text{twcs}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $\text{trwd} \geq \text{trwd}(\text{MIN.})$, $\text{tcwd} \geq \text{tcwd}(\text{MIN.})$, $\text{tawd} \geq \text{tawd}(\text{MIN.})$ and $\text{tcpwd} \geq \text{tcpwd}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

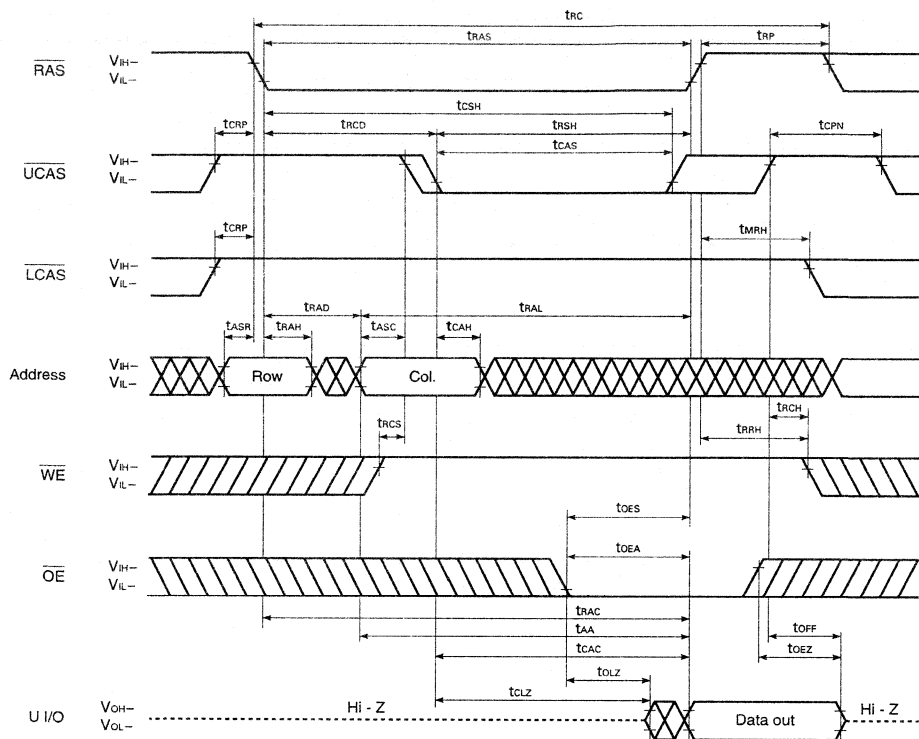
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ Setup Time	t _{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RASS}	100	–	100	–	100	–	100	–	μ s	1
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RPS}	90	–	110	–	130	–	150	–	ns	1
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ Hold Time (Hidden Refresh Cycle)	t _{WHR}	15	–	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μ PD42S16160, 42S18160.

Read Cycle

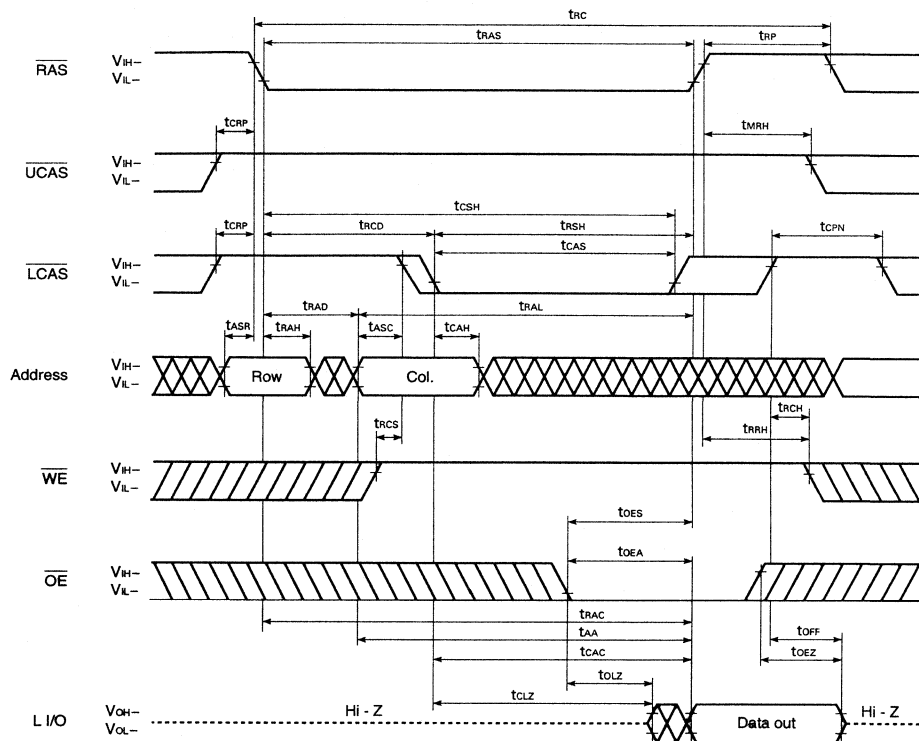


Upper Byte Read Cycle



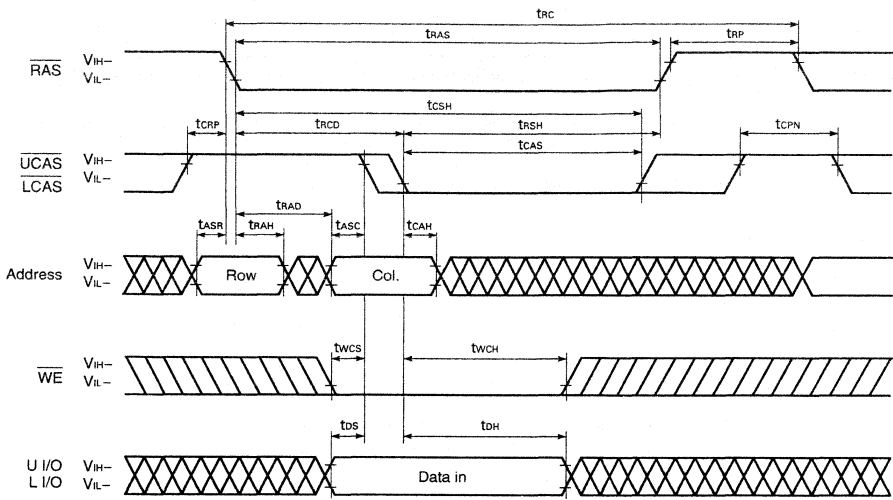
Remark L I/O : Hi-Z

Lower Byte Read Cycle



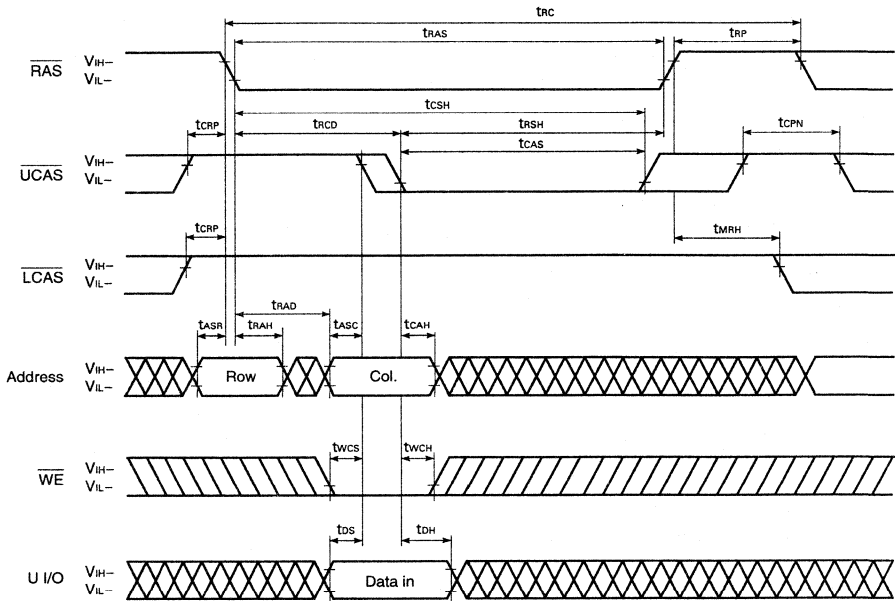
Remark U I/O : Hi-Z

Early Write Cycle



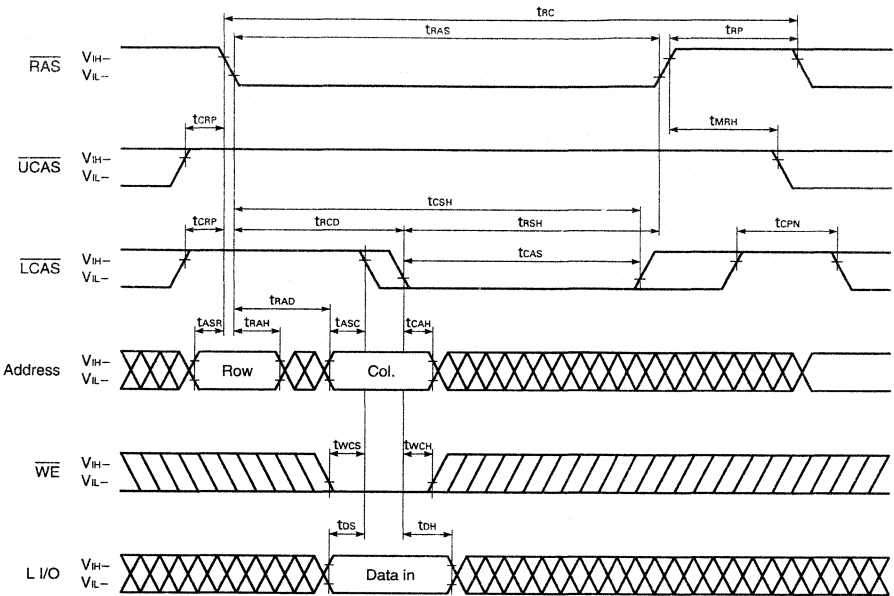
Remark $\overline{\text{OE}}$: Don't care

Upper Byte Early Write Cycle



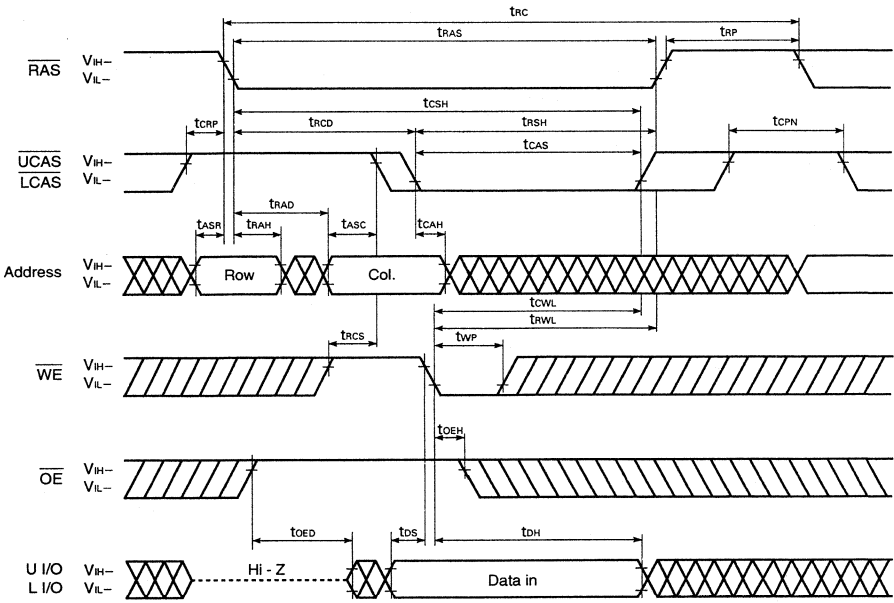
Remark $\overline{OE}$, L I/O : Don't care

Lower Byte Early Write Cycle

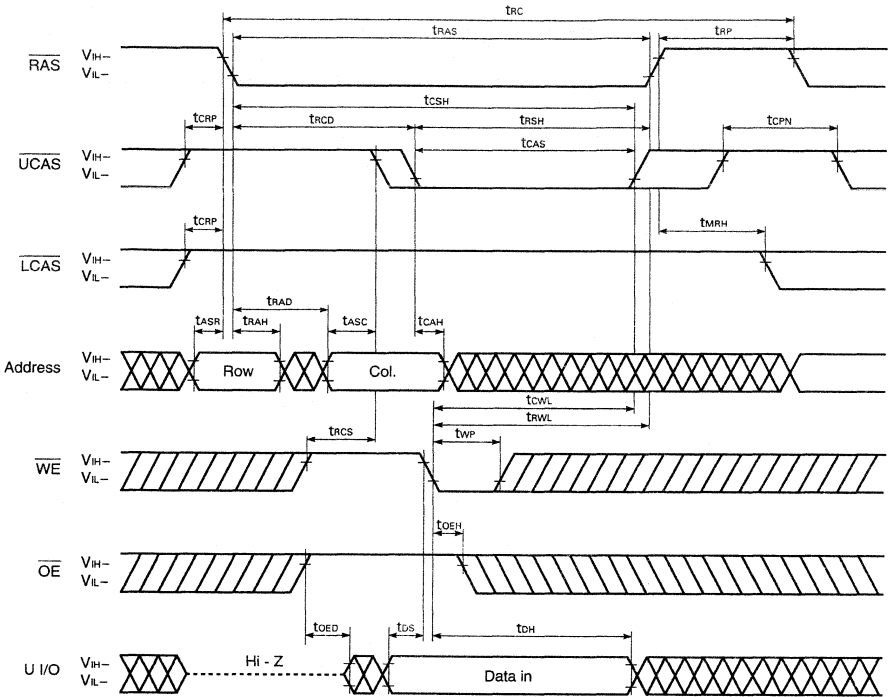


Remark $\overline{OE}$, U I/O : Don't care

Late Write Cycle

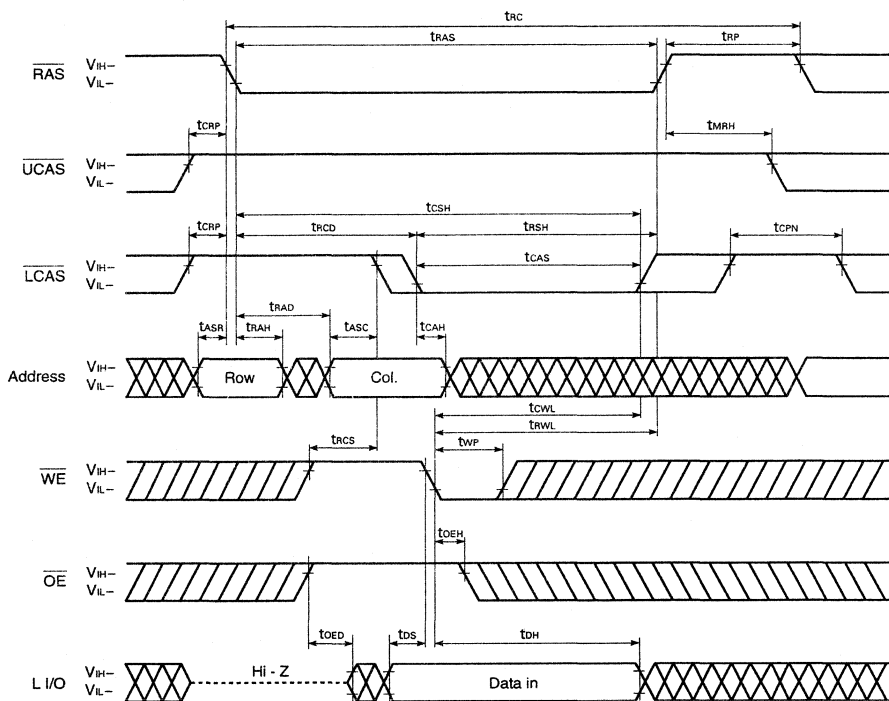


Upper Byte Late Write Cycle



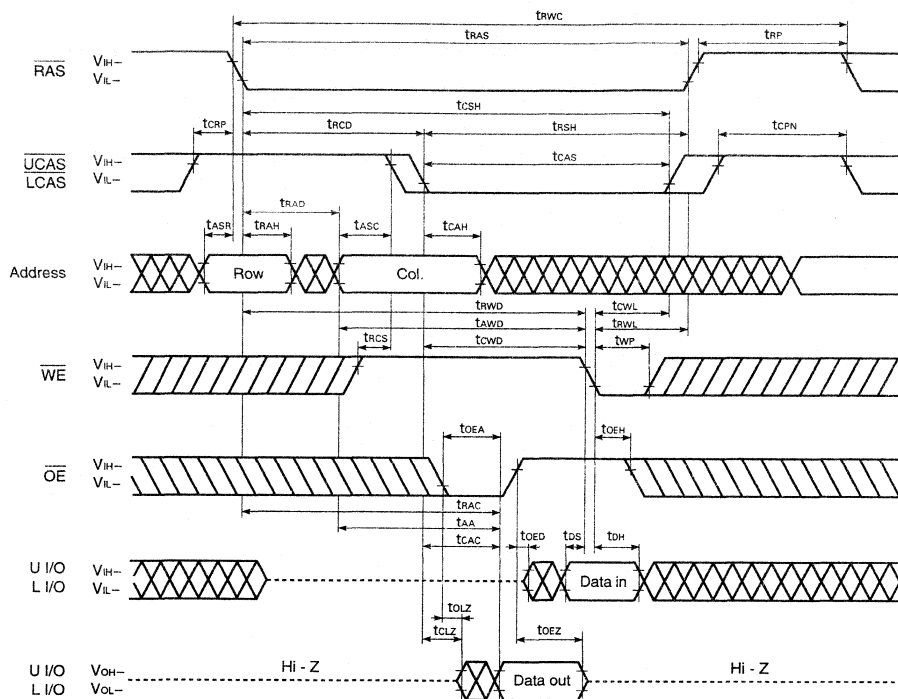
Remark L I/O : Don't care

Lower Byte Late Write Cycle



Remark U I/O : Don't care

Read Modify Write Cycle



[illegible]

Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

[illegible]

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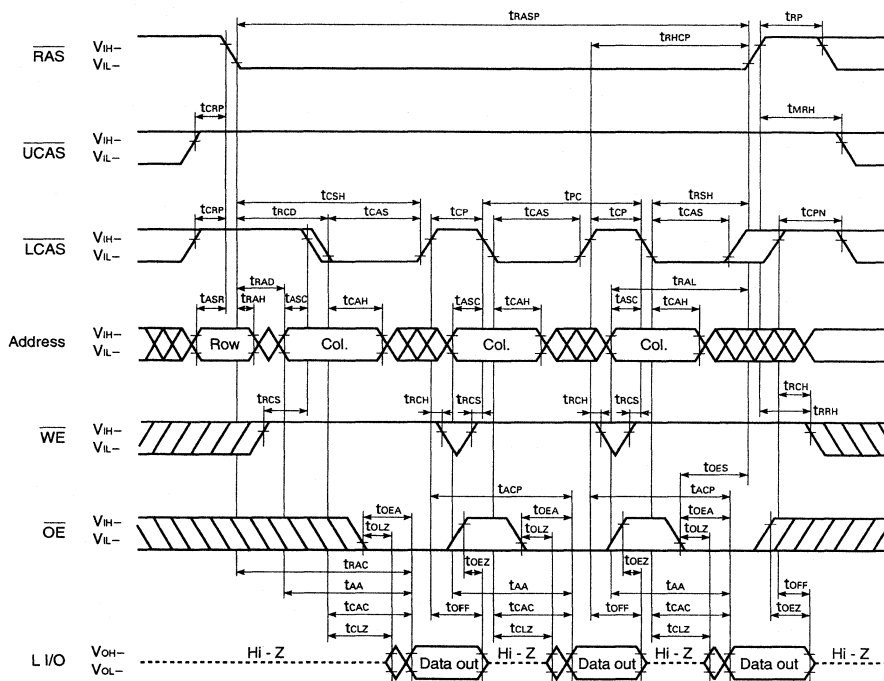
[illegible]

224

[illegible]

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

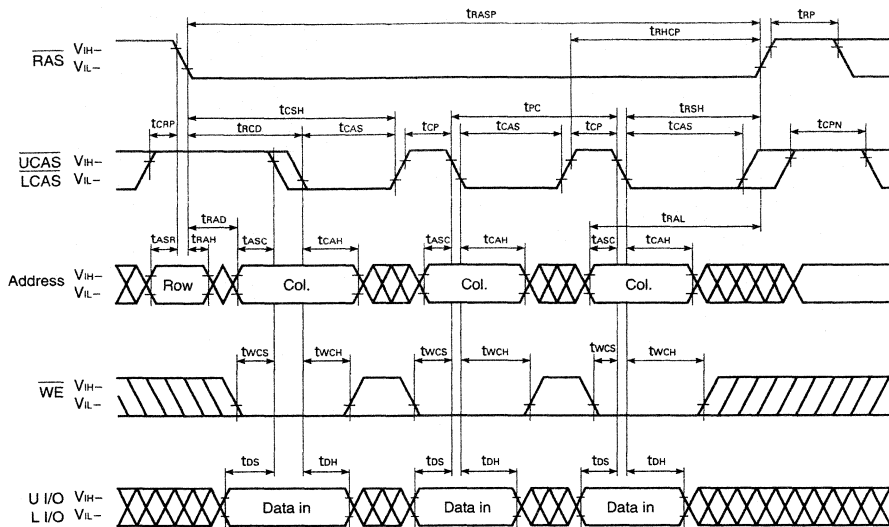
Fast Page Mode Lower Byte Read Cycle



Remark U I/O : Hi-Z

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

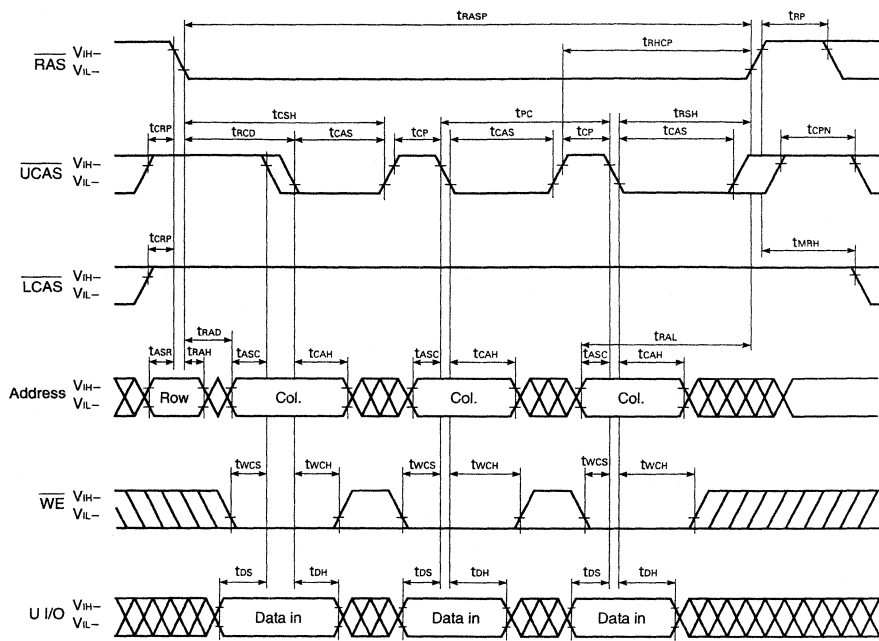
Fast Page Mode Early Write Cycle



Remark $\overline{OE}$: Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

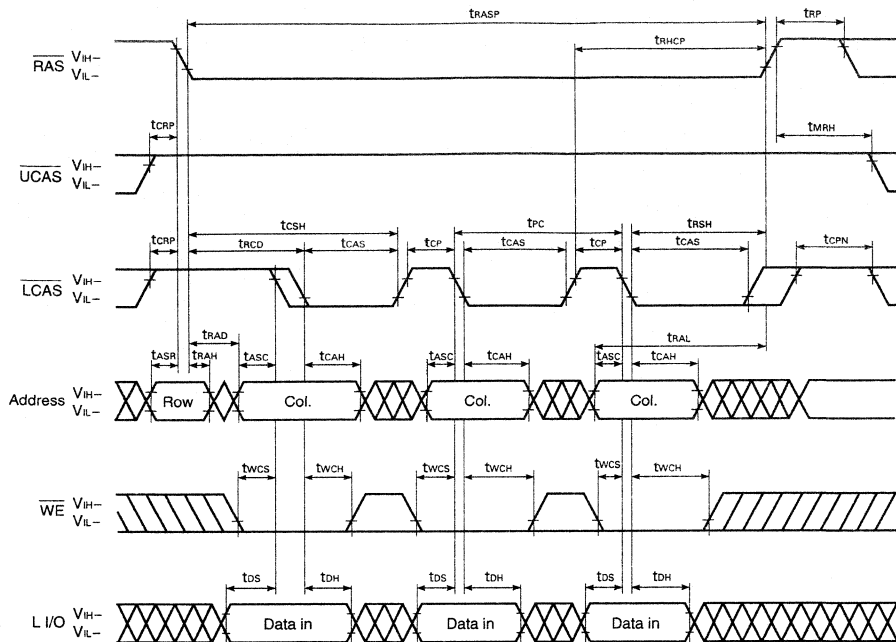
Fast Page Mode Upper Byte Early Write Cycle



Remark $\overline{OE}$, L I/O : Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

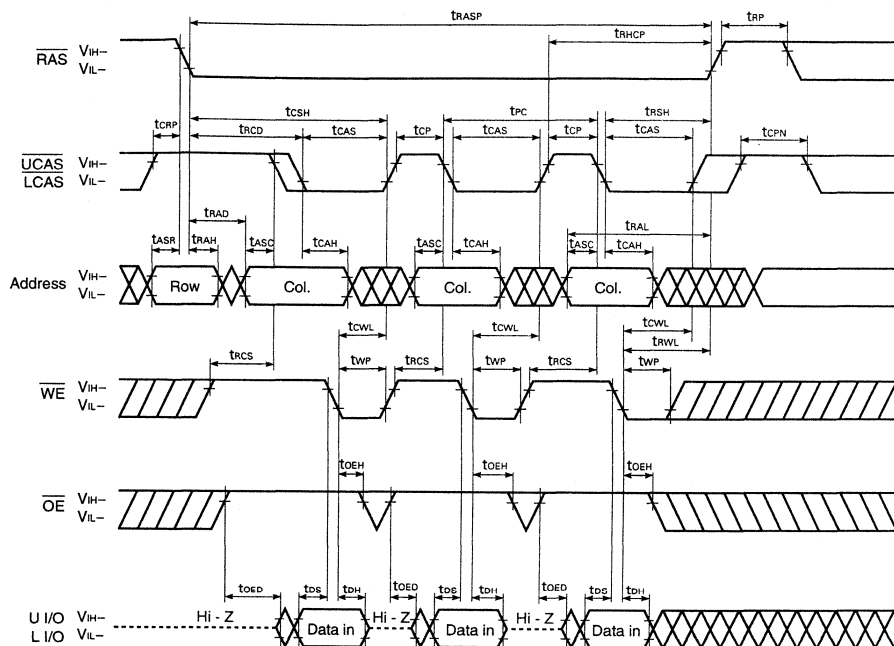
Fast Page Mode Lower Byte Early Write Cycle



Remark $\overline{OE}$, U I/O : Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

[illegible]

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

The diagram illustrates the timing relationships between several control and data signals during memory access operations. The signals shown are:

- RAS**: Row Address Strobe, active low.
- UCAS**: Upper Chip Address Strobe, active low.
- LCAS**: Lower Chip Address Strobe, active low.
- Address**: Data bus address, alternating between Row and Column addresses.
- WE**: Write Enable, active low.
- OE**: Output Enable, active low.
- L I/O**: Local Input/Output data bus.
- U I/O**: User Input/Output data bus.

Key timing parameters labeled include:

- t_{TRASP}**, **t_{RHP}**, **t_{RP}**: RAS pulse width and recovery times.
- t_{CRP}**, **t_{MRH}**: UCAS setup and hold times.
- t_{CSH}**, **t_{CAS}**, **t_{CP}**, **t_{PC}**, **t_{SH}**, **t_{CA}**, **t_{CPN}**: Various chip select and column strobe timing parameters.
- t_{ASR}**, **t_{AH}**, **t_{ASC}**, **t_{CAH}**: Address setup and hold times.
- t_{TWL}**, **t_{WPL}**, **t_{ACS}**, **t_{OWL}**, **t_{RWL}**: Write enable and output enable timing parameters.
- t_{OEH}**: Output Enable hold time.
- t_{OD}**, **t_{DS}**, **t_{DH}**: Data bus output delay, setup, and hold times.

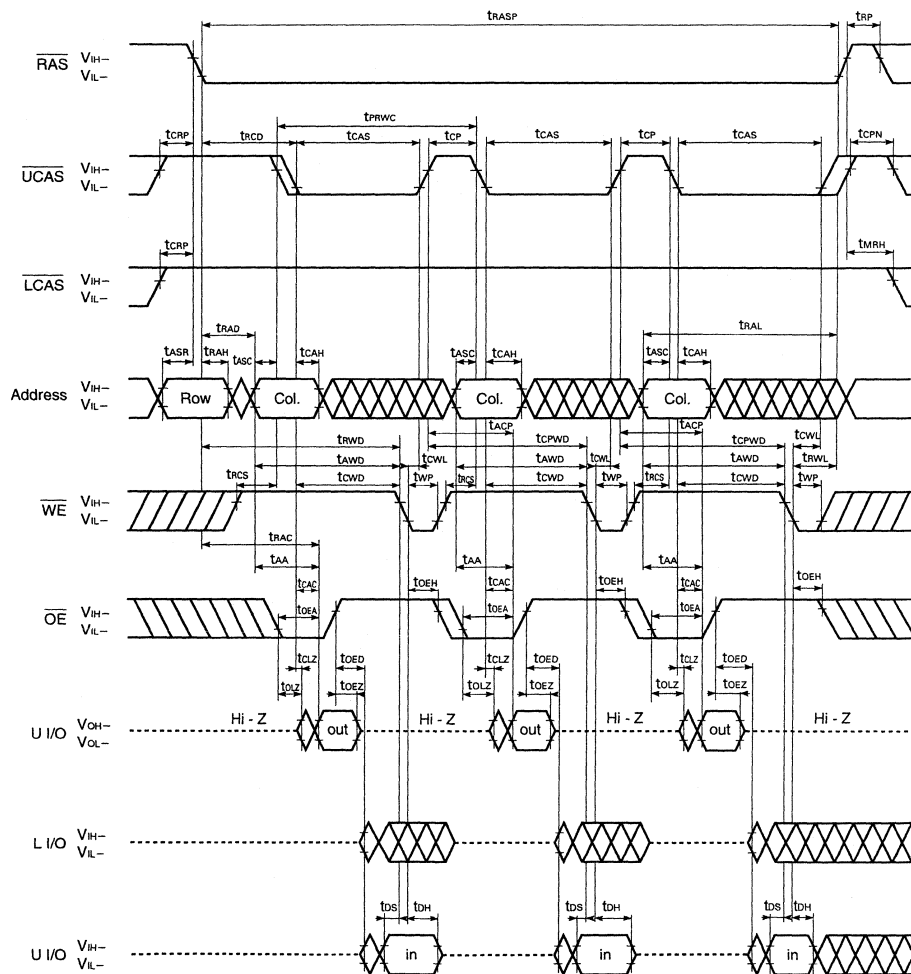
Data flow is indicated by arrows: from L I/O to U I/O for writes, and from U I/O to L I/O for reads.

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

[illegible]

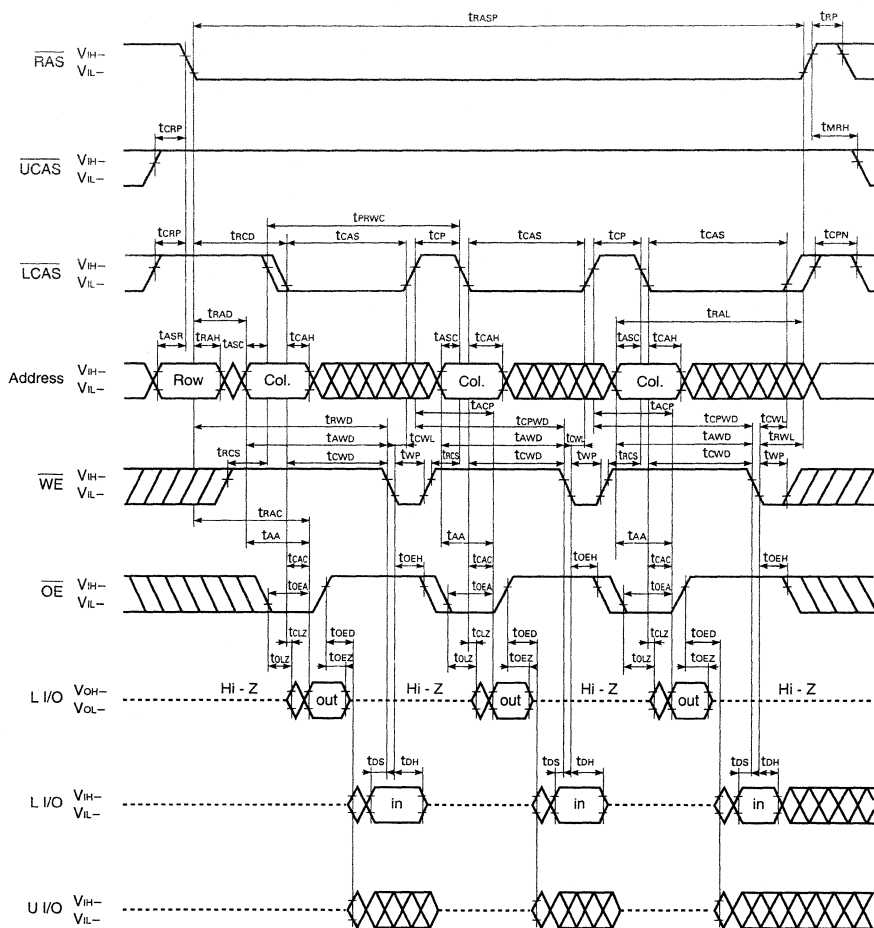
233

Fast Page Mode Upper Byte Read Modify Write Cycle



Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

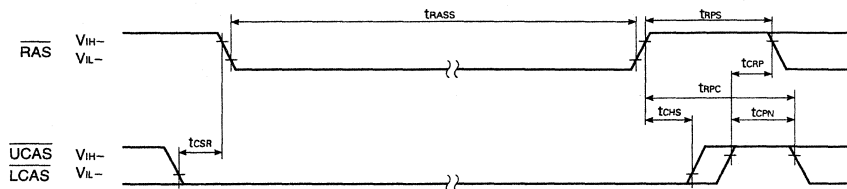
Fast Page Mode Lower Byte Read Modify Write Cycle



Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle (Only for the μ PD42S16160, 42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

★ **Cautions on Use of CAS Before RAS Self Refresh**

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16160 : 4 096 times within a 64 ms interval

μ PD42S18160 : 1 024 times within a 16 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

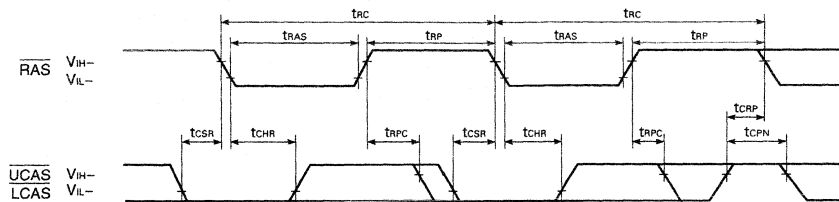
When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16160 : 4 096 times within a 64 ms interval

μ PD42S18160 : 1 024 times within a 16 ms interval

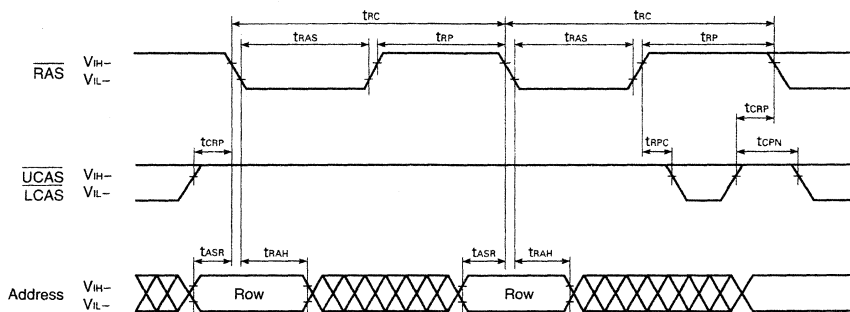
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



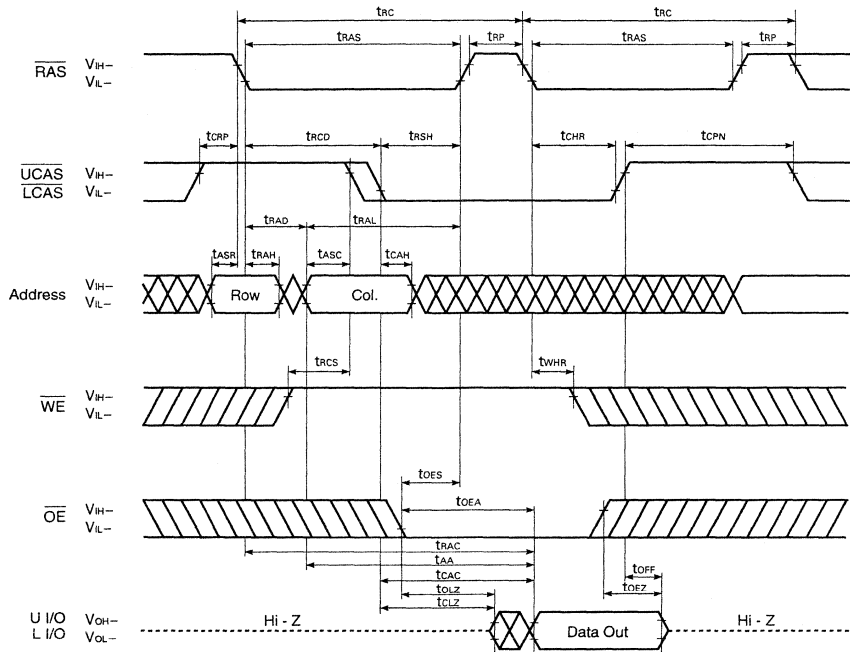
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

RAS Only Refresh Cycle

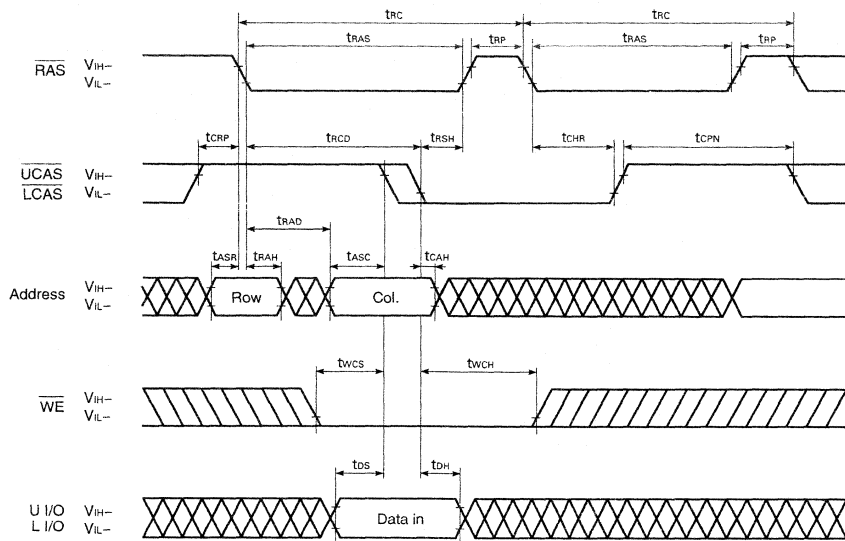


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Hidden Refresh Cycle (Read)



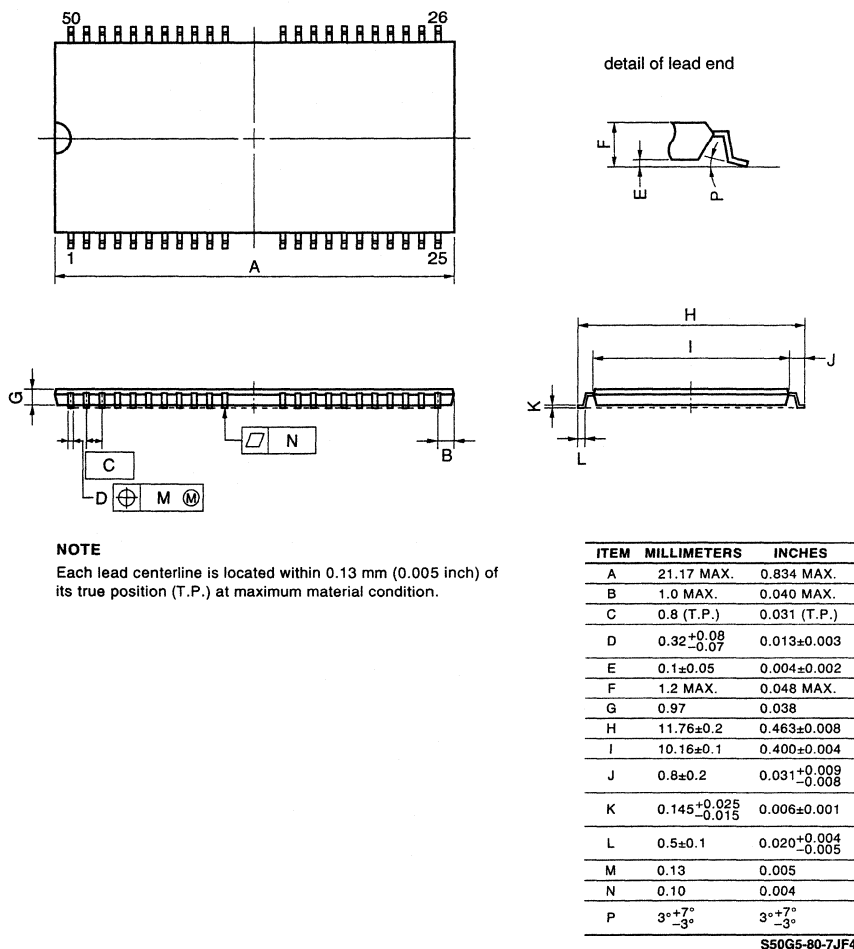
Hidden Refresh Cycle (Write)



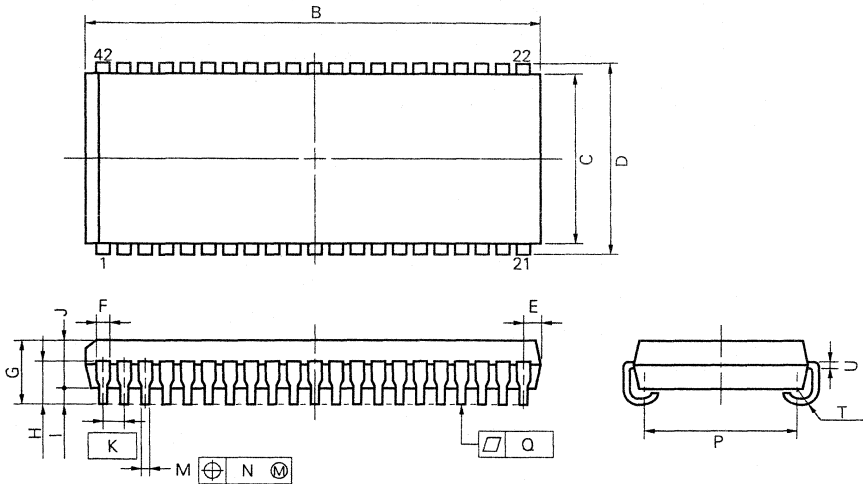
Remark $\overline{OE}$: Don't care

★ Package Drawings

50PIN PLASTIC TSOP(II) (400 mil)



42 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P42LE-400A

ITEM	MILLIMETERS	INCHES
B	27.56 ^{+0.2} _{-0.35}	1.085 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

★ Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met when soldering μPD42S16160, 4216160, 42S18160, 4218160.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16160G5, 4216160G5, 42S18160G5, 4218160G5 : 50-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limitNote : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing residual flux with water after the first reflow process.	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limitNote : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing residual flux with water after the first reflow process.	VP15-107-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μ PD42S16160LE, 4216160LE, 42S18160LE, 4218160LE : 42-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit Note : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit Note : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.
 Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

16 M-BIT DYNAMIC RAM**1 M-WORD BY 16-BIT, HYPER PAGE MODE, BYTE READ/WRITE MODE****Description**

The μ PD4216165 is a 1 048 576 words by 16 bits dynamic CMOS RAM with optional hyper page mode.

Hyper page mode is a kind of the page mode and is useful for the read operation.

The μ PD4216165 is packed in 50-pin plastic TSOP(III) and 42-pin plastic SOJ.

Features

- Hyper page mode
- 1 048 576 words by 16 bits organization
- Single +5.0 V $\pm$ 10 % power supply
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 4 096 refresh cycles/64 ms

Part number	Access time (MAX.)	R / W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μ PD4216165-50	50 ns	84 ns	20 ns
μ PD4216165-60	60 ns	104 ns	25 ns
μ PD4216165-70	70 ns	124 ns	30 ns

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD4216165G5-50-7JF	50 ns	50-pin Plastic TSOP(II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4216165G5-60-7JF	60 ns		
μ PD4216165G5-70-7JF	70 ns		
μPD4216165G5-50-7KF	50 ns	50-pin Plastic TSOP(II) (400 mil) Reverse bent	
μPD4216165G5-60-7KF	60 ns		
μPD4216165G5-70-7KF	70 ns		
μ PD4216165LE-50	50 ns	42-pin Plastic SOJ (400 mil)	
μ PD4216165LE-60	60 ns		
μ PD4216165LE-70	70 ns		

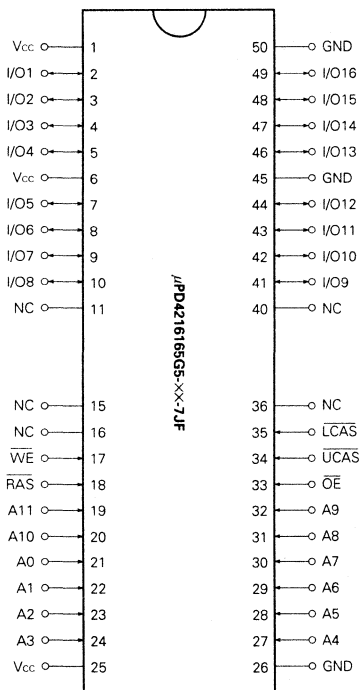
Quality Grade**Standard**

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number 1E1-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

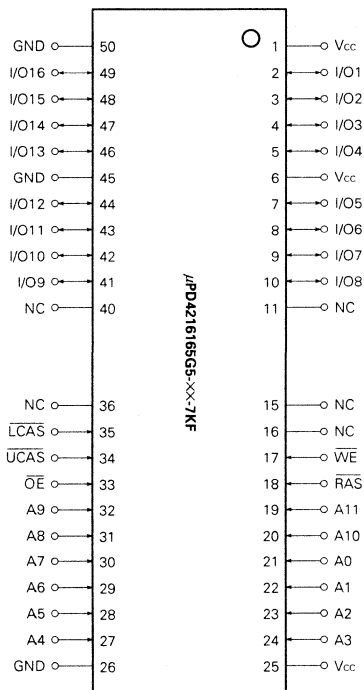
The information in this document is subject to change without notice.

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II) (400 mil)

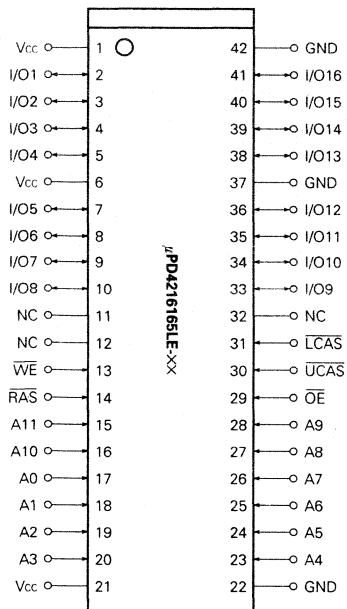


Reverse bent



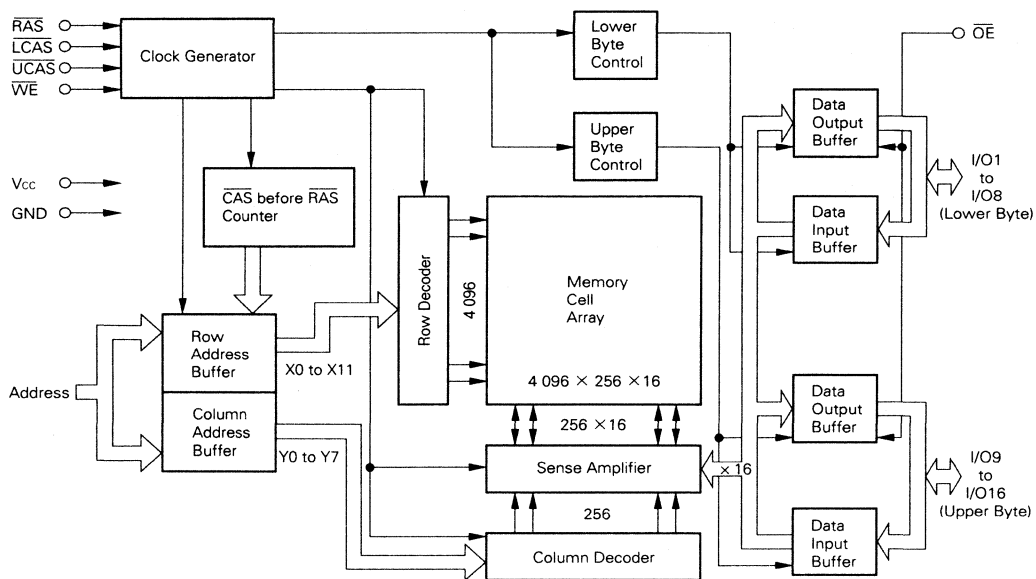
- A0 to A11 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{UCAS}}$: Column Address Strobe (upper)
- $\overline{\text{LCAS}}$: Column Address Strobe (lower)
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- V_{cc} : Power Supply
- GND : Ground
- NC : No Connection

42-pin Plastic SOJ (400 mil)



- A0 to A11 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
- LCAS : Column Address Strobe (lower)
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Input/Output Pin Functions

The μPD4216165 has input pins $\overline{RAS}$, $\overline{CAS}$ **Note**, $\overline{WE}$, $\overline{OE}$, A0 to A11 and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)		Address bus. Input total 20-bit of address signal, upper 12-bit and lower 8 -bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Electrical Specifications

- CAS means UCAS and LCAS.
- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

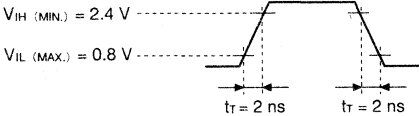
Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current	I _{CC1}	RAS, CAS Cycling			110	mA	1, 2, 3
		t _{RC} = t _{RC} (MIN.)			100		
		I _O = 0 mA			90		
Standby current	I _{CC2}	RAS, CAS $\geq V_{IH}$ (MIN.), I _O = 0 mA			2	mA	
		RAS, CAS $\geq V_{CC} - 0.2$ V, I _O = 0 mA			1		
RAS only refresh current	I _{CC3}	RAS Cycling, CAS $\geq V_{IH}$ (MIN.)			110	mA	1,2,3,4
		t _{RC} = t _{RC} (MIN.), I _O = 0 mA			100		
					90		
Operating current (Hyper page mode)	I _{CC4}	RAS $\leq V_{IL}$ (MAX.), CAS Cycling			120	mA	1, 2, 5
		t _{HPC} = t _{HPC} (MIN.), I _O = 0 mA			110		
					100		
CAS before RAS refresh current	I _{CC5}	RAS Cycling			110	mA	1, 2
		t _{RC} = t _{RC} (MIN.)			100		
		I _O = 0 mA			90		
Input leakage current	I _I (L)	V _I = 0 to 5.5 V All other pins not under test = 0 V	-10		+10	μ A	
Output leakage current	I _O (L)	V _O = 0 to 5.5 V Output is disabled (Hi-Z)	-10		+10	μ A	
High level output voltage	V _{OH}	I _O = -2.5 mA	2.4			V	
Low level output voltage	V _{OL}	I _O = +2.1 mA			0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during RAS $\leq V_{IL}$ (MAX.) and CAS $\geq V_{IH}$ (MIN.).
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

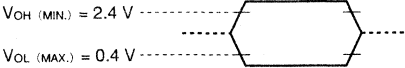
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{RC}	84	—	104	—	124	—	ns	
RAS Precharge Time	t _{RP}	30	—	40	—	50	—	ns	
CAS Precharge Time	t _{CPN}	7	—	10	—	10	—	ns	
RAS Pulse Width	t _{RAS}	50	10 000	60	10 000	70	10 000	ns	
CAS Pulse Width	t _{CAS}	7	10 000	10	10 000	12	10 000	ns	
RAS Hold Time	t _{RSH}	7	—	10	—	12	—	ns	
CAS Hold Time	t _{CSH}	35	—	40	—	50	—	ns	
RAS to CAS Delay Time	t _{RCD}	11	37	14	45	14	52	ns	1
RAS to Column Address Delay Time	t _{RAD}	9	25	12	30	12	35	ns	1
CAS to RAS Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	2
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	7	—	10	—	10	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	7	—	10	—	12	—	ns	
OE Lead Time Referenced to RAS	t _{OES}	0	—	0	—	0	—	ns	
CAS to Data Setup Time	t _{CLZ}	0	—	0	—	0	—	ns	
OE to Data Setup Time	t _{OLZ}	0	—	0	—	0	—	ns	
OE to Data Delay Time	t _{OED}	10	—	13	—	15	—	ns	
Masked Byte Write Hold Time Referenced to RAS	t _{MRH}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t _T	1	50	1	50	1	50	ns	
Refresh Time	t _{REF}	—	64	—	64	—	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD}(MAX.)$ and $t_{RCD} \leq t_{RCD}(MAX.)$	$t_{RAC}(MAX.)$	$t_{RAC}(MAX.)$
$t_{RAD} > t_{RAD}(MAX.)$ and $t_{RCD} \leq t_{RCD}(MAX.)$	$t_{AA}(MAX.)$	$t_{RAD} + t_{AA}(MAX.)$
$t_{RCD} > t_{RCD}(MAX.)$	$t_{CAC}(MAX.)$	$t_{RCD} + t_{CAC}(MAX.)$

$t_{RAD}(MAX.)$ and $t_{RCD}(MAX.)$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}(MAX.)$ and $t_{RCD} \geq t_{RCD}(MAX.)$ will not cause any operation problems.

2. $t_{CRP}(MIN.)$ requirement is applied for RAS, CAS cycles preceded by any cycle.

Read Cycle

Parameter	Symbol	$t_{RAC} = 50\text{ ns}$		$t_{RAC} = 60\text{ ns}$		$t_{RAC} = 70\text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from RAS	t_{RAC}	–	50	–	60	–	70	ns	1
Access Time from CAS	t_{CAC}	–	13	–	15	–	18	ns	1
Access Time from Column Address	t_{AA}	–	25	–	30	–	35	ns	1
Access Time from OE	t_{OEA}	–	13	–	15	–	18	ns	
Column Address Lead Time Referenced to RAS	t_{RAL}	25	–	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to RAS	t_{RRH}	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to CAS	t_{RCH}	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from OE	t_{OEZ}	0	10	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD}(MAX.)$ and $t_{RCD} \leq t_{RCD}(MAX.)$	$t_{RAC}(MAX.)$	$t_{RAC}(MAX.)$
$t_{RAD} > t_{RAD}(MAX.)$ and $t_{RCD} \leq t_{RCD}(MAX.)$	$t_{AA}(MAX.)$	$t_{RAD} + t_{AA}(MAX.)$
$t_{RCD} > t_{RCD}(MAX.)$	$t_{CAC}(MAX.)$	$t_{RCD} + t_{CAC}(MAX.)$

$t_{RAD}(MAX.)$ and $t_{RCD}(MAX.)$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}(MAX.)$ and $t_{RCD} \geq t_{RCD}(MAX.)$ will not cause any operation problems.

2. Either $t_{RCH}(MIN.)$ or $t_{RRH}(MIN.)$ should be met in read cycles.
3. $t_{OEZ}(MAX.)$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	7	–	10	–	10	–	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	7	–	10	–	10	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	7	–	10	–	12	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	7	–	10	–	12	–	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	–	0	–	0	–	ns	
Data-in Setup Time	t _{DS}	0	–	0	–	0	–	ns	3
Data-in Hold Time	t _{DH}	7	–	10	–	10	–	ns	3

- Notes**
1. t_{WP(MIN.)} is applied for late write cycles or read modify write cycles. In early write cycles, t_{WCH(MIN.)} should be met.
 2. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS(MIN.)} and t_{DH(MIN.)} are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	107	–	133	–	157	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	64	–	77	–	89	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	27	–	32	–	37	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	39	–	47	–	54	–	ns	1

- Note**
1. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwd ≥ trwd(MIN.), tcwd ≥ tcwd(MIN.), tawd ≥ tawd(MIN.), and tcpwd ≥ tcpwd(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{HPC}	20	–	25	–	30	–	ns	
RAS Pulse Width	t _{RASP}	50	125 000	60	125 000	70	125 000	ns	
CAS Pulse Width	t _{HCAS}	7	10 000	10	10 000	12	10 000	ns	
CAS Precharge Time	t _{CP}	7	–	10	–	10	–	ns	
Access Time from CAS Precharge	t _{ACP}	–	27	–	35	–	40	ns	
CAS Precharge to WE Delay Time	t _{CPWD}	41	–	52	–	59	–	ns	1
RAS Hold Time from CAS Precharge	t _{RHCP}	27	–	35	–	40	–	ns	
Read Modify Write Cycle Time	t _{HPRWC}	52	–	66	–	75	–	ns	
Data Output Hold Time	t _{DHC}	5	–	5	–	5	–	ns	
Output Buffer Turn-off Delay from WE	t _{WEZ}	0	10	0	13	0	15	ns	2,3
WE Pulse Width	t _{WPZ}	7	–	10	–	10	–	ns	3
Output Buffer Turn-off Delay from RAS	t _{OFR}	0	10	0	13	0	15	ns	2,3
Output Buffer Turn-off Delay from CAS	t _{OFC}	0	10	0	13	0	15	ns	2,3

Notes 1. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$, and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)

$\overline{WE}$: inactive, $\overline{OE}$: active

t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)

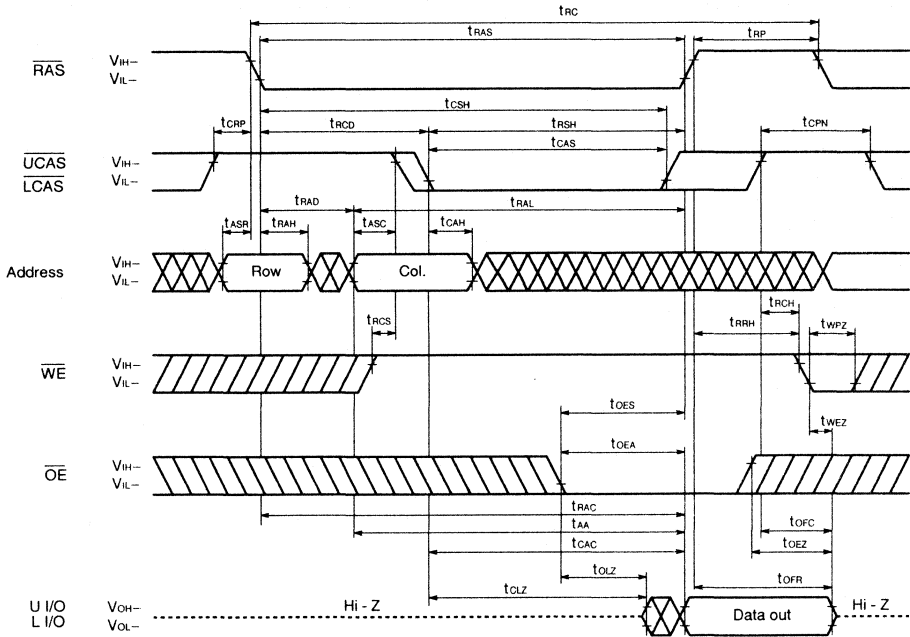
$\overline{WE}$: active, $\overline{OE}$: active ... t_{WEZ} , t_{WPZ} are effective.

$\overline{WE}$: inactive, $\overline{OE}$: inactive ... t_{OEZ} is effective.

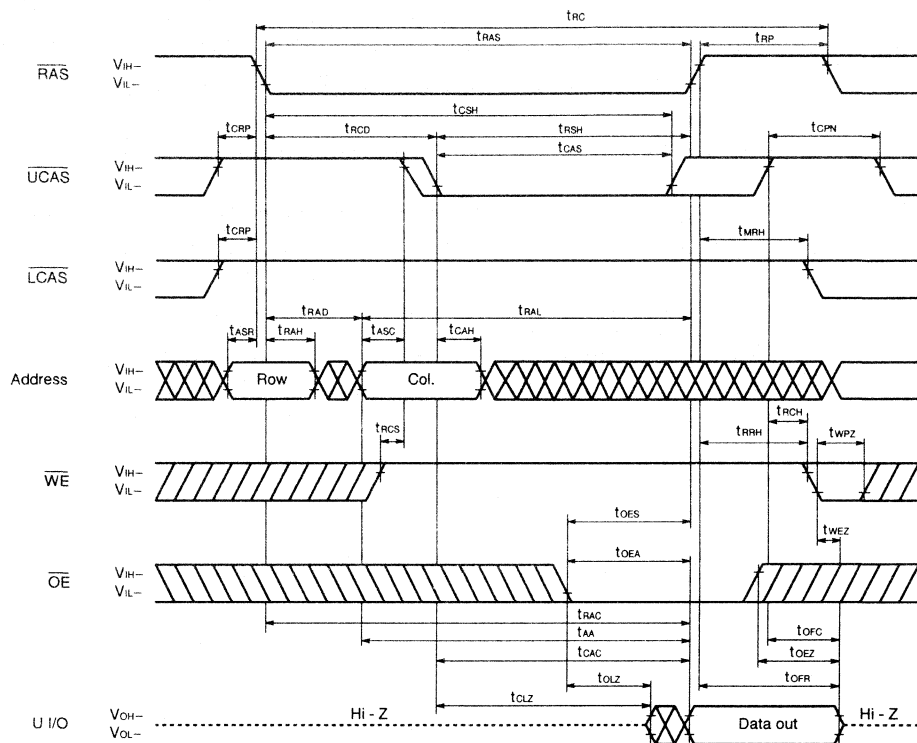
Refresh Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	–	5	–	5	–	ns	
CAS Hold Time ($\overline{CAS}$ before RAS Refresh)	t _{CHR}	10	–	10	–	10	–	ns	
RAS Precharge CAS Hold Time	t _{RPC}	5	–	5	–	5	–	ns	
WE Hold Time (Hidden Refresh Cycle)	t _{WHR}	15	–	15	–	15	–	ns	

Read Cycle

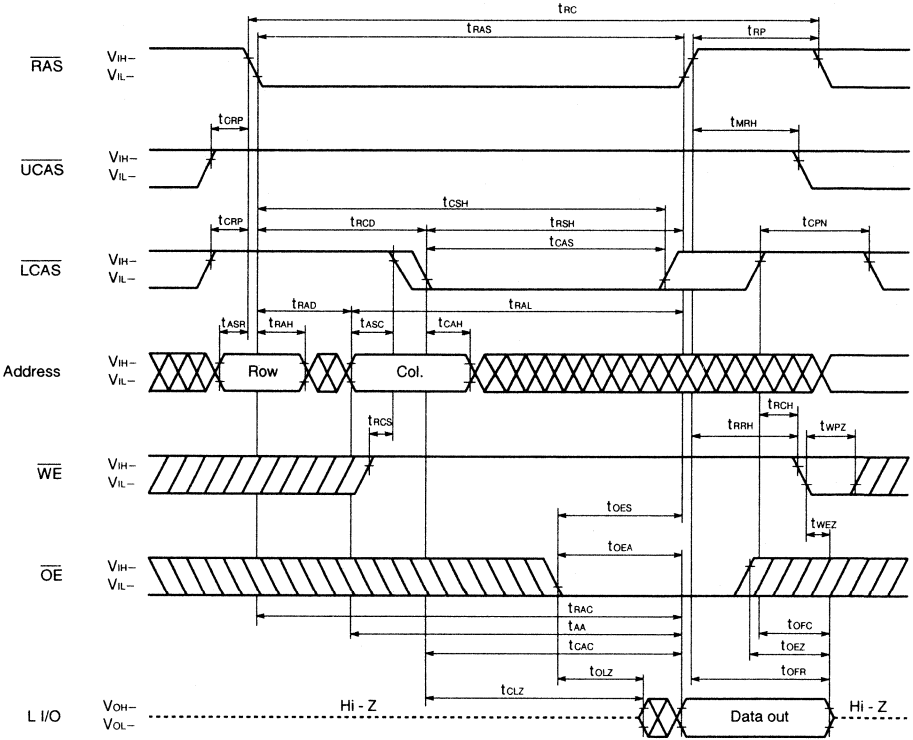


Upper Byte Read Cycle



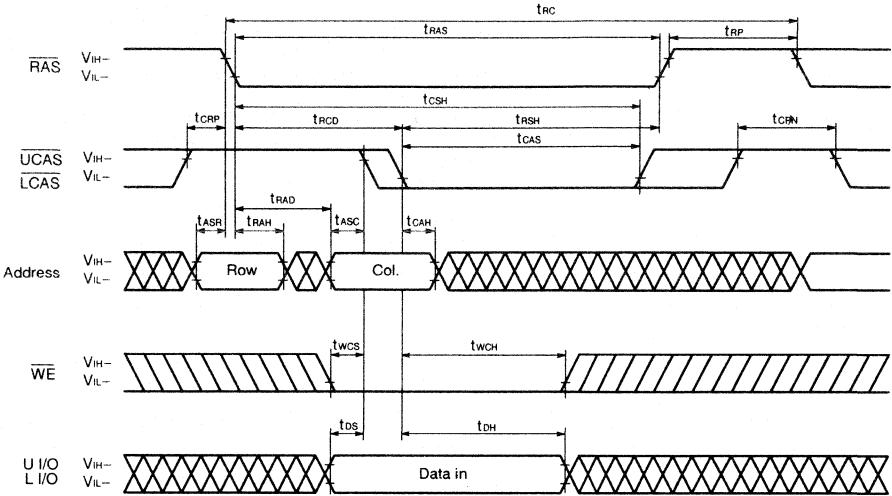
Remark L I/O : Hi-Z

Lower Byte Read Cycle



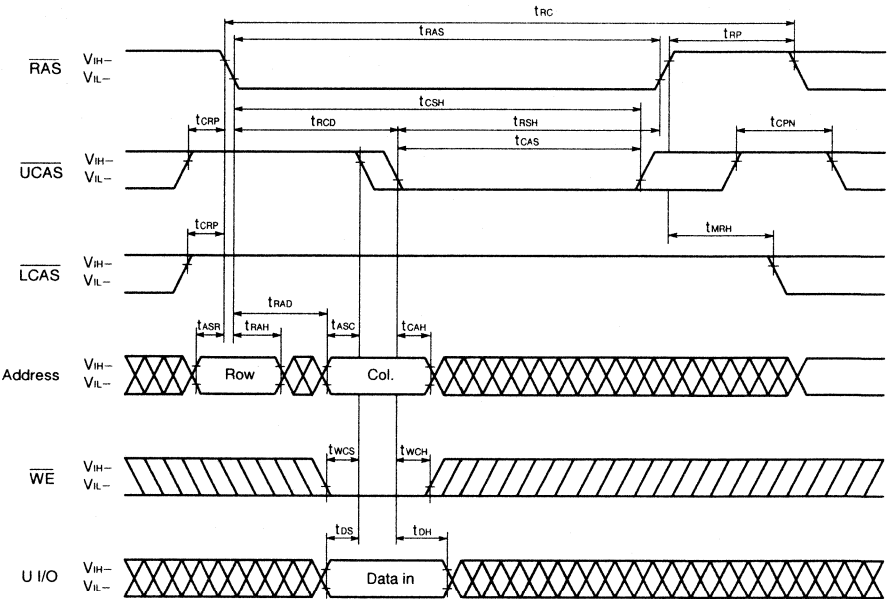
Remark U I/O : Hi-Z

Early Write Cycle



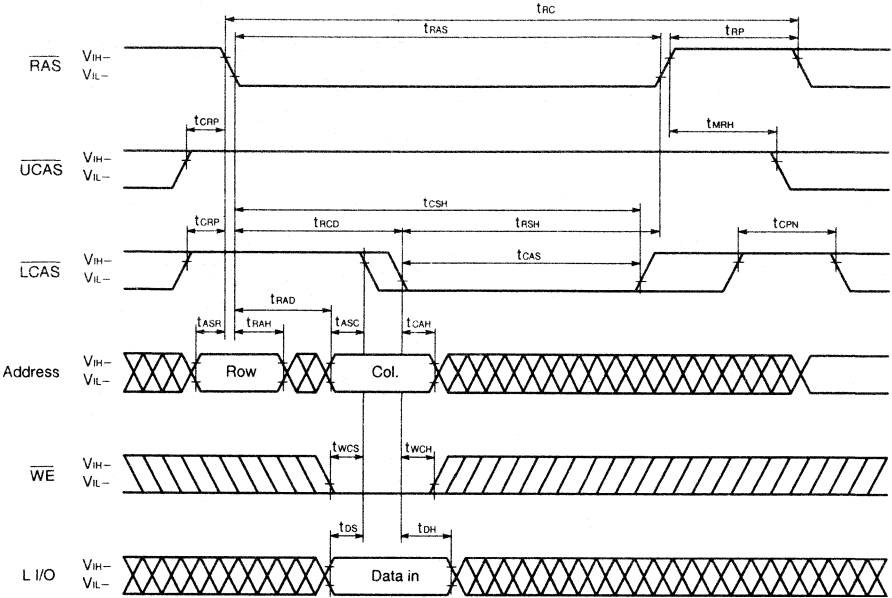
Remark $\overline{\text{OE}}$: Don't care

Upper Byte Early Write Cycle



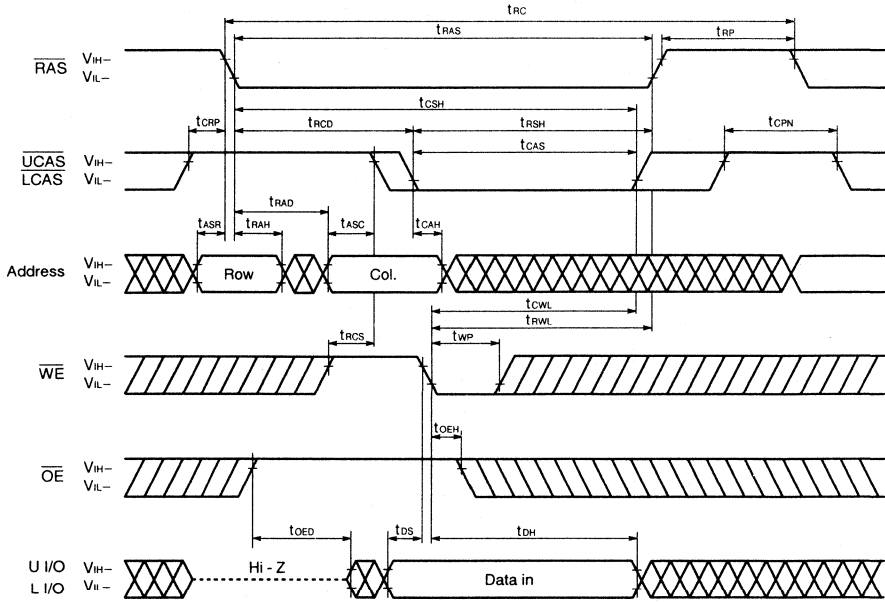
Remark $\overline{OE}$, L I/O : Don't care

Lower Byte Early Write Cycle

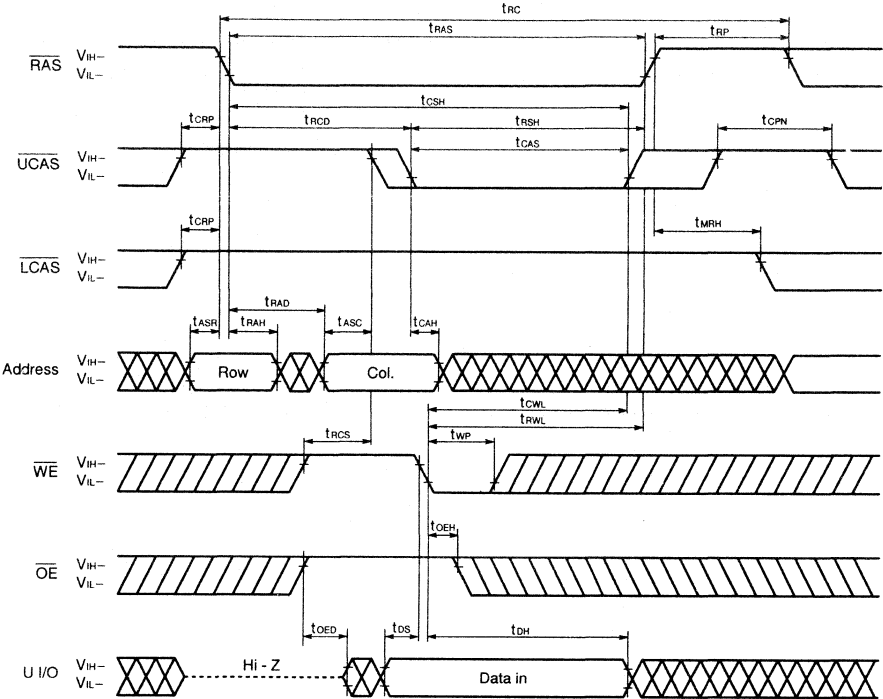


Remark $\overline{\text{OE}}$, U I/O : Don't care

Late Write Cycle

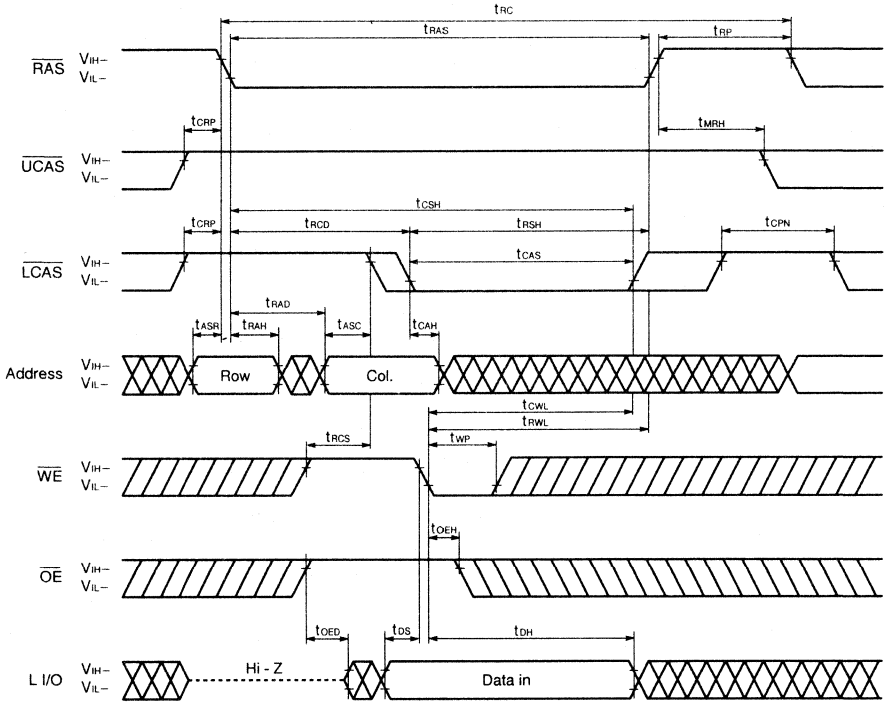


Upper Byte Late Write Cycle



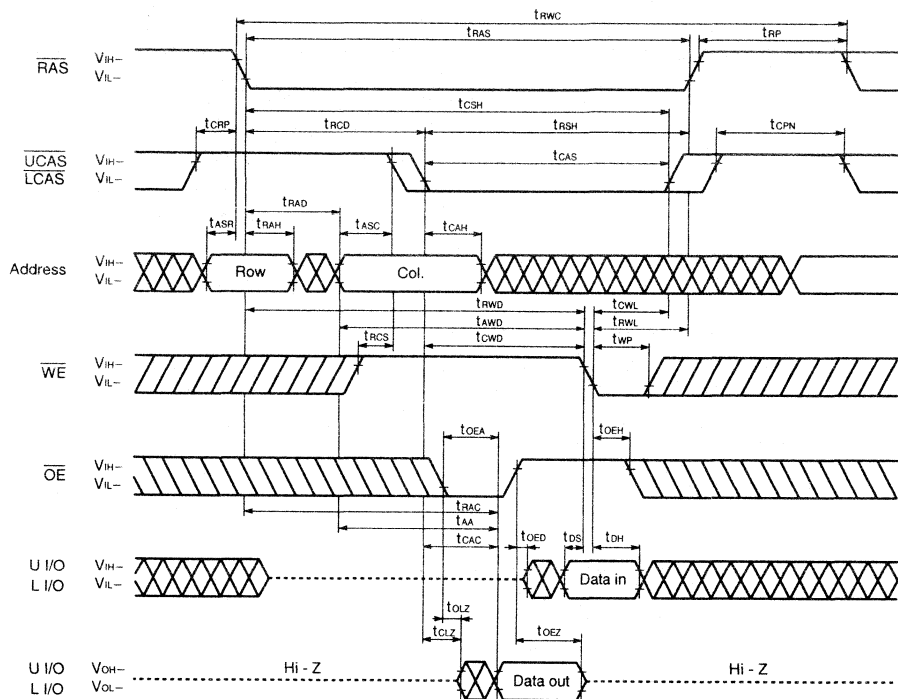
Remark L I/O : Don't care

Lower Byte Late Write Cycle

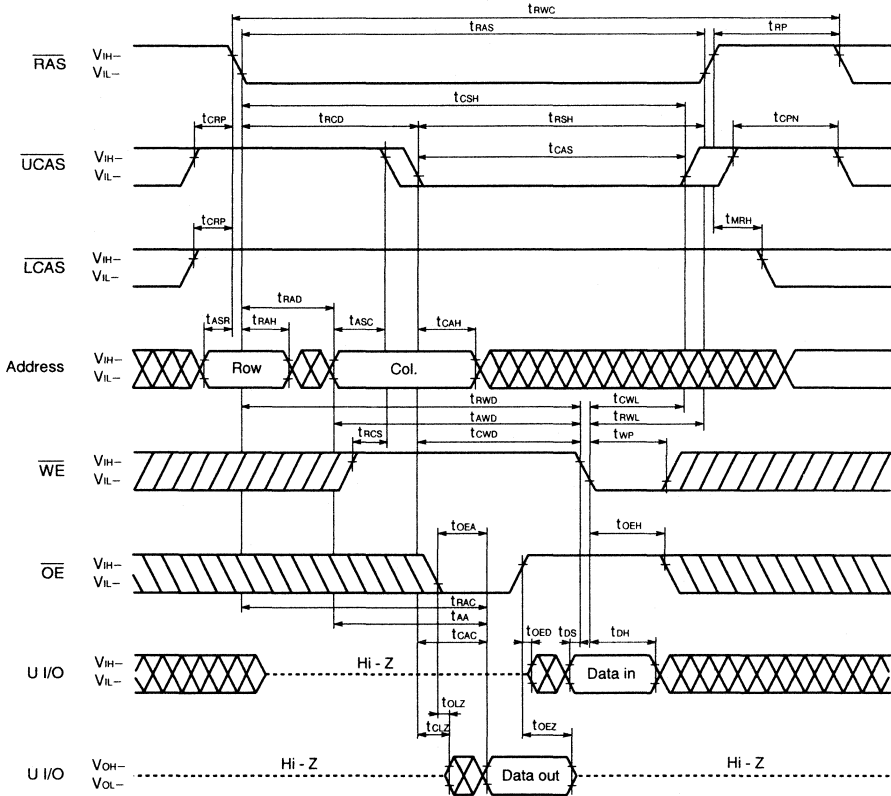


Remark U I/O : Don't care

Read Modify Write Cycle

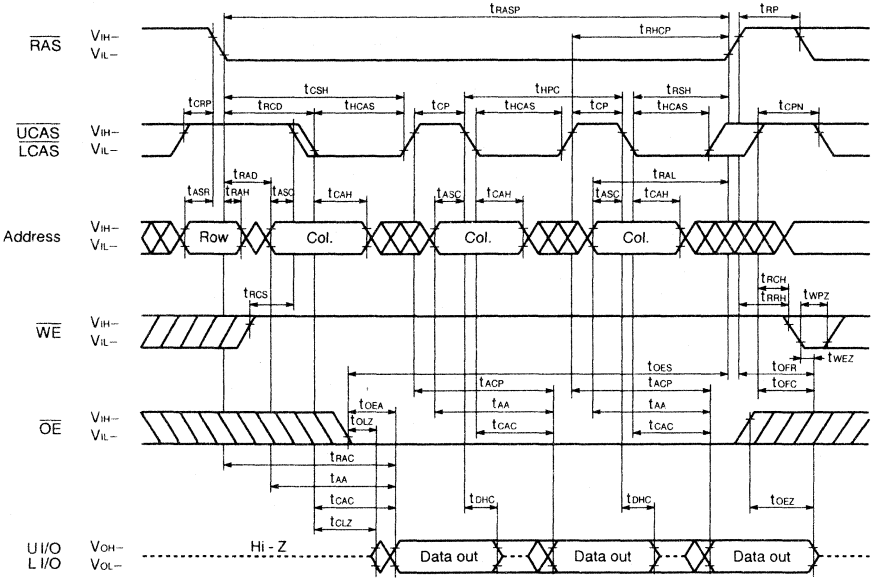


Upper Byte Read Modify Write Cycle

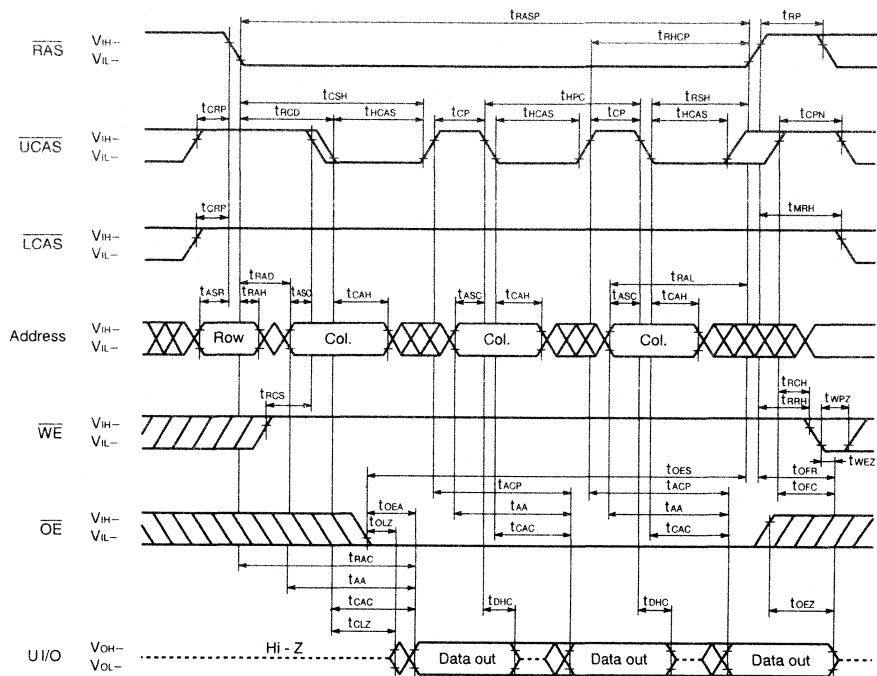


Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode Read Cycle

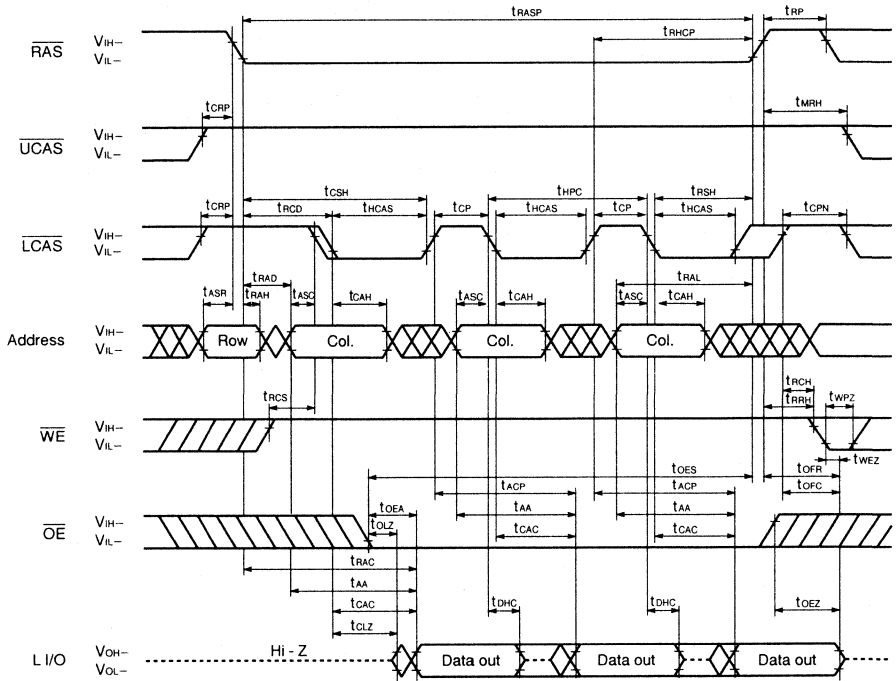


Hyper Page Mode Upper Byte Read Cycle



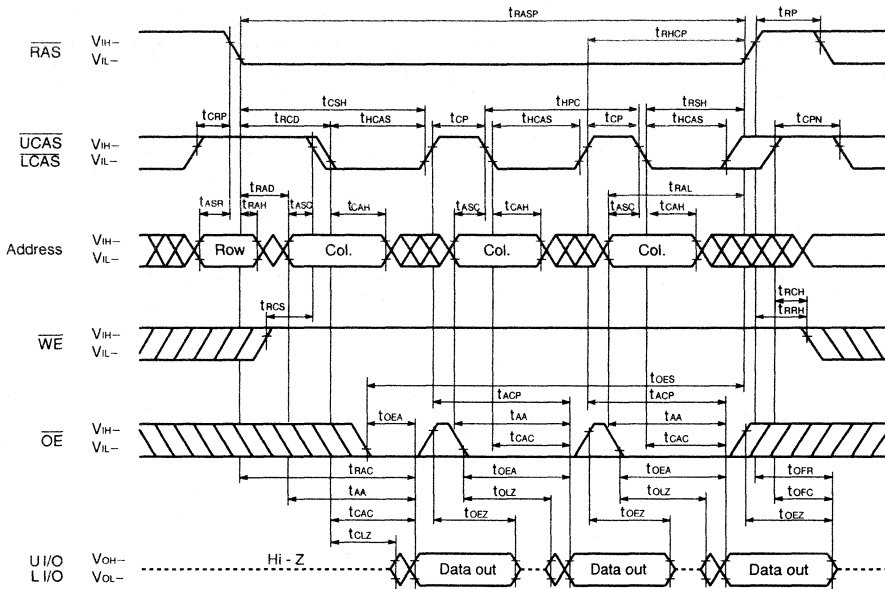
Remark L I/O : Hi-Z

Hyper Page Mode Lower Byte Read Cycle

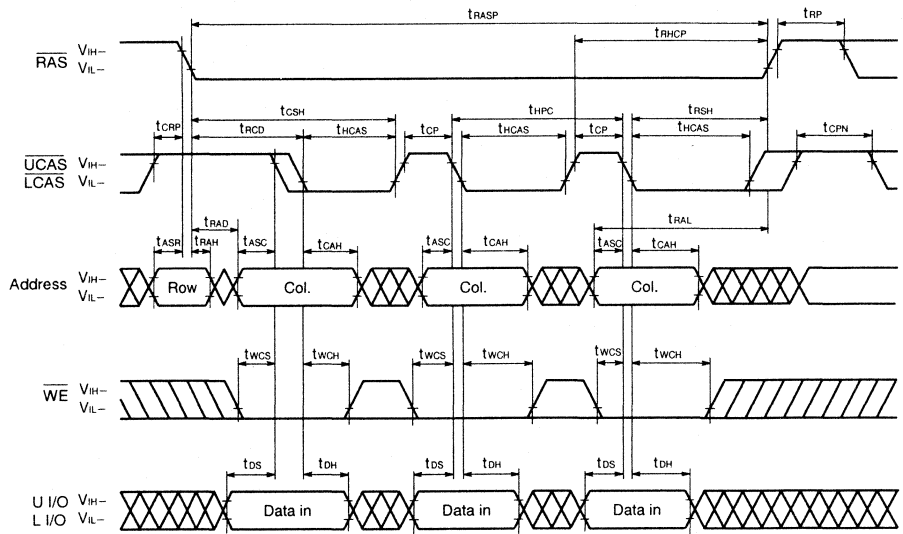


Remark U I/O : Hi-Z

Hyper Page Mode Read Cycle ($\overline{\text{OE}}$ Control)

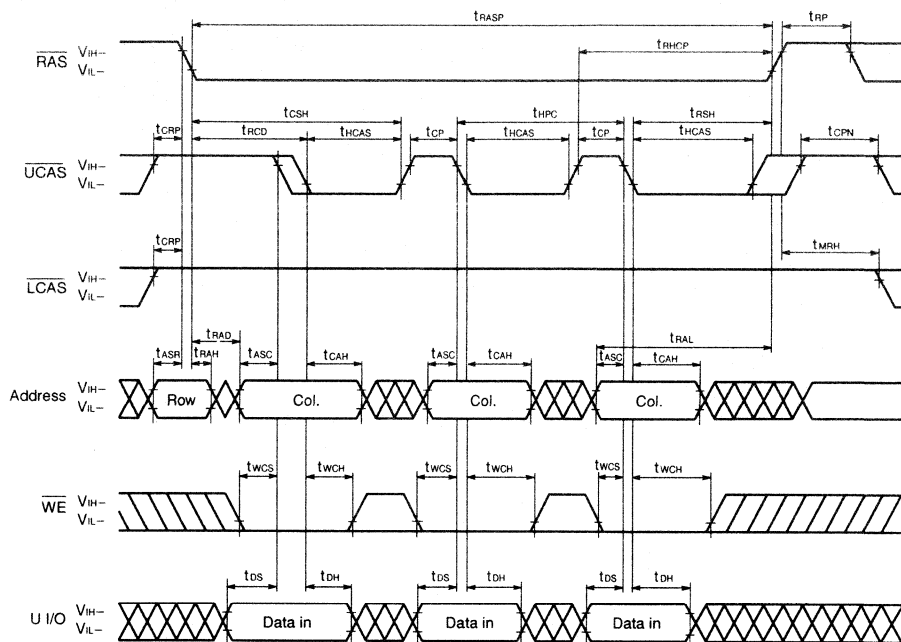


Hyper Page Mode Early Write Cycle



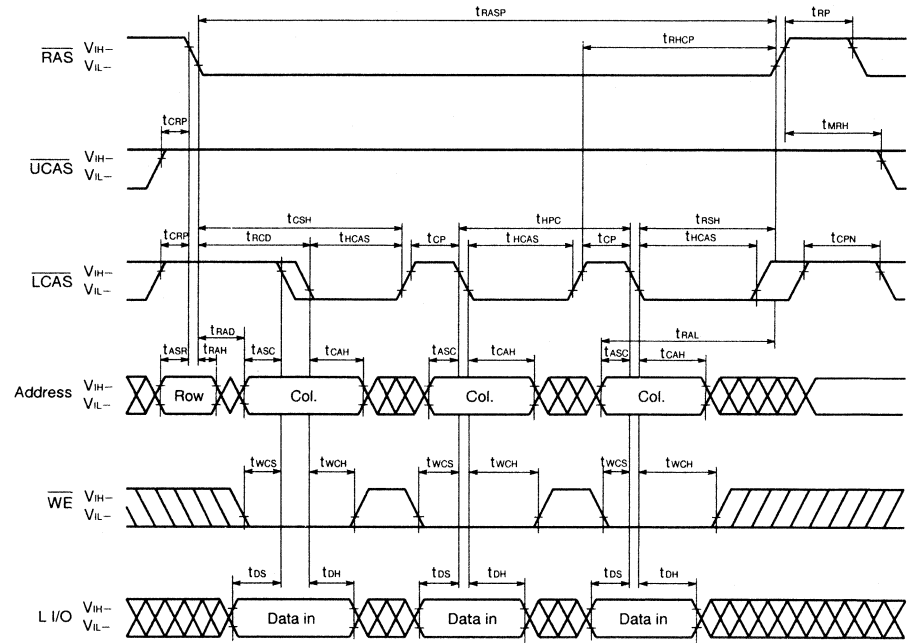
Remark $\overline{OE}$: Don't care

Hyper Page Mode Upper Byte Early Write Cycle



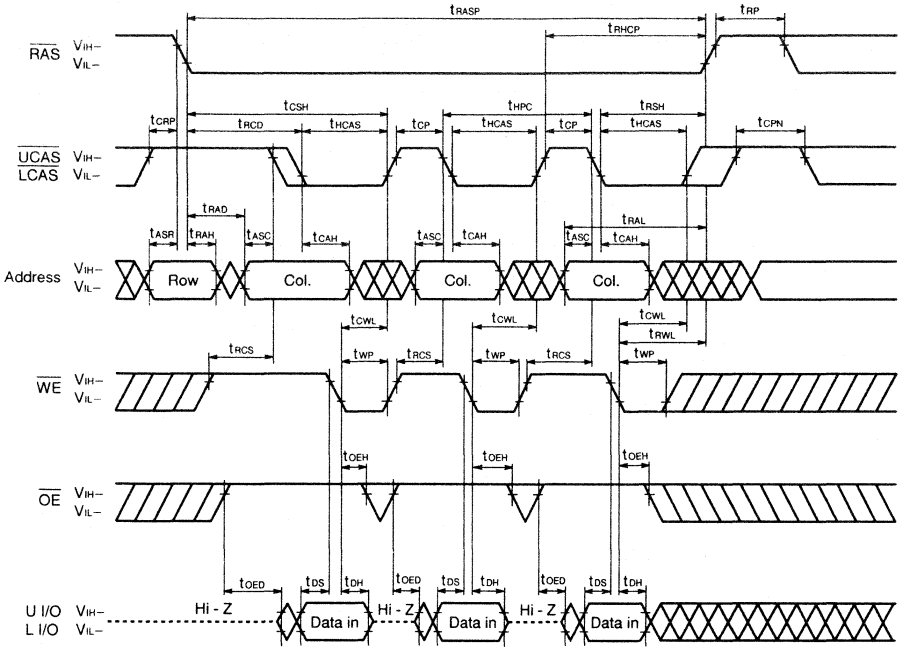
Remark $\overline{OE}$, L I/O : Don't care

Hyper Page Mode Lower Byte Early Write Cycle



Remark $\overline{OE}$, U I/O : Don't care

Hyper Page Mode Late Write Cycle



The diagram illustrates the timing relationships between several control and data signals during memory access operations. The signals shown are:

- RAS**: Row Address Strobe, active low.
- UCAS**: User Chip Address Strobe, active low.
- LCAS**: Local Chip Address Strobe, active low.
- Address**: Bus address signal, alternating between Row and Column addresses.
- WE**: Write Enable, active low.
- OE**: Output Enable, active low.
- L I/O**: Local Input/Output bus.
- U I/O**: User Input/Output bus.

Key timing parameters labeled include:

- t_{RASP} , t_{RHCP} , t_{RP}
- t_{CRP} , t_{CD} , t_{CAS} , t_{CP} , t_{HPC} , t_{SH} , t_{HCAS} , t_{CPN}
- t_{MRH}
- t_{RAD} , t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH} , t_{AL} , t_{CAH}
- t_{CWL} , t_{CS} , t_{WP} , t_{OEH} , t_{OED}
- t_{DS} , t_{DH}

Remark In this cycle, the input data to Lower I/O is ineffective.

The diagram illustrates the timing relationships between several control and data signals during memory access operations. The signals shown are:

- RAS**: Row Address Strobe, active low.
- UCAS**: User Chip Address Strobe, active low.
- LCAS**: Local Chip Address Strobe, active low.
- Address**: Bus address signal, alternating between Row and Column addresses.
- WE**: Write Enable, active low.
- OE**: Output Enable, active low.
- L/I/O**: Local/IO bus data signal.
- U/I/O**: User/IO bus data signal.

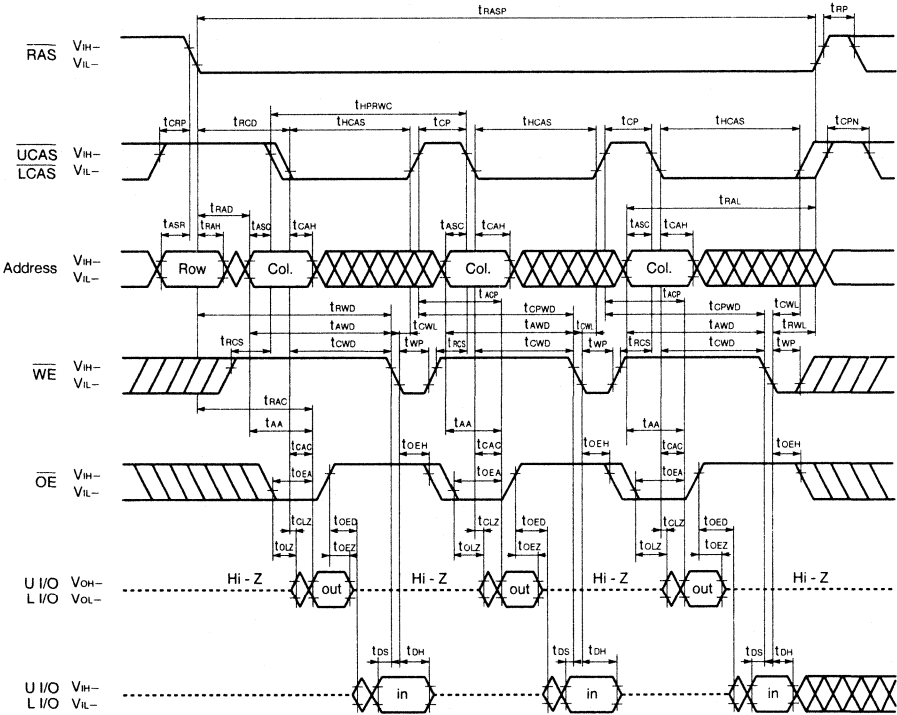
Key timing parameters labeled include:

- t_{RASP} , t_{RHCP} , t_{AP}
- t_{MRH}
- t_{CRP} , t_{CSH} , t_{HCAS} , t_{CP} , t_{HPC} , t_{ASH} , t_{CPN}
- t_{RAD} , t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH} , t_{TSC} , t_{TCAH} , t_{RAL} , t_{TCAH}
- t_{CWL} , t_{TRCS} , t_{WP} , t_{TOEH}
- t_{OED} , t_{OS} , t_{OH}

The diagram shows three distinct memory access cycles, each involving Row and Column address phases, followed by data transfer phases on the L/I/O and U/I/O buses.

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Hyper Page Mode Read Modify Write Cycle



[illegible]

Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

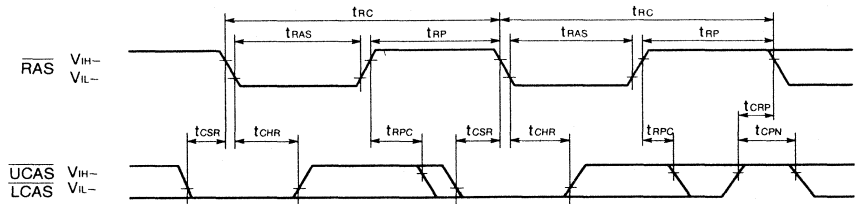
The timing diagram illustrates the sequence of signals for the 64K1602 LCD module. The signals and their timing parameters are as follows:

- RAS**: V_{IH} and V_{IL} levels. Timing parameters: t_{CRP} (RAS setup), t_{HPRWC} (RAS pulse width), t_{RCS} (RAS to column strobe delay), t_{RWD} (RAS to row write delay), t_{RWL} (RAS to row latch delay).
- UCAS**: V_{IH} and V_{IL} levels. Timing parameters: t_{CRP} (UCAS setup), t_{HPRWC} (UCAS pulse width), t_{RCS} (UCAS to column strobe delay), t_{RWD} (UCAS to row write delay), t_{RWL} (UCAS to row latch delay).
- LCAS**: V_{IH} and V_{IL} levels. Timing parameters: t_{CRP} (LCAS setup), t_{HPRWC} (LCAS pulse width), t_{RCS} (LCAS to column strobe delay), t_{RWD} (LCAS to row write delay), t_{RWL} (LCAS to row latch delay).
- Address**: V_{IH} and V_{IL} levels. Timing parameters: t_{RCS} (Address to column strobe delay), t_{RWD} (Address to row write delay), t_{RWL} (Address to row latch delay).
- WE**: V_{IH} and V_{IL} levels. Timing parameters: t_{RCS} (WE to column strobe delay), t_{RWD} (WE to row write delay), t_{RWL} (WE to row latch delay).
- OE**: V_{IH} and V_{IL} levels. Timing parameters: t_{RCS} (OE to column strobe delay), t_{RWD} (OE to row write delay), t_{RWL} (OE to row latch delay).
- L I/O**: V_{OH} and V_{OL} levels. Timing parameters: t_{RCS} (L I/O to column strobe delay), t_{RWD} (L I/O to row write delay), t_{RWL} (L I/O to row latch delay).
- U I/O**: V_{IH} and V_{IL} levels. Timing parameters: t_{RCS} (U I/O to column strobe delay), t_{RWD} (U I/O to row write delay), t_{RWL} (U I/O to row latch delay).

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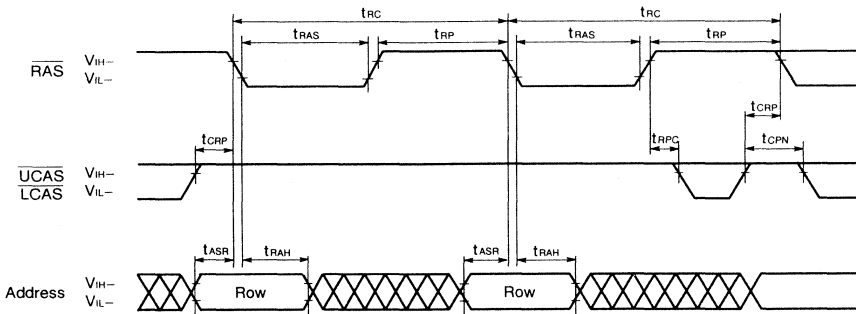
[illegible]

CAS Before RAS Refresh Cycle



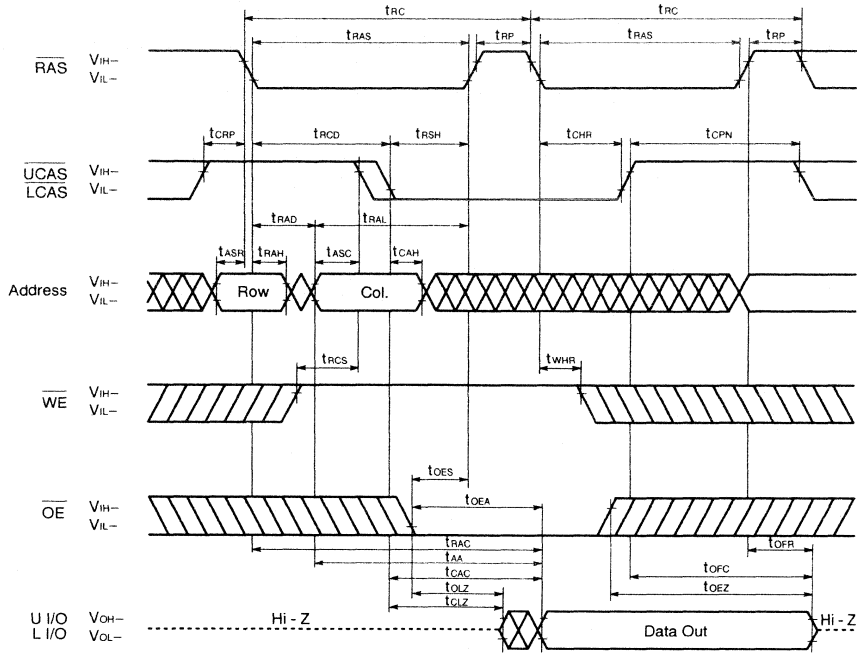
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

RAS Only Refresh Cycle

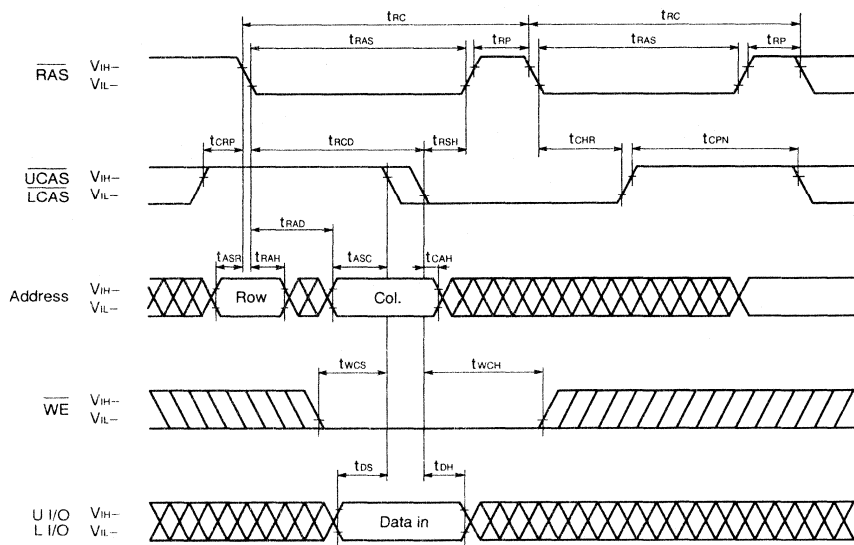


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Hidden Refresh Cycle (Read)



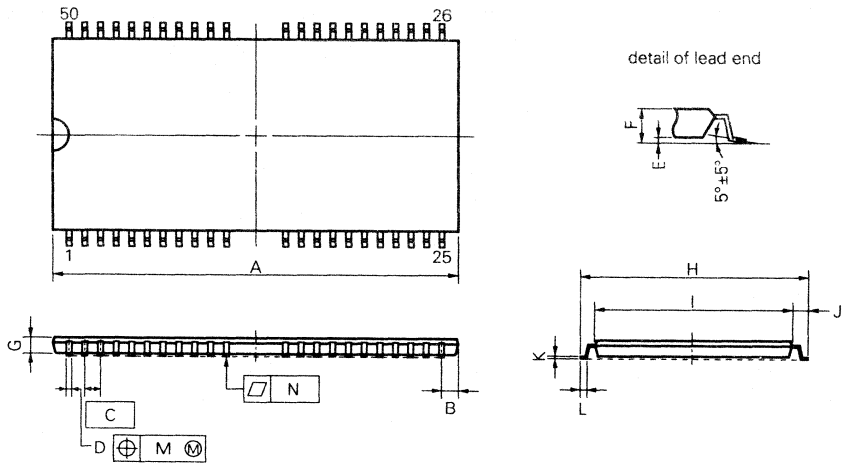
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

50 PIN PLASTIC TSOP(II) (400 mil)



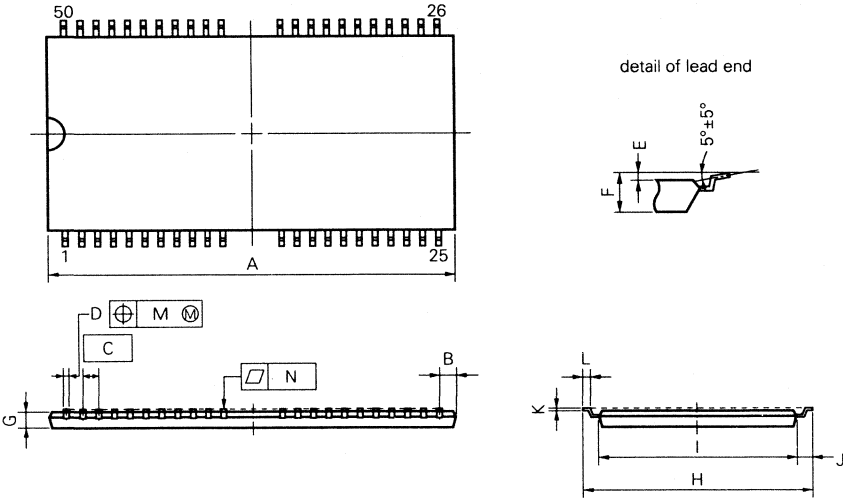
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S50G5-80-7JF-1

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004

50 PIN PLASTIC TSOP(II) (400 mil)



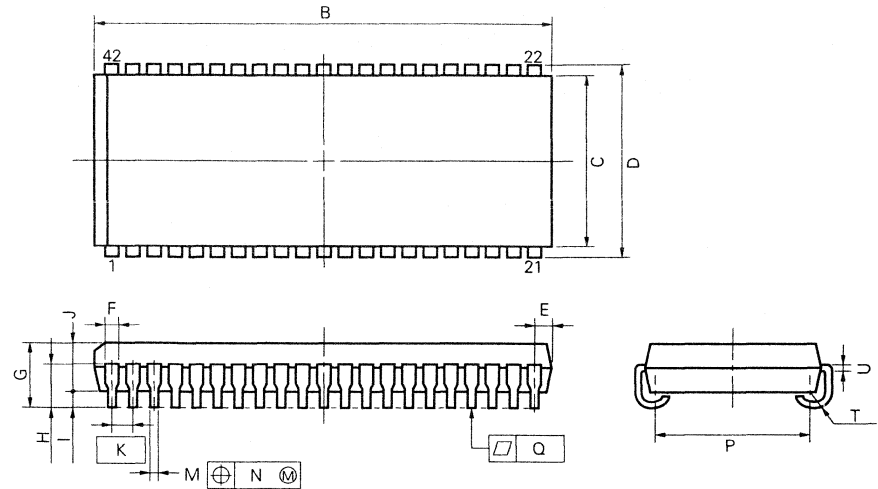
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S50G5-80-7KF-1

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004

42 PIN PLASTIC SOJ (400 mil)



P42LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	27.56 ^{+0.2} _{-0.35}	1.085 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD4216165.

Type of Surface Mount Device

μ PD4216165G5 : 50-pin Plastic TSOP (II) (400 mil)

μ PD4216165LE : 42-pin Plastic SOJ (400 mil)

16M Dynamic RAM

[3.3V $\pm$ 0.3V]



MOS INTEGRATED CIRCUIT

μ PD42S16400L, 4216400L, 42S17400L, 4217400L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM

4 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μ PD42S16400L, 4216400L, 42S17400L, 4217400L are 4 194 304 words by 4 bits dynamic CMOS RAMs.

These differ in refresh cycle and the μ PD42S16400L, 42S17400L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (see the table below).

These are packed in 26-pin plastic TSOP (II) and 26-pin plastic SOJ.

Features

- 4 194 304 words by 4 bits organization
- Single +3.3 V ± 0.3 V power supply
- Fast page mode
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S16400L-A60, 4216400L-A60	288 mW	60 ns	110 ns	40 ns
μ PD42S17400L-A60, 4217400L-A60	360 mW			
μ PD42S16400L-A70, 4216400L-A70	252 mW	70 ns	130 ns	45 ns
μ PD42S17400L-A70, 4217400L-A70	324 mW			
μ PD42S16400L-A80, 4216400L-A80	216 mW	80 ns	150 ns	50 ns
μ PD42S17400L-A80, 4217400L-A80	288 mW			

- The μ PD42S16400L, μ PD42S17400L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S16400L	4 096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μ PD42S17400L	2 048 cycles/128 ms		
μ PD4216400L	4 096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)
μ PD4217400L	2 048 cycles/32 ms		

The information in this document is subject to change without notice.

The mark ★ shows revised points.

★ Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD42S16400LG3-A60-7JD	60 ns	26-pin plastic TSOP(II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S17400LG3-A60-7JD			
μPD42S16400LG3-A70-7JD	70 ns		
μPD42S17400LG3-A70-7JD			
μPD42S16400LG3-A80-7JD	80 ns		
μPD42S17400LG3-A80-7JD			
μPD42S16400LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD42S17400LLA-A60			
μPD42S16400LLA-A70	70 ns		
μPD42S17400LLA-A70			
μPD42S16400LLA-A80	80 ns		
μPD42S17400LLA-A80			
μPD4216400LG3-A60-7JD	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD4217400LG3-A60-7JD			
μPD4216400LG3-A70-7JD	70 ns		
μPD4217400LG3-A70-7JD			
μPD4216400LG3-A80-7JD	80 ns		
μPD4217400LG3-A80-7JD			
μPD4216400LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD4217400LLA-A60			
μPD4216400LLA-A70	70 ns		
μPD4217400LLA-A70			
μPD4216400LLA-A80	80 ns		
μPD4217400LLA-A80			

Quality Grade

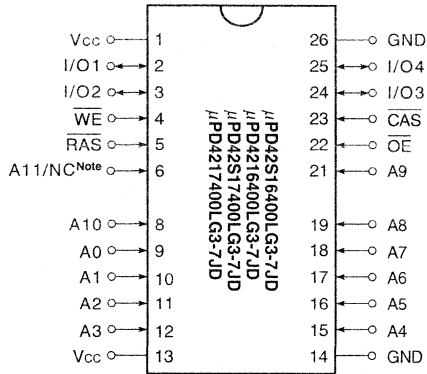
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

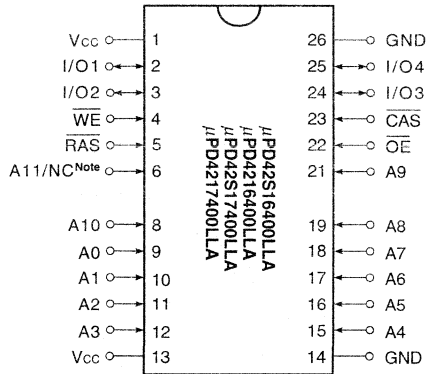
Pin Configurations (Marking Side)



26-pin Plastic TSOP (II) (300 mil)



26-pin Plastic SOJ (300 mil)

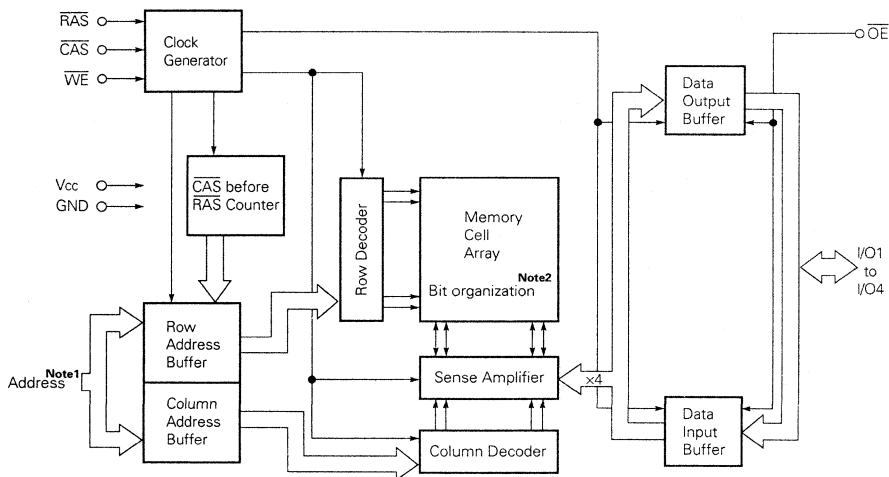


Note A11 ... μPD42S16400L, 4216400L

NC ... μPD42S17400L, 4217400L

- A0 to A11 : Address Inputs
- I/O1 to I/O4 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S16400L, 4216400L	A0 to A11	A0 to A9
μPD42S17400L, 4217400L	A0 to A10	A0 to A10

2. μPD42S16400L...4 096 × 1 024 × 4 μPD42S17400L...2 048 × 2 048 × 4

Input/Output Pin Functions

The μ PD42S16400L, 4216400L, 42S17400L, 4217400L have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11/A10^{Note1} and input/output pins I/O1 to I/O4.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • CAS before RAS refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11/A10 ^{Note1} (Address inputs)		Address bus. Input total 22-bit of address signal, upper 12/11 ^{Note2} -bit and lower 10/11 ^{Note3} -bit in sequence (address multiplex method). Therefore, one word is selected from 4 194 304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t _{ASR} , t _{ASC}) and hold time (t _{RAH} , t _{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/ Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

- Notes**
1. A11... μ PD42S16400L, 4216400L A10... μ PD42S17400L, 4217400L
 2. 12... μ PD42S16400L, 4216400L 11... μ PD42S17400L, 4217400L
 3. 10... μ PD42S16400L, 4216400L 11... μ PD42S17400L, 4217400L

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-0.5 to +4.6	V
Supply Voltage	V_{CC}		-0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low Level Input Voltage	V_{IL}		-0.3		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

[μ PD42S16400L, 4216400L]

Parameter		Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	RAS, CAS Cycling trc = trc(MIN.) I _O = 0 mA	trac = 60 ns		80	mA	1, 2, 3
				trac = 70 ns		70		
				trac = 80 ns		60		
Standby current	μ PD42S16400L	I _{CC2}	RAS, CAS $\geq V_{IH(MIN.)}$, I _O = 0 mA			0.5	mA	
			RAS, CAS $\geq V_{CC} - 0.2$ V, I _O = 0 mA			0.15		
	μ PD4216400L		RAS, CAS $\geq V_{IH(MIN.)}$, I _O = 0 mA			2		
			RAS, CAS $\geq V_{CC} - 0.2$ V, I _O = 0 mA			0.5		
RAS only refresh current		I _{CC3}	RAS Cycling, CAS $\geq V_{IH(MIN.)}$ trc = trc(MIN.), I _O = 0 mA	trac = 60 ns		80	mA	1, 2, 3, 4
				trac = 70 ns		70		
				trac = 80 ns		60		
Operating current (Fast page mode)		I _{CC4}	RAS $\leq V_{IL(MAX.)}$, CAS Cycling tpc = tpc(MIN.), I _O = 0 mA	trac = 60 ns		70	mA	1, 2, 5
				trac = 70 ns		60		
				trac = 80 ns		50		
CAS before RAS refresh current		I _{CC5}	RAS Cycling trc = trc(MIN.) I _O = 0 mA	trac = 60 ns		80	mA	1, 2
				trac = 70 ns		70		
				trac = 80 ns		60		
CAS before RAS long refresh current (4 096 Cycles / 128 ms, only for the μ PD42S16400L)		I _{CC6}	CAS before RAS refresh : 4 096 Cycles / 128 ms RAS, CAS : V _{CC} -0.2 V $\leq V_{IH} \leq V_{IH(MAX.)}$ 0 V $\leq V_{IL} \leq 0.2$ V Standby : RAS $\geq V_{CC}-0.2$ V Address : Don't care WE, OE : V _{IH} I _O = 0 mA	tr _{AS} $\leq$ 1 μ s		220	μ A	1, 2
Self refresh current (CAS before RAS self refresh, only for the μ PD42S16400L)		I _{CC7}	RAS, CAS : V _{CC} -0.2 V $\leq V_{IH} \leq V_{IH(MAX.)}$ 0 V $\leq V_{IL} \leq 0.2$ V I _O = 0 mA			150	μ A	2
Input leakage current		I _{IL}	V _I = 0 to 3.6 V All other pins not under test = 0 V	-5		+5	μ A	
Output leakage current		I _{OL}	V _O = 0 to 3.6 V Output is disabled (Hi-Z)	-5		+5	μ A	
High level output voltage		V _{OH}	I _O = -2.0 mA	2.4			V	
Low level output voltage		V _{OL}	I _O = +2.0 mA			0.4	V	

[μ PD42S17400L, 4217400L]

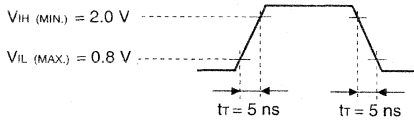
Parameter		Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling			100	mA	1, 2, 3
			$\text{trc} = \text{trc}(\text{MIN.})$			90		
			$\text{I}_\text{O} = 0 \text{ mA}$			80		
Standby current	μ PD42S17400L	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), \text{I}_\text{O} = 0 \text{ mA}$			0.5	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, \text{I}_\text{O} = 0 \text{ mA}$			0.15		
	μ PD4217400L		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), \text{I}_\text{O} = 0 \text{ mA}$			2		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, \text{I}_\text{O} = 0 \text{ mA}$			0.5		
RAS only refresh current		I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$			100	mA	1,2,3,4
			$\text{trc} = \text{trc}(\text{MIN.}), \text{I}_\text{O} = 0 \text{ mA}$			90		
						80		
Operating current (Fast page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling			70	mA	1, 2, 5
			$\text{tpc} = \text{tpc}(\text{MIN.}), \text{I}_\text{O} = 0 \text{ mA}$			60		
						50		
CAS before RAS refresh current		I _{CC5}	$\overline{\text{RAS}}$ Cycling			100	mA	1, 2
			$\text{trc} = \text{trc}(\text{MIN.})$			90		
			$\text{I}_\text{O} = 0 \text{ mA}$			80		
CAS before RAS long refresh current (2 048 Cycles / 128 ms, only for the μ PD42S17400L)		I _{CC6}	CAS before RAS refresh : 2 048 Cycles / 128 ms $\overline{\text{RAS}}, \overline{\text{CAS}}$: $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby : $\overline{\text{RAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : Don't care $\overline{\text{WE}}, \text{OE} : V_{\text{IH}}$ $\text{I}_\text{O} = 0 \text{ mA}$			200	μ A	1, 2
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for the μ PD42S17400L)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}$: $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $\text{I}_\text{O} = 0 \text{ mA}$			150	μ A	2
Input leakage current		I _{IL(L)}	$V_{\text{I}} = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V	-5		+5	μ A	
Output leakage current		I _{OL(L)}	$V_{\text{O}} = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)	-5		+5	μ A	
High level output voltage		V _{OH}	$\text{I}_\text{O} = -2.0 \text{ mA}$	2.4			V	
Low level output voltage		V _{OL}	$\text{I}_\text{O} = +2.0 \text{ mA}$			0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (trc and tpc).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

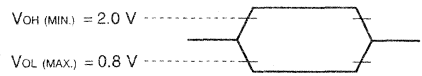
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	trac = 60 ns		trac = 70 ns		trac = 80 ns		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Read / Write Cycle Time	trc	110	–	130	–	150	–	ns		
RAS Precharge Time	trp	40	–	50	–	60	–	ns		
CAS Precharge Time	tcpn	10	–	10	–	10	–	ns		
RAS Pulse Width	tras	60	10 000	70	10 000	80	10 000	ns		
CAS Pulse Width	tcas	15	10 000	18	10 000	20	10 000	ns		
RAS Hold Time	trsh	15	–	18	–	20	–	ns		
CAS Hold Time	tcsH	60	–	70	–	80	–	ns		
RAS to CAS Delay Time	trcd	20	40	20	50	25	60	ns	1	
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	1	
CAS to RAS Precharge Time	tcpR	5	–	5	–	5	–	ns	2	
Row Address Setup Time	tasR	0	–	0	–	0	–	ns		
Row Address Hold Time	trah	10	–	10	–	12	–	ns		
Column Address Setup Time	tasc	0	–	0	–	0	–	ns		
Column Address Hold Time	tcaH	15	–	15	–	15	–	ns		
OE Lead Time Referenced to RAS	toes	0	–	0	–	0	–	ns		
CAS to Data Setup Time	tclZ	0	–	0	–	0	–	ns		
OE to Data Setup Time	tolZ	0	–	0	–	0	–	ns		
OE to Data Delay Time	toed	15	–	15	–	20	–	ns		
Transition Time (Rise and Fall)	tt	3	50	3	50	3	50	ns		
Refresh Time	μPD42S16400L, 42S17400L	tREF	–	128	–	128	–	128	ms	3
	μPD4216400L		–	64	–	64	–	64		
	μPD4217400L		–	32	–	32	–	32		

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
t _{RA} ≤ t _{RA} (MAX.) and t _{RC} ≤ t _{RC} (MAX.)	t _{RAC} (MAX.)	t _{RAC} (MAX.)
t _{RA} > t _{RA} (MAX.) and t _{RC} ≤ t _{RC} (MAX.)	t _{AA} (MAX.)	t _{RA} + t _{AA} (MAX.)
t _{RC} > t _{RC} (MAX.)	t _{CAC} (MAX.)	t _{RC} + t _{CAC} (MAX.)

t_{RA}(MAX.) and t_{RC}(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions t_{RA} ≥ t_{RA}(MAX.) and t_{RC} ≥ t_{RC}(MAX.) will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.
3. This specification is applied only to the μ PD42S16400L, 42S17400L.

Read Cycle

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		$t_{RAC} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	18	–	20	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	–	40	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	15	–	18	–	20	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	40	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	3
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi - Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
WE Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10	–	10	–	15	–	ns	1
WE Pulse Width	t _{WP}	10	–	10	–	15	–	ns	1
WE Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20	–	20	–	20	–	ns	
WE Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15	–	15	–	15	–	ns	
WE Setup Time	t _{WCS}	0	–	0	–	0	–	ns	2
OE Hold Time	t _{OEH}	0	–	0	–	0	–	ns	
Data-in Setup Time	t _{DS}	0	–	0	–	0	–	ns	3
Data-in Hold Time	t _{DH}	10	–	15	–	15	–	ns	3

- Notes**
1. t_{WP(MIN.)} is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH(MIN.)} should be met.
 2. If t_{WCS} ≥ t_{WCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle.
 3. t_{DS(MIN.)} and t_{DH(MIN.)} are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the WE falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t _{RWC}	160	–	180	–	205	–	ns	
$\overline{\text{RAS}}$ to WE Delay Time	t _{RWD}	85	–	95	–	110	–	ns	1
$\overline{\text{CAS}}$ to WE Delay Time	t _{CWD}	40	–	43	–	50	–	ns	1
Column Address to WE Delay Time	t _{AWD}	55	–	60	–	70	–	ns	1

- Note**
1. If t_{WCS} ≥ t_{WCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If t_{RWD} ≥ t_{RWD(MIN.)}, t_{CWD} ≥ t_{CWD(MIN.)}, t_{AWD} ≥ t_{AWD(MIN.)} and t_{CPWD} ≥ t_{CPWD(MIN.)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

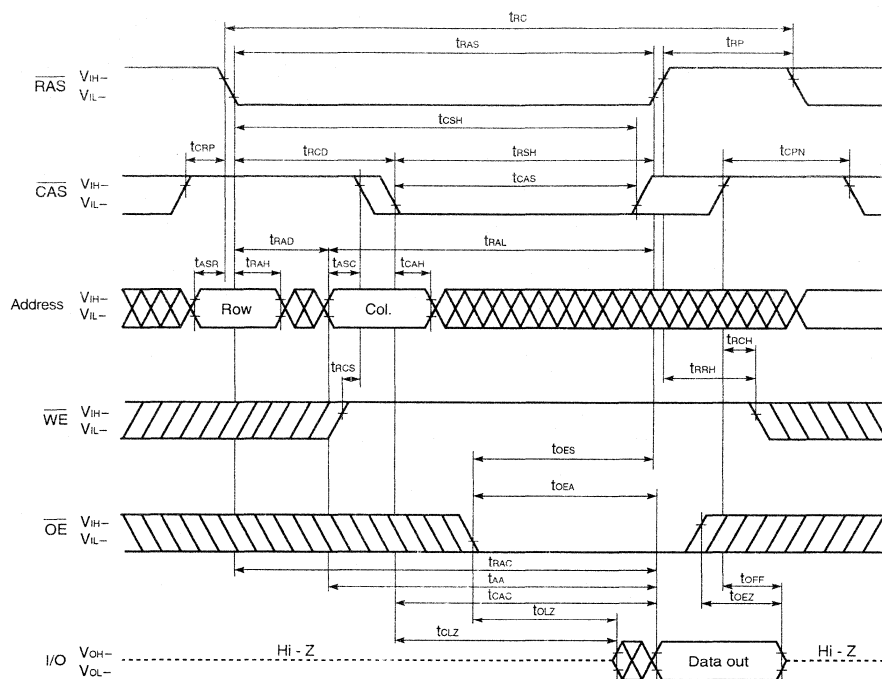
Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	TPC	40	–	45	–	50	–	ns	
Access Time from CAS Precharge	TACP	–	35	–	40	–	45	ns	
RAS Pulse Width	TRASP	60	125 000	70	125 000	80	125 000	ns	
CAS Precharge Time	TCP	10	–	10	–	10	–	ns	
RAS Hold Time from CAS Precharge	TRHCP	35	–	40	–	45	–	ns	
Read Modify Write Cycle Time	TPRWC	85	–	90	–	105	–	ns	
CAS Precharge to WE Delay Time	TCPWD	58	–	65	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$ and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

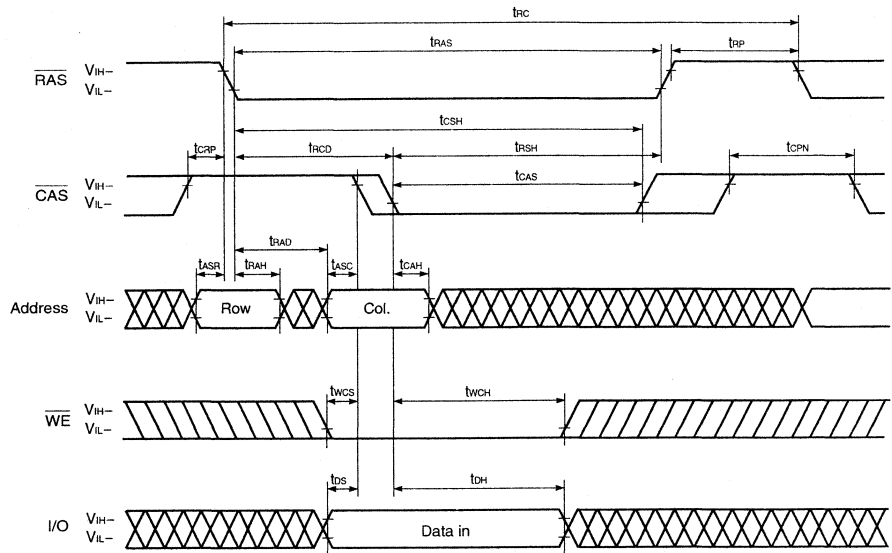
Refresh Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	TCSR	5	–	5	–	5	–	ns	
CAS Hold Time (CAS before RAS Refresh)	TCHR	10	–	10	–	10	–	ns	
RAS Precharge CAS Hold Time	TRPC	5	–	5	–	5	–	ns	
RAS Pulse Width (CAS before RAS Self Refresh Cycle)	TRASS	100	–	100	–	100	–	μs	1
RAS Precharge Time (CAS before RAS Self Refresh Cycle)	TRPS	110	–	130	–	150	–	ns	1
CAS Hold Time (CAS before RAS Self Refresh Cycle)	TCHS	–50	–	–50	–	–50	–	ns	1
WE Setup Time	TWSR	10	–	10	–	10	–	ns	
WE Hold Time	TWHR	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S16400L, 42S17400L.

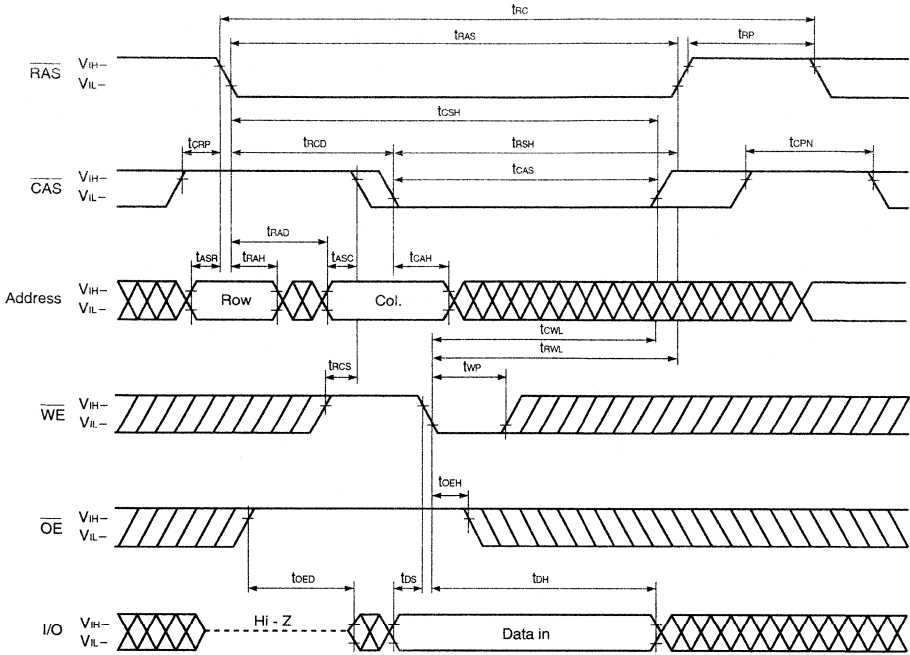


Early Write Cycle

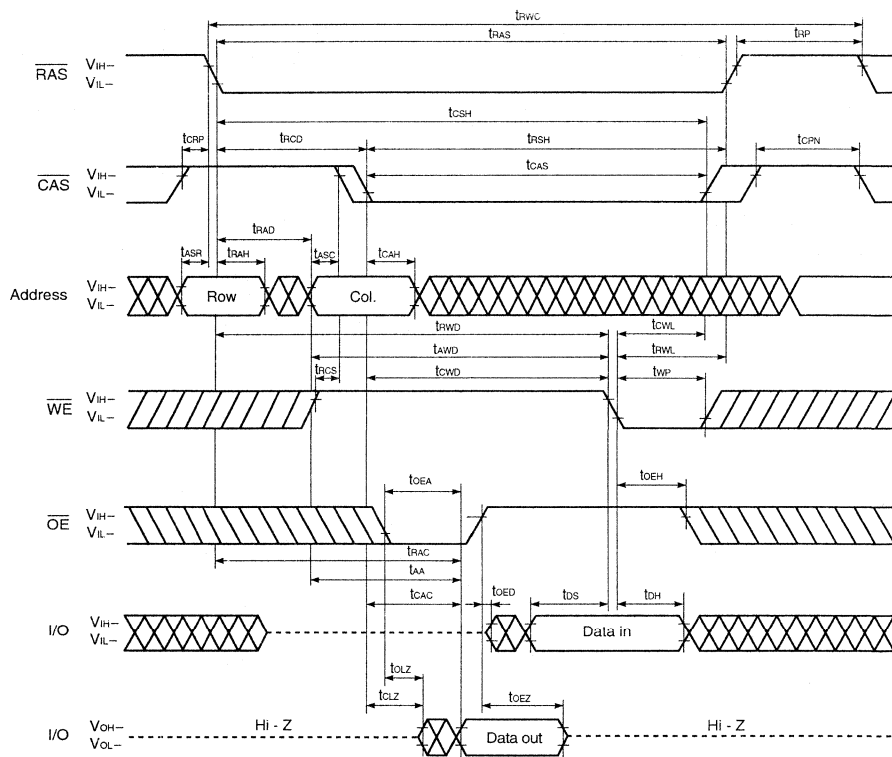


Remark $\overline{OE}$: Don't care

Late Write Cycle



Read Modify Write Cycle



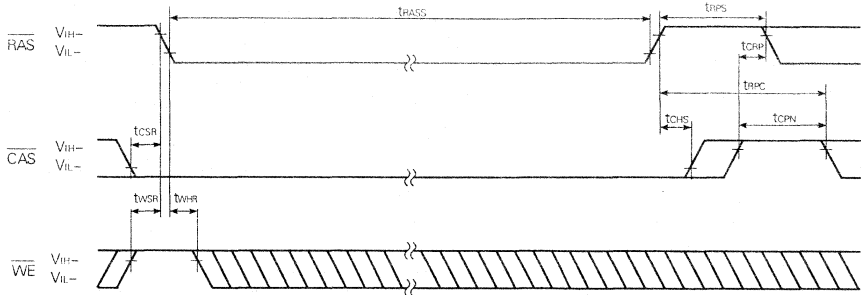
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CAS Before RAS Self Refresh Cycle (Only for the μ PD42S16400L, 42S17400L)



Remark Address, OE : Don't care I/O : Hi-Z

Cautions on Use of CAS Before RAS Self Refresh



CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16400L : 4 096 times within a 64 ms interval

μ PD42S17400L : 2 048 times within a 32 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

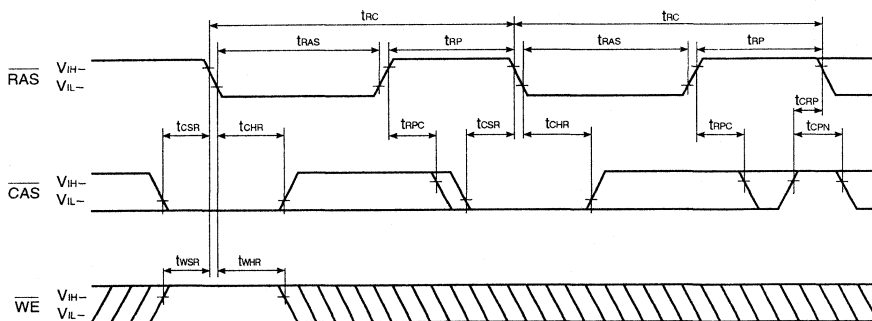
When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16400L : 4 096 times within a 64 ms interval

μ PD42S17400L : 2 048 times within a 32 ms interval

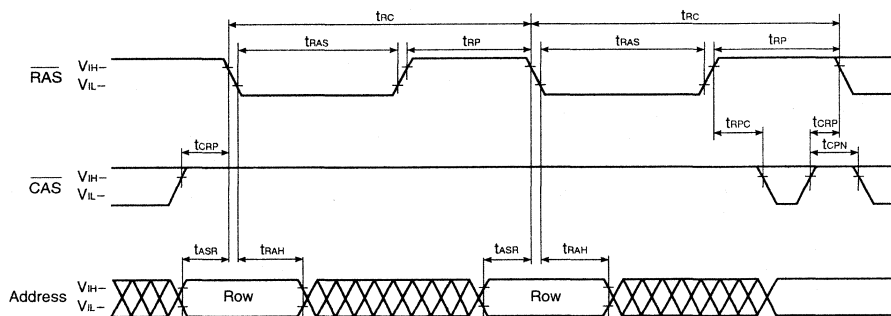
For details, please refer to **How to use DRAM** User's Manual.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi - Z

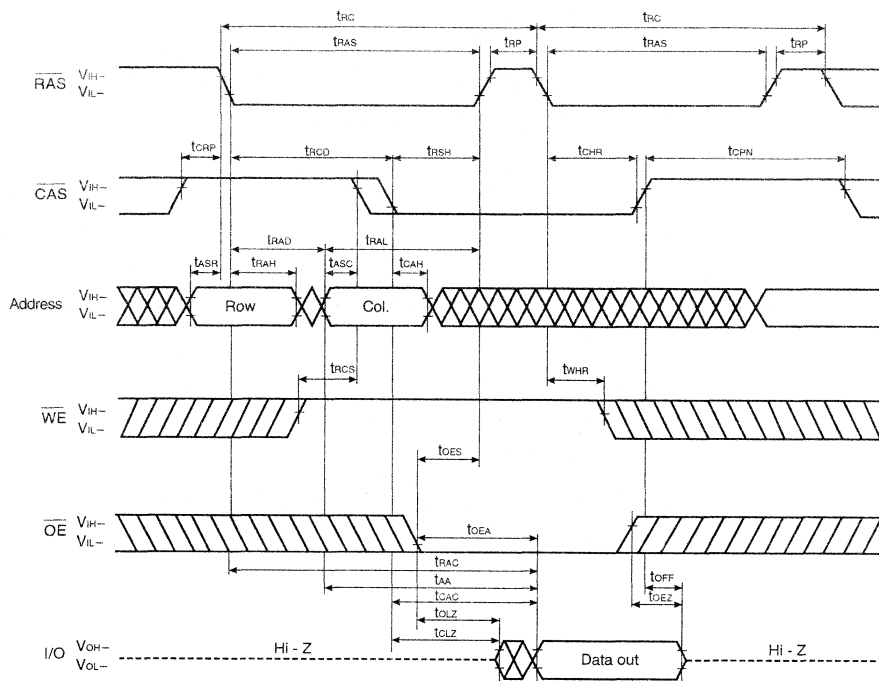
$\overline{\text{RAS}}$ Only Refresh Cycle



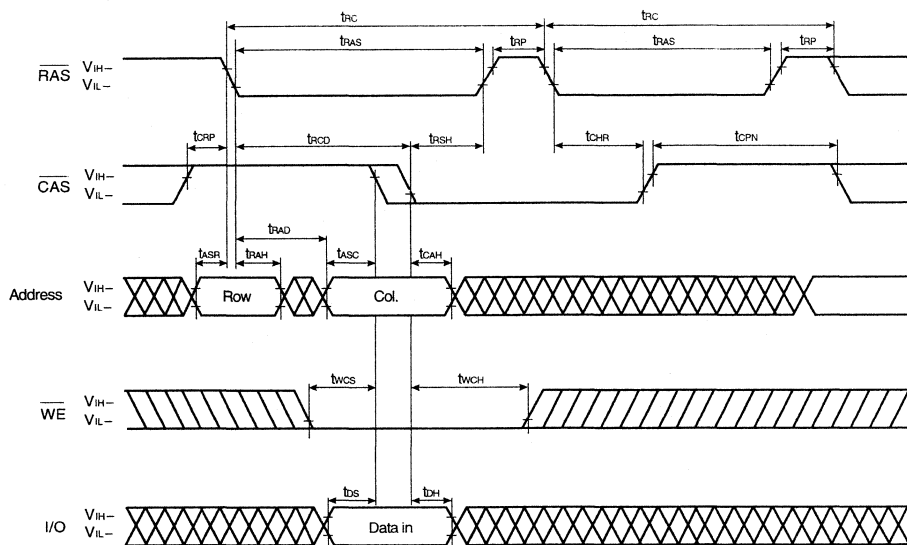
Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O: Hi - Z

Hidden Refresh Cycle (Read)

★

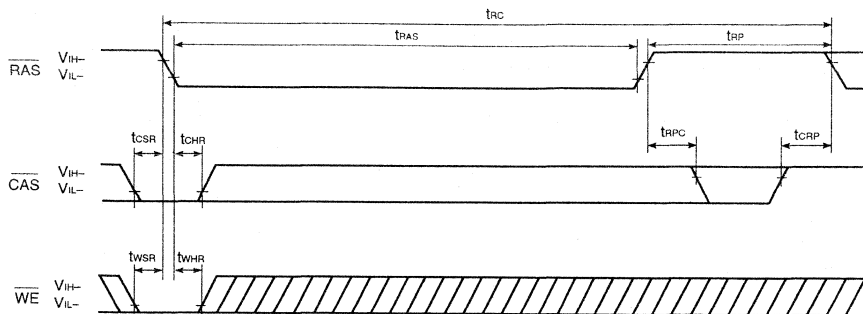


★ Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O : Hi - Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 16$ -bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output="1": Normal write (all memory cells)

Output="0": Abnormal write

(3) Refresh

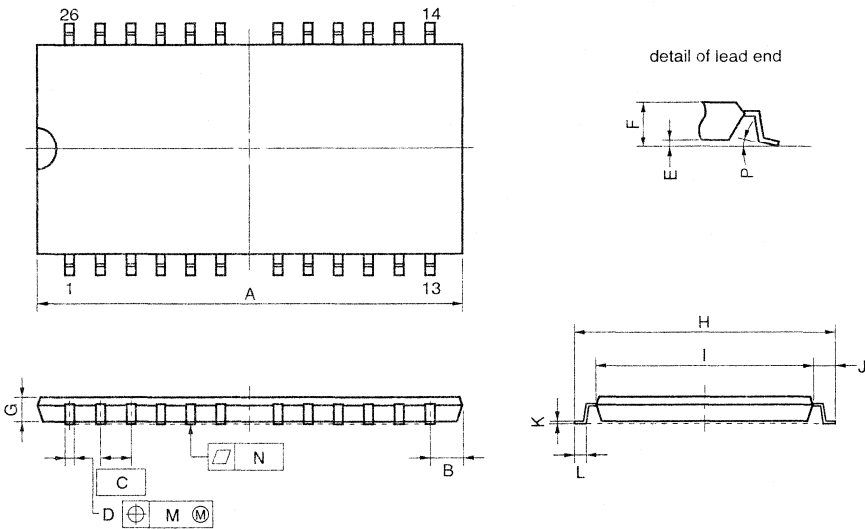
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

★ Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)

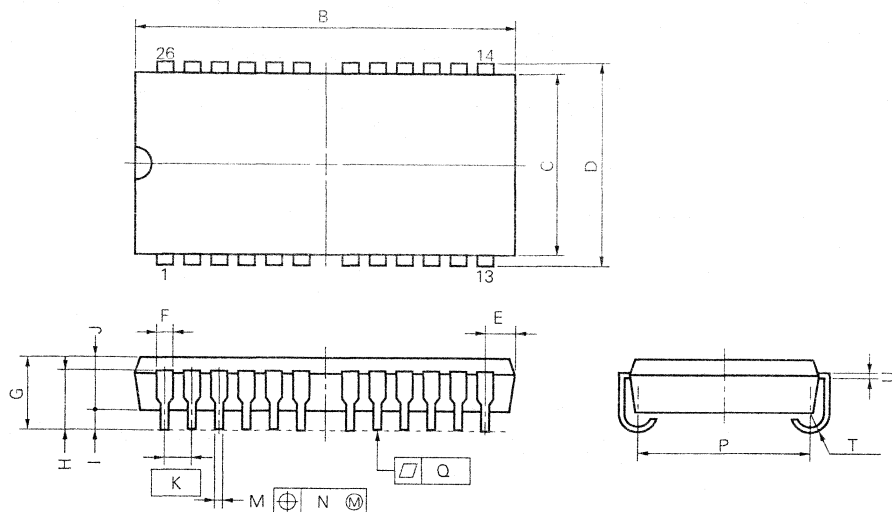


NOTE
 Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.42 ^{+0.08} _{-0.07}	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004
P	3°+7° -3°	3°+7° -3°

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S26LA-300A

ITEM	MILLIMETERS	INCHES
B	17.1 ^{+0.25} _{-0.65}	0.673 ^{+0.010} _{-0.002}
C	7.62	0.300
D	8.47±0.2	0.333 ^{+0.009} _{-0.008}
E	1.03±0.15	0.041 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.54±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

★ Recommended Soldering Conditions

The following conditions (see tables below) must be met for soldering conditions of the μPD42S16400L, 4216400L, 42S17400L, 4217400L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16400LG3, 4216400LG3, 42S17400LG3, 4217400LG3 : 26-pin plastic TSOP(II) (300 mil)

Please consult with our sales offices.

μPD42S16400LLA, 4216400LLA, 42S17400LLA, 4217400LLA : 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

MOS INTEGRATED CIRCUIT

μ PD42S16405L, 4216405L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM
4 M-WORD BY 4-BIT, HYPER PAGE MODE

DESCRIPTION

The μ PD42S16405L, 4216405L are 4 194 304 words by 4 bits dynamic CMOS RAMs with optional hyper page mode.

Hyper page mode is a kind of page mode and is useful for the read operation.

The μ PD42S16405L, 4216405L are packed in 26-pin plastic TSOP(III) and 26-pin plastic SOJ.

FEATURES

- Hyper page mode
- Single +3.3 V $\pm$ 0.3 V power supply
- 4 194 304 words by 4 bits organization

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μ PD42S16405L-A60, 4216405L-A60	60 ns	104 ns	25 ns
μ PD42S16405L-A70, 4216405L-A70	70 ns	124 ns	30 ns

- μ PD42S16405L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh
μ PD42S16405L	4 096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh
		$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
		$\overline{\text{RAS}}$ only refresh
		Hidden refresh
μ PD4216405L	4 096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
		$\overline{\text{RAS}}$ only refresh
		Hidden refresh

The information in this document is subject to change without notice.

ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μPD42S16405LG3-A60-7JD	60 ns	26-pin Plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh
μPD42S16405LG3-A70-7JD	70 ns		
μPD42S16405LG3-A60-7KD	60 ns	26-pin Plastic TSOP (II) (300 mil)	CAS before $\overline{\text{RAS}}$ refresh
μPD42S16405LG3-A70-7KD	70 ns	Reverse bent	$\overline{\text{RAS}}$ only refresh
μPD42S16405LLA-A60	60 ns	26-pin Plastic SOJ (300 mil)	Hidden refresh
μPD42S16405LLA-A70	70 ns		
μPD4216405LG3-A60-7JD	60 ns	26-pin Plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
μPD4216405LG3-A70-7JD	70 ns		
μPD4216405LG3-A60-7KD	60 ns	26-pin Plastic TSOP (II) (300 mil)	$\overline{\text{RAS}}$ only refresh
μPD4216405LG3-A70-7KD	70 ns	Reverse bent	Hidden refresh
μPD4216405LLA-A60	60 ns	26-pin Plastic SOJ (300 mil)	Hidden refresh
μPD4216405LLA-A70	70 ns		

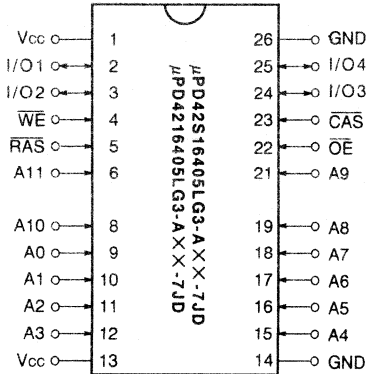
QUALITY GRADE

Standard

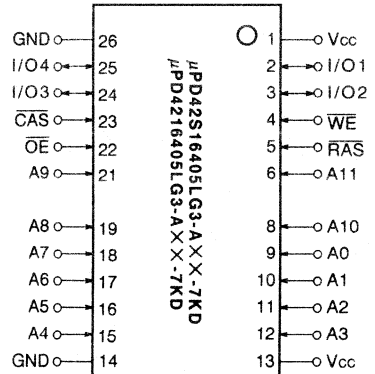
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATIONS (Marking Side)

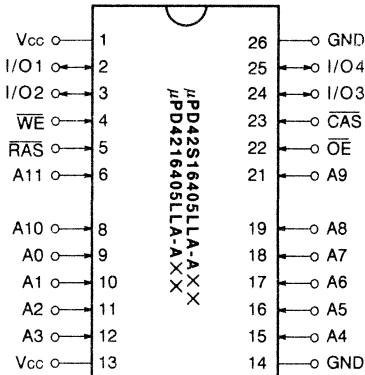
26-pin Plastic TSOP (III) (300 mil)



Reverse bent

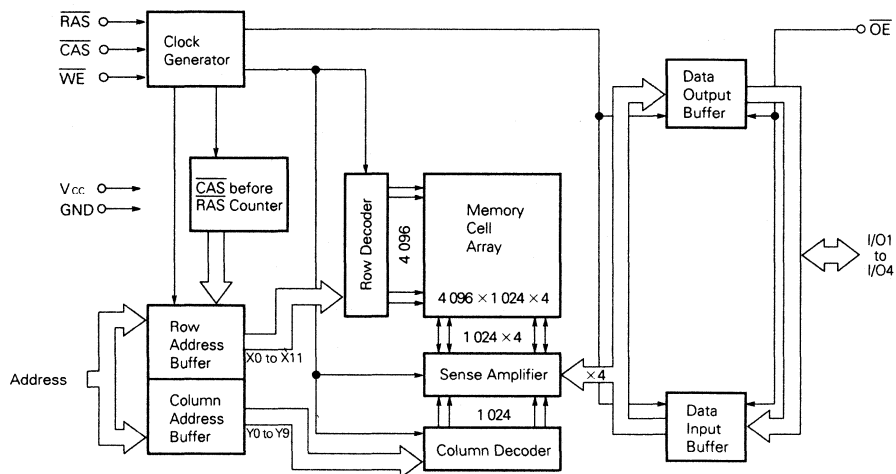


26-pin Plastic SOJ (300 mil)



- A0 to A11 : Address Inputs
- I/O1 to I/O4 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground

BLOCK DIAGRAM



INPUT/OUTPUT PIN FUNCTIONS

The μPD42S16405L, 4216405L have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11 and input/output pins I/O1 to I/O4.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)		Address bus. Input total 22-bit of address signal, upper 12-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 4 194 304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/ Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

ELECTRICAL SPECIFICATIONS Notes1, 2**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Ambient temperature	T_a		0		70	°C

CAPACITANCE ($T_a = +25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A11			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1 to I/O4			7	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	RAS, CAS Cycling t _{RC} = t _{RC(MIN.)} I _O = 0 mA	t _{RAC} = 60 ns t _{RAC} = 70 ns	80 70	mA	3,4,7
Standby current	μPD42S16405L μPD4216405L	I _{CC2} RAS, CAS ≥ V _{IH(MIN.)} , I _O = 0 mA RAS, CAS ≥ V _{CC} - 0.2 V, I _O = 0 mA RAS, CAS ≥ V _{IH(MIN.)} , I _O = 0 mA RAS, CAS ≥ V _{CC} - 0.2 V, I _O = 0 mA		0.5 0.15 2 0.5	mA	
RAS only refresh current	I _{CC3}	RAS Cycling CAS ≥ V _{IH(MIN.)} t _{RC} = t _{RC(MIN.)} I _O = 0 mA	t _{RAC} = 60 ns t _{RAC} = 70 ns	80 70	mA	3,4,5,7
Operating current (Hyper page mode)	I _{CC4}	RAS ≤ V _{IL(MAX.)} CAS Cycling t _{HPC} = t _{HPC(MIN.)} I _O = 0 mA	t _{RAC} = 60 ns t _{RAC} = 70 ns	90 80	mA	3,4,6
CAS before RAS refresh current	I _{CC5}	RAS Cycling t _{RC} = t _{RC(MIN.)} I _O = 0 mA	t _{RAC} = 60 ns t _{RAC} = 70 ns	80 70	mA	3,4
CAS before RAS long refresh current (4 096 Cycles / 128 ms, only for the μPD42S16405L)	I _{CC6}	CAS before RAS refresh : 4 096 Cycles / 128 ms RAS, CAS : V _{CC} -0.2 V ≤ V _{IH} ≤ V _{IH(MAX.)} 0 V ≤ V _{IL} ≤ 0.2 V Standby : RAS, CAS ≥ V _{CC} -0.2 V Address : V _{IH} or V _{IL} WE, OE : V _{IH} I _O = 0 mA	t _{RAS} ≤ 1 μs	220	μA	3,4
Self refresh current (CAS before RAS self refresh, only for the μPD42S16405L)	I _{CC7}	RAS, CAS : V _{CC} -0.2 V ≤ V _{IH} ≤ V _{IH(MAX.)} 0 V ≤ V _{IL} ≤ 0.2 V I _O = 0 mA		150	μA	4
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V all other pins not under test = 0 V		-5 +5	μA	
Output leakage current	I _{O(L)}	V _O = 0 to 3.6 V Output is disabled (Hi-Z)		-5 +5	μA	
High level output voltage	V _{OH}	I _O = -2.0 mA		2.4	V	
Low level output voltage	V _{OL}	I _O = +2.0 mA		0.4	V	

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted) Notes 8, 9 (1/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{RC}	104		124		ns	
Read Modify Write Cycle Time	t _{RWC}	133		157		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		15		18	ns	10, 11
Access Time from Column Address	t _{AA}		30		35	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEA}		15		18	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	12	30	12	35	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0		0		ns	11
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	13		15		ns	
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OEZ}	0	13	0	15	ns	12, 19
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0		0		ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{OES}	0		0		ns	
Transition Time (Rise and Fall)	t _T	1	50	1	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10 000	70	10 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	10		12		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	10	10 000	12	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	40		50		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	14	45	14	52	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		ns	
Row Address Setup Time	t _{ASR}	0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		ns	
Column Address Setup Time	t _{ASC}	0		0		ns	
Column Address Hold Time	t _{CAH}	10		12		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		ns	
Read Command Setup Time	t _{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		ns	15
$\overline{\text{WE}}$ Pulse Width	t _{WP}	10		10		ns	15
Data-in Setup Time	t _{DS}	0		0		ns	16
Data-in Hold Time	t _{DH}	10		10		ns	16
Write Command Setup Time	t _{WCS}	0		0		ns	18
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	32		37		ns	18
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	77		89		ns	18
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	47		54		ns	18

(2/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
WE Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	10		12		ns	
WE Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	10		12		ns	
CAS Setup Time for CAS before RAS Refresh	t _{CSR}	5		5		ns	
CAS Hold Time for CAS before RAS Refresh	t _{CHR}	10		10		ns	
RAS Pulse Width for CAS before RAS Self Refresh	t _{RASS}	100		100		μ s	17
RAS Precharge Time for CAS before RAS Self Refresh	t _{RPS}	110		130		ns	17
CAS Hold Time for CAS before RAS Self Refresh	t _{CHS}	- 50		- 50		ns	17
WE Setup Time	t _{WSR}	10		10		ns	
WE Hold Time	t _{WHR}	15		15		ns	
Refresh Time	μ PD42S16405L	t _{REF}	128		128	ms	17
	μ PD4216405L		64		64		

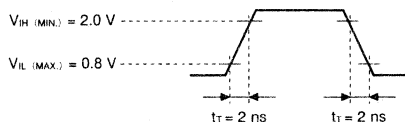
HYPER PAGE MODE

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{HPC}	25		30		ns	
RAS Pulse Width	t _{RASP}	60	125 000	70	125 000	ns	
CAS Pulse Width	t _{HCAS}	10	10 000	12	10 000	ns	
CAS Precharge Time	t _{CP}	10		10		ns	
CAS Precharge to WE Delay Time	t _{CPWD}	52		59		ns	18
Read Modify Write Cycle Time	t _{HPRWC}	66		75		ns	
Data Output Hold Time	t _{DHC}	5		5		ns	
Output Buffer Turn-off Delay from $\overline{\text{WE}}$	t _{WEZ}	0	13	0	15	ns	12, 19
WE Pulse Width	t _{WPZ}	10		10		ns	19
Output Buffer Turn-off Delay from $\overline{\text{RAS}}$	t _{OFR}	0	13	0	15	ns	12, 19
Output Buffer Turn-off Delay from CAS	t _{OFC}	0	13	0	15	ns	12, 19

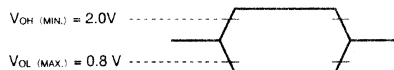
- Notes**
1. All voltages are referenced to GND.
 2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
 3. Icc1, Icc3, Icc4, Icc5 and Icc6 depend on cycle rates (t_{RAC} and t_{HPC}).
 4. Specified values are obtained with outputs unloaded.
 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
 6. Icc4 is measured assuming that all column address inputs are switched only once during each hyper page cycle.
 7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{IL(\text{MAX.})}$ and $\text{CAS} \geq V_{IH(\text{MIN.})}$.
 8. AC measurements assume t_r = 2 ns.

Notes 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}}(\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

11. Loading conditions are 1 TTL and 100 pF.
12. $t_{\text{OFC}}(\text{MAX.})$, $t_{\text{OFR}}(\text{MAX.})$, $t_{\text{WEZ}}(\text{MAX.})$ and $t_{\text{OEZ}}(\text{MAX.})$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .
13. $t_{\text{CRP}}(\text{MIN.})$ requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles preceded by any cycles.
14. Either $t_{\text{RCH}}(\text{MIN.})$ or $t_{\text{RRH}}(\text{MIN.})$ should be met in read cycles.
15. $t_{\text{WP}}(\text{MIN.})$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{\text{WCH}}(\text{MIN.})$ should be met.
16. $t_{\text{DS}}(\text{MIN.})$ and $t_{\text{DH}}(\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
17. This specification is applied only to the μPD42S16405L.
18. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{\text{RWd}} \geq t_{\text{RWd}}(\text{MIN.})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{MIN.})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{MIN.})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
19. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on state of each signal.

(1) $\overline{\text{RAS}}$, $\overline{\text{CAS}}$: inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

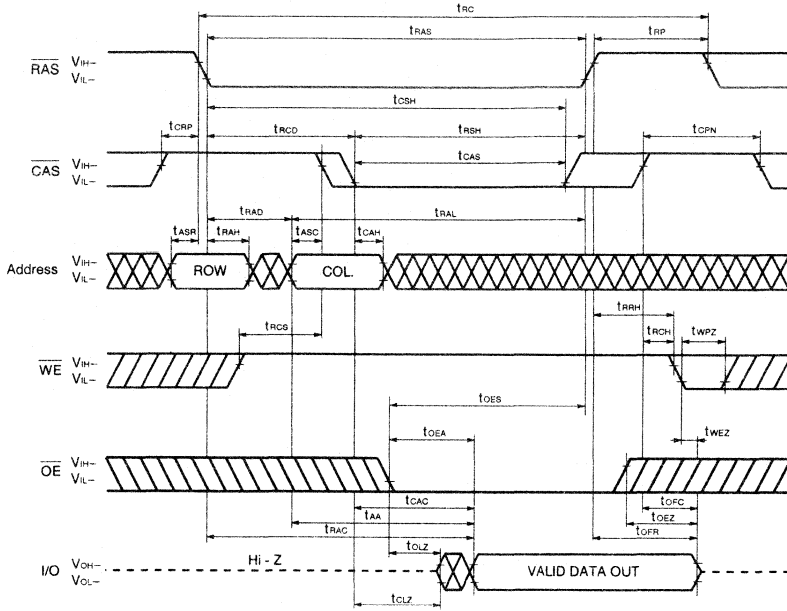
t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

(2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

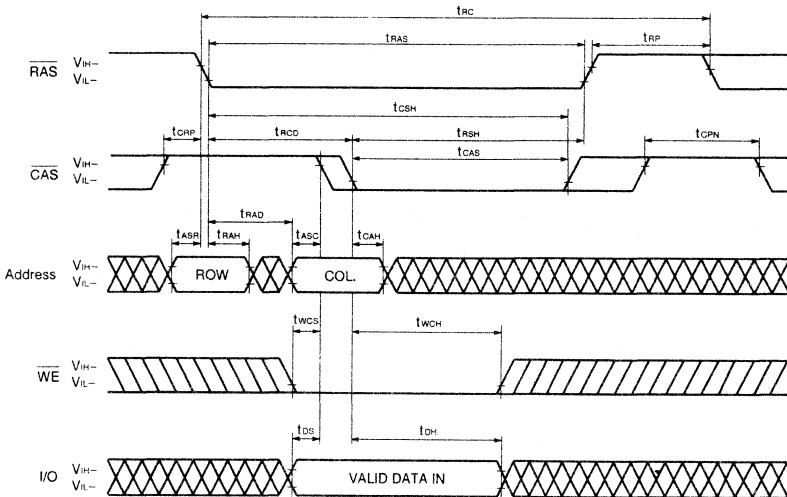
$\overline{\text{WE}}$: active, $\overline{\text{OE}}$: active... t_{WEZ} , t_{WPZ} are effective.

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: inactive... t_{OEZ} is effective.

READ CYCLE



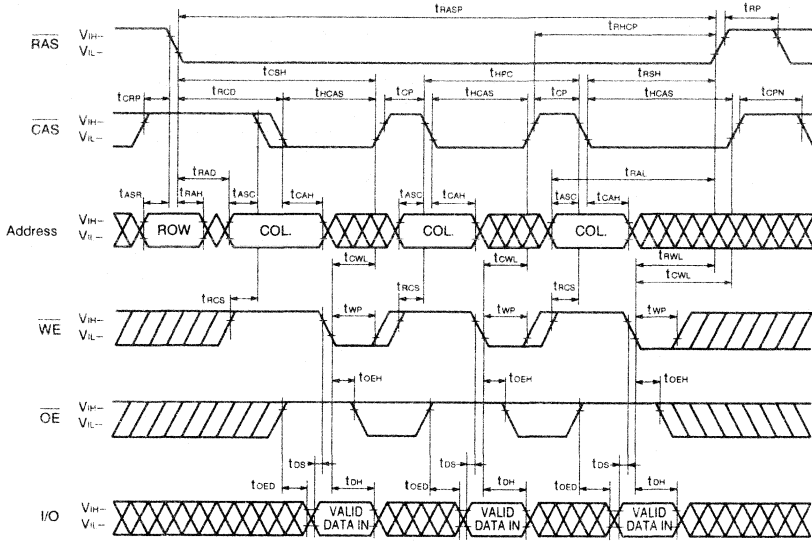
EARLY WRITE CYCLE



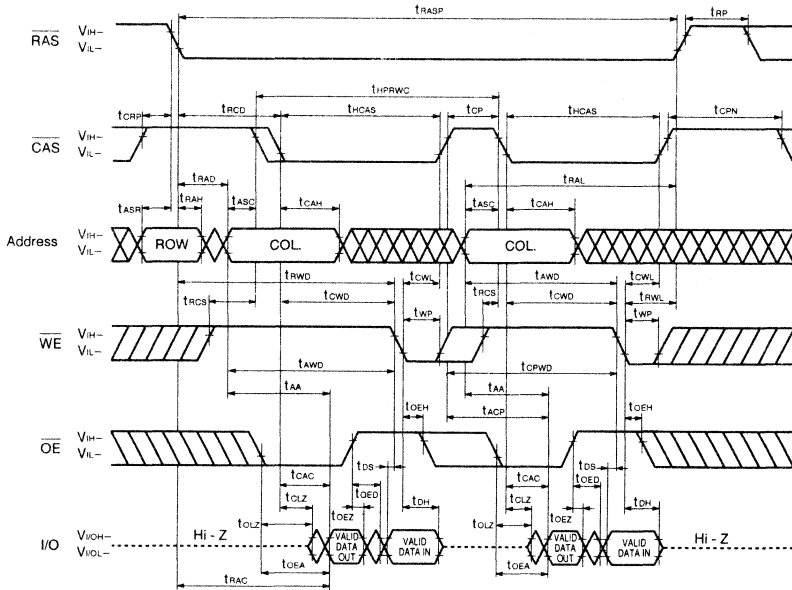
Remark $\overline{\text{OE}}$ = Don't Care

[illegible]

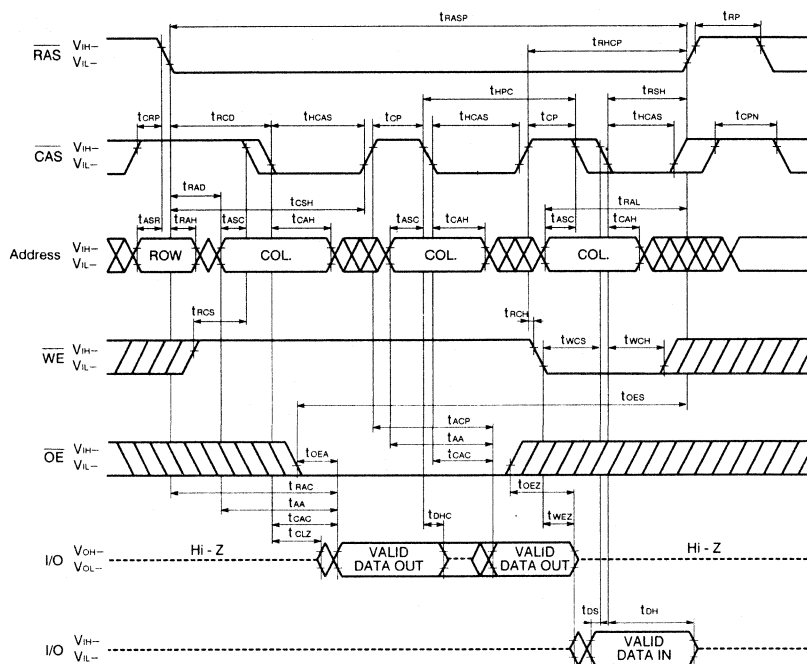
HYPER PAGE MODE LATE WRITE CYCLE



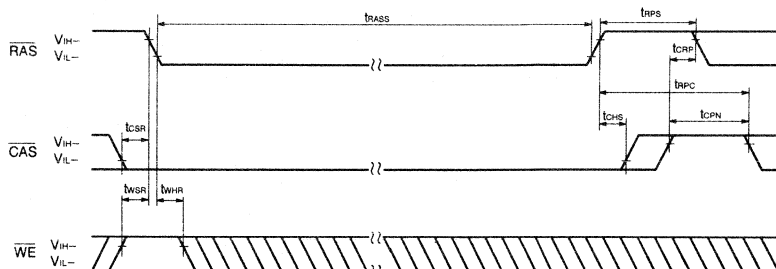
HYPER PAGE MODE READ MODIFY WRITE CYCLE



HYPER PAGE MODE READ AND WRITE CYCLE



CAS Before RAS Self Refresh Cycle (Only for the μPD42S16405L)



Remark Address, $\overline{OE}$: Don't care I/O : Hi - Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

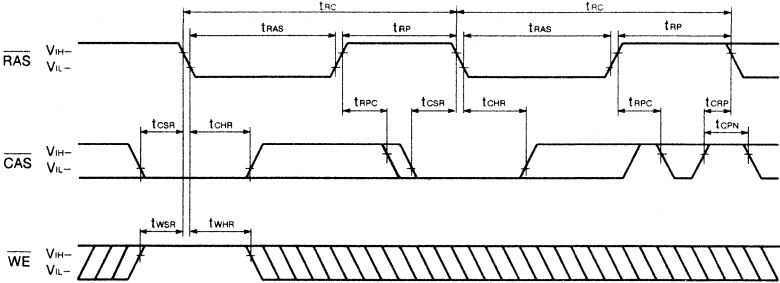
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 4 096 times within a 64 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh 4 096 times within an interval of 64 ms or less just before and after setting CAS before RAS self refresh.

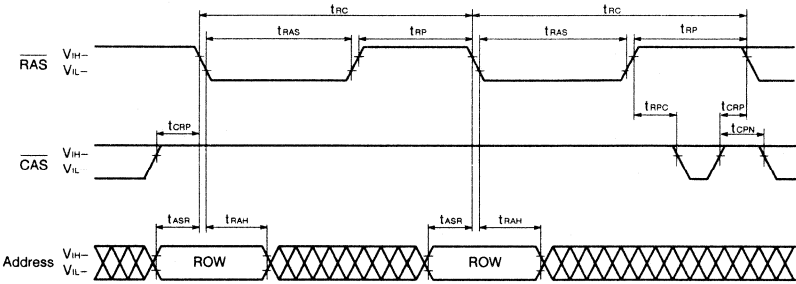
For details, please refer to **How to use DRAM User's Manual**.

CAS BEFORE RAS REFRESH CYCLE



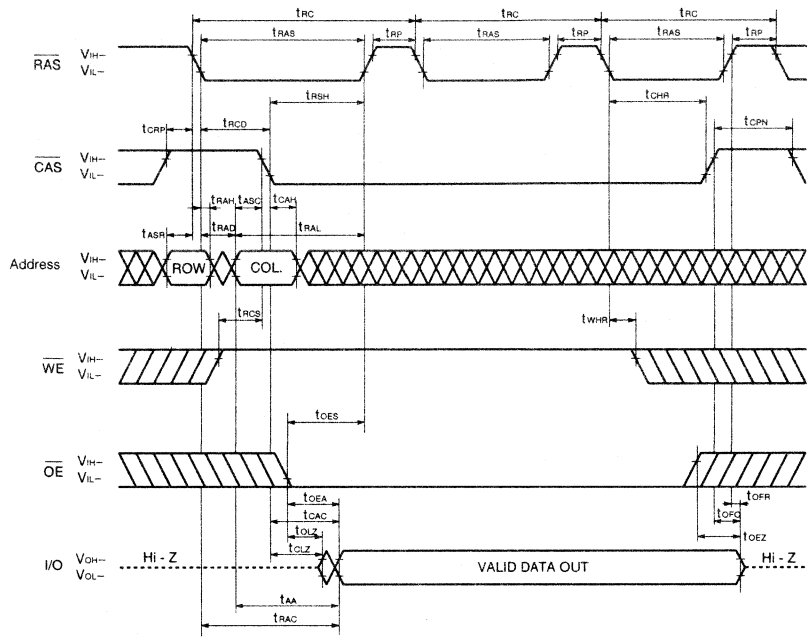
Remark Address, $\overline{OE}$ = Don't care I/O = Hi - Z

RAS ONLY REFRESH CYCLE

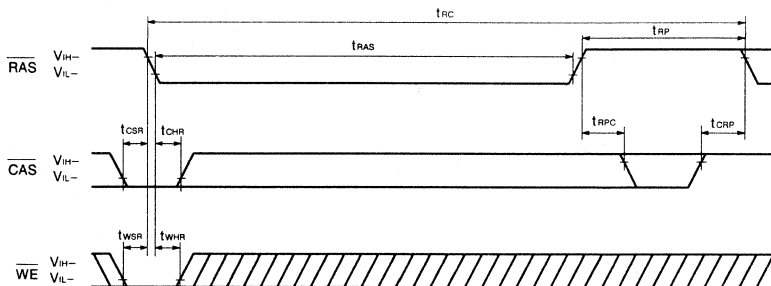


Remark $\overline{WE}$, $\overline{OE}$ = Don't care I/O = Hi - Z

HIDDEN REFRESH CYCLE



TEST MODE SET CYCLE ($\overline{WE}$, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE)



Remark Address, $\overline{OE}$ = Don't care I/O = Hi - Z

TEST MODE

TEST MODE is fast test function. On using this mode, test time is reduced to 1/4. In this TEST MODE, internal organization is 1 M words by 16 bits apparently. Don't care about the input levels of the column address input A0, A1.

1. How to enter TEST MODE

Through TEST MODE SET CYCLE ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle), the device enters TEST MODE.

2. Write / Read in TEST MODE

Write data of "1" or "0" through I/O1 to I/O4 by controlling address except for above-mentioned address. Each input data through each I/O write 4 bits at once. And read through I/O1 to I/O4 to check written data. In case of writing each 4 bits rightly, each I/O data is "1". But wrong, the data is "0".

3. Refresh in TEST MODE

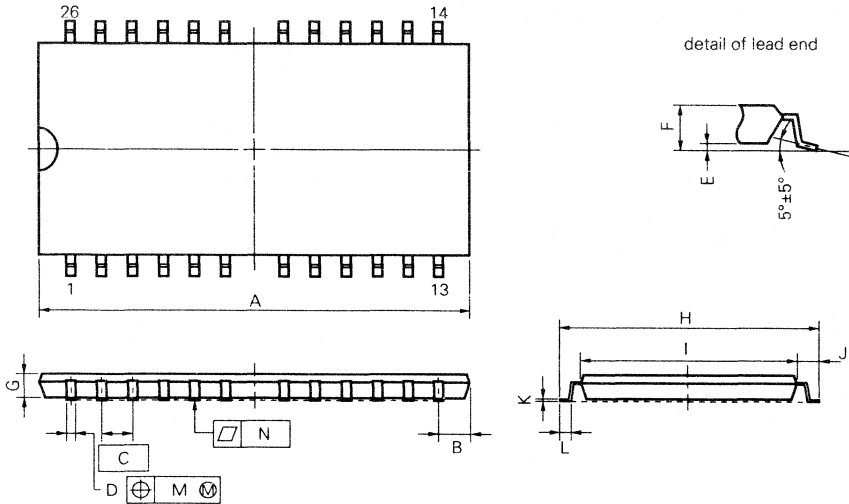
Use normal read cycle or $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

4. How to exit from TEST MODE

Through $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, the device exits from TEST MODE.

PACKAGE DRAWINGS

26 PIN PLASTIC TSOP(II) (300 mil)



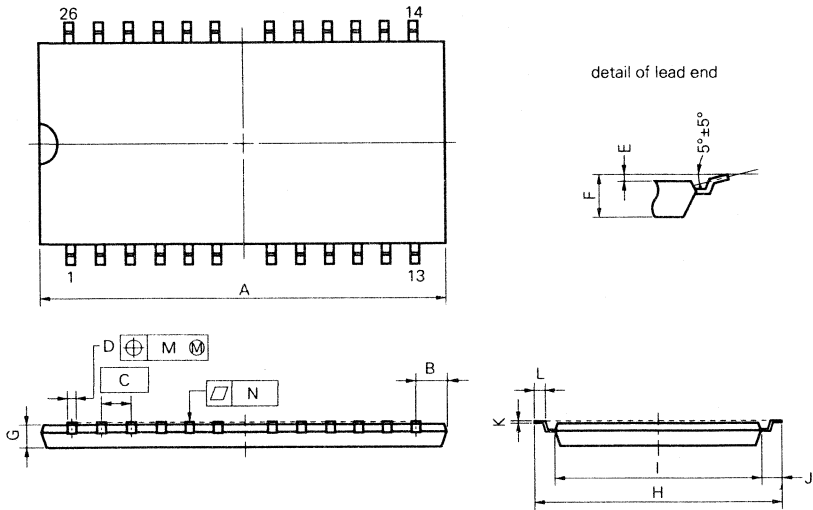
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S26G3-50-7JD-1

ITEM	MILLIMETERS	INCHES
A	17.40 MAX.	0.685 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

26 PIN PLASTIC TSOP(II) (300 mil)



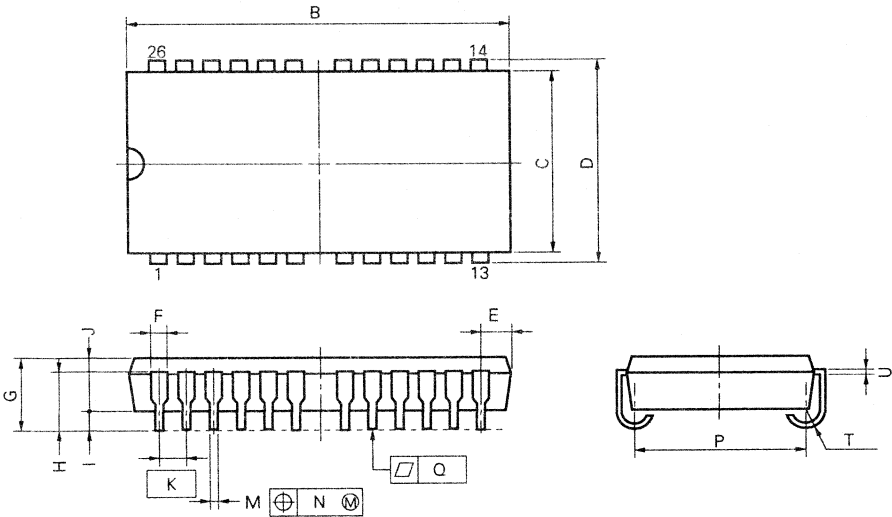
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S26G3-50-7KD-1

ITEM	MILLIMETERS	INCHES
A	17.40 MAX.	0.685 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

26 PIN PLASTIC SOJ (300 mil)



S26LA-300A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	17.1 ^{+0.25} _{-0.05}	0.673 ^{+0.010} _{-0.002}
C	7.62	0.300
D	8.47±0.2	0.333 ^{+0.009} _{-0.008}
E	1.03±0.15	0.041 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μPD42S16405L, 4216405L.

TYPE OF SURFACE MOUNT DEVICE

μPD42S16405LG3, 4216405LG3 : 26-pin Plastic TSOP (II) (300 mil)

μPD42S16405LLA, 4216405LLA : 26-pin Plastic SOJ (300 mil)

MOS INTEGRATED CIRCUIT

μ PD42S16800L, 4216800L, 42S17800L, 4217800L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 2 M-WORD BY 8-BIT, FAST PAGE MODE

Description

The μ PD42S16800L, 4216800L, 42S17800L, 4217800L are 2 097 152 words by 8 bits dynamic CMOS RAMs.

These differ in refresh cycle and the μ PD42S16800L, 42S17800L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (see the table below).

These are packed in 28-pin plastic TSOP(III) and 28-pin plastic SOJ.

Features

- 2 097 152 words by 8 bits organization
- Single +3.3 V $\pm$ 0.3 V power supply
- Fast page mode
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S16800L-A60, 4216800L-A60	288 mW	60 ns	110 ns	40 ns
μ PD42S17800L-A60, 4217800L-A60	360 mW			
μ PD42S16800L-A70, 4216800L-A70	252 mW	70 ns	130 ns	45 ns
μ PD42S17800L-A70, 4217800L-A70	324 mW			
μ PD42S16800L-A80, 4216800L-A80	216 mW	80 ns	150 ns	50 ns
μ PD42S17800L-A80, 4217800L-A80	288 mW			

- The μ PD42S16800L, μ PD42S17800L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S16800L	4 096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μ PD42S17800L	2 048 cycles/128 ms		
μ PD4216800L	4 096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)
μ PD4217800L	2 048 cycles/32 ms		

The information in this document is subject to change without notice.

The mark ★ shows revised points.

★ Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD42S16800LG5-A60-7JD	60 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S17800LG5-A60-7JD			
μ PD42S16800LG5-A70-7JD	70 ns		
μ PD42S17800LG5-A70-7JD			
μ PD42S16800LG5-A80-7JD	80 ns		
μ PD42S17800LG5-A80-7JD			
μ PD42S16800LLE-A60	60 ns	28-pin plastic SOJ (400 mil)	
μ PD42S17800LLE-A60			
μ PD42S16800LLE-A70	70 ns		
μ PD42S17800LLE-A70			
μ PD42S16800LLE-A80	80 ns		
μ PD42S17800LLE-A80			
μ PD4216800LG5-A60-7JD	60 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4217800LG5-A60-7JD			
μ PD4216800LG5-A70-7JD	70 ns		
μ PD4217800LG5-A70-7JD			
μ PD4216800LG5-A80-7JD	80 ns		
μ PD4217800LG5-A80-7JD			
μ PD4216800LLE-A60	60 ns	28-pin plastic SOJ (400 mil)	
μ PD4217800LLE-A60			
μ PD4216800LLE-A70	70 ns		
μ PD4217800LLE-A70			
μ PD4216800LLE-A80	80 ns		
μ PD4217800LLE-A80			

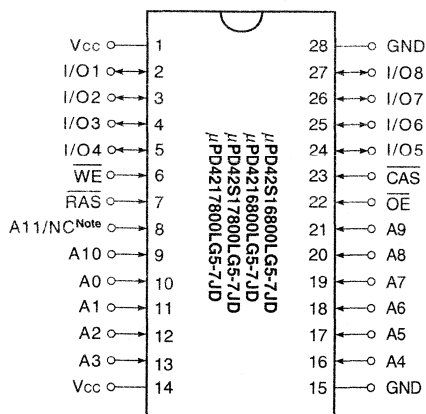
Quality Grade

Standard

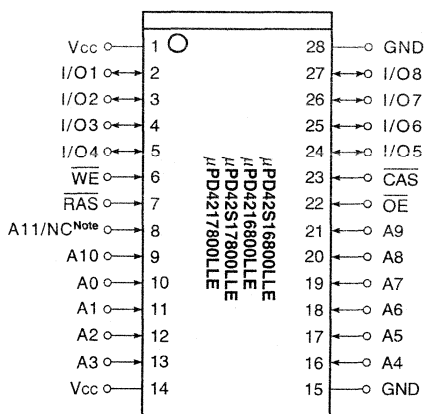
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking Side)

28-pin Plastic TSOP(II) (400 mil)



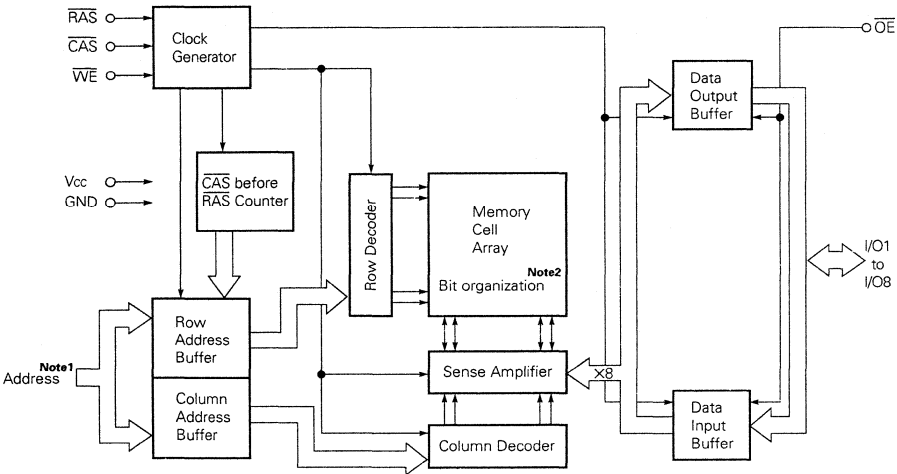
28-pin Plastic SOJ (400 mil)



- A0 to A11 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Note A11 ...μPD42S16800L, 4216800L
 NC ...μPD42S17800L, 4217800L (No connection)

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S16800L, 4216800L	A0 to A11	A0 to A8
μPD42S17800L, 4217800L	A0 to A10	A0 to A9

2. μPD42S16800L, 4216800L...4 096 × 512 × 8 μPD42S17800L, 4217800L...2 048 × 1 024 × 8

Input/Output Pin Functions

The μPD42S16800L, 4216800L, 42S17800L, 4217800L have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11/A10^{Note1} and input/output pins I/O1 to I/O8.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • CAS before RAS refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11/A10 ^{Note1} (Address inputs)		Address bus. Input total 21-bit of address signal, upper 12/11 ^{Note2} -bit and lower 9/10 ^{Note3} -bit in sequence (address multiplex method). Therefore, one word is selected from 2 097 152-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (tASR, tASC) and hold time (tRAH, tCAH) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/ Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Notes 1. A11...μPD42S16800L, 4216800L

2. 12...μPD42S16800L, 4216800L

3. 9...μPD42S16800L, 4216800L

A10...μPD42S17800L, 4217800L

11...μPD42S17800L, 4217800L

10...μPD42S17800L, 4217800L

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-0.5 to +4.6	V
Supply Voltage	V_{CC}		-0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low Level Input Voltage	V_{IL}		-0.3		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

[μ PD42S16800L, 4216800L]

Parameter		Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	RAS, CAS Cycling trc = trc(MIN.) I _O = 0 mA	trAC = 60 ns		80	mA	1, 2, 3
				trAC = 70 ns		70		
				trAC = 80 ns		60		
Standby current	μ PD42S16800L	I _{CC2}	RAS, CAS $\geq V_{IH(MIN.)}$, I _O = 0 mA			0.5	mA	
			RAS, CAS $\geq V_{CC} - 0.2$ V, I _O = 0 mA			0.15		
	μ PD4216800L		RAS, CAS $\geq V_{IH(MIN.)}$, I _O = 0 mA			2		
			RAS, CAS $\geq V_{CC} - 0.2$ V, I _O = 0 mA			0.5		
RAS only refresh current		I _{CC3}	RAS Cycling, CAS $\geq V_{IH(MIN.)}$ trc = trc(MIN.), I _O = 0 mA	trAC = 60 ns		80	mA	1,2,3,4
				trAC = 70 ns		70		
				trAC = 80 ns		60		
Operating current (Fast page mode)		I _{CC4}	RAS $\leq V_{IL(MAX.)}$, CAS Cycling tpc = tpc(MIN.), I _O = 0 mA	trAC = 60 ns		70	mA	1, 2, 5
				trAC = 70 ns		60		
				trAC = 80 ns		50		
CAS before RAS refresh current		I _{CC5}	RAS Cycling trc = trc(MIN.) I _O = 0 mA	trAC = 60 ns		80	mA	1, 2
				trAC = 70 ns		70		
				trAC = 80 ns		60		
CAS before RAS long refresh current (4 096 Cycles / 128 ms, only for the μ PD42S16800L)		I _{CC6}	CAS before RAS refresh: 4 096 Cycles / 128 ms RAS, CAS: $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX.)}$ 0 V $\leq V_{IL} \leq 0.2$ V Standby : RAS $\geq V_{CC} - 0.2$ V Address : Don't care WE, OE : V _{IH} I _O = 0 mA	trAS $\leq$ 1 μ s		220	μ A	1, 2
Self refresh current (CAS before RAS self refresh, only for the μ PD42S16800L)		I _{CC7}	RAS, CAS: $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX.)}$ 0 V $\leq V_{IL} \leq 0.2$ V I _O = 0 mA			150	μ A	2
Input leakage current		I _{IL}	V _I = 0 to 3.6 V All other pins not under test = 0 V	-5		+5	μ A	
Output leakage current		I _{OL}	V _O = 0 to 3.6 V Output is disabled (Hi-Z)	-5		+5	μ A	
High level output voltage		V _{OH}	I _O = -2.0 mA	2.4			V	
Low level output voltage		V _{OL}	I _O = +2.0 mA			0.4	V	

[μPD42S17800L, 4217800L]

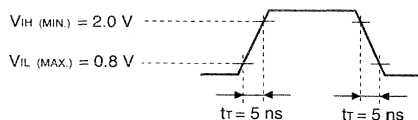
Parameter		Symbol	Test Condition		MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$			100	mA	1, 2, 3
				$\text{trac} = 70 \text{ ns}$			90		
				$\text{trac} = 80 \text{ ns}$			80		
Standby current	μPD42S17800L	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN.})}, \text{I}_\text{O} = 0 \text{ mA}$				0.5	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, \text{I}_\text{O} = 0 \text{ mA}$				0.15		
	μPD4217800L		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN.})}, \text{I}_\text{O} = 0 \text{ mA}$				2		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, \text{I}_\text{O} = 0 \text{ mA}$				0.5		
$\overline{\text{RAS}}$ only refresh current		I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN.})}$ $\text{trc} = \text{trc}(\text{MIN.}), \text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$			100	mA	1,2,3,4
				$\text{trac} = 70 \text{ ns}$			90		
				$\text{trac} = 80 \text{ ns}$			80		
Operating current (Fast page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}(\text{MAX.})}, \overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.}), \text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$			70	mA	1, 2, 5
				$\text{trac} = 70 \text{ ns}$			60		
				$\text{trac} = 80 \text{ ns}$			50		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$			100	mA	1, 2
				$\text{trac} = 70 \text{ ns}$			90		
				$\text{trac} = 80 \text{ ns}$			80		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (2 048 Cycles / 128 ms, only for the μPD42S17800L)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: 2 048 Cycles/128 ms $\overline{\text{RAS}}, \overline{\text{CAS}}:$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}(\text{MAX.})}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby : $\overline{\text{RAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : Don't care $\overline{\text{WE}}, \overline{\text{OE}} : V_{\text{IH}}$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} \leq 1 \mu\text{s}$			200	μA	1, 2
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for the μPD42S17800L)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}:$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}(\text{MAX.})}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $\text{I}_\text{O} = 0 \text{ mA}$				150	μA	2
Input leakage current		I _{I(L)}	$V_{\text{I}} = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V		-5		+5	μA	
Output leakage current		I _{O(L)}	$V_{\text{O}} = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)		-5		+5	μA	
High level output voltage		V _{OH}	$\text{I}_\text{O} = -2.0 \text{ mA}$		2.4			V	
Low level output voltage		V _{OL}	$\text{I}_\text{O} = +2.0 \text{ mA}$				0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (trc and tpc).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}(\text{MAX.})}$ and $\overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN.})}$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

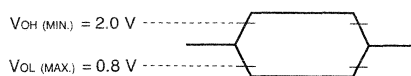
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		t _{RC}	110	–	130	–	150	–	ns	
RAS Precharge Time		t _{RP}	40	–	50	–	60	–	ns	
CAS Precharge Time		t _{CPN}	10	–	10	–	10	–	ns	
RAS Pulse Width		t _{RAS}	60	10 000	70	10 000	80	10 000	ns	
CAS Pulse Width		t _{CAS}	15	10 000	18	10 000	20	10 000	ns	
RAS Hold Time		t _{RSH}	15	–	18	–	20	–	ns	
CAS Hold Time		t _{CSH}	60	–	70	–	80	–	ns	
RAS to CAS Delay Time		t _{ACD}	20	45	20	50	25	60	ns	1
RAS to Column Address Delay Time		t _{RAD}	15	30	15	35	17	40	ns	1
CAS to RAS Precharge Time		t _{CRP}	5	–	5	–	5	–	ns	2
Row Address Setup Time		t _{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time		t _{RAH}	10	–	10	–	12	–	ns	
Column Address Setup Time		t _{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time		t _{CAH}	15	–	15	–	15	–	ns	
OE Lead Time Referenced to RAS		t _{OES}	0	–	0	–	0	–	ns	
CAS to Data Setup Time		t _{CLZ}	0	–	0	–	0	–	ns	
OE to Data Setup Time		t _{OLZ}	0	–	0	–	0	–	ns	
OE to Data Delay Time		t _{OED}	13	–	15	–	15	–	ns	
Transition Time (Rise and Fall)		t _T	3	50	3	50	3	50	ns	
Refresh Time	μPD42S16800L, 42S17800L	t _{REF}	–	128	–	128	–	128	ms	3
	μPD4216800L		–	64	–	64	–	64		
	μPD4217800L		–	32	–	32	–	32		

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
t _{RAD} ≤ t _{RAD} (MAX.) and t _{RC} ≤ t _{RC} (MAX.)	t _{RAC} (MAX.)	t _{RAC} (MAX.)
t _{RAD} > t _{RAD} (MAX.) and t _{RC} ≤ t _{RC} (MAX.)	t _{AA} (MAX.)	t _{RAD} + t _{AA} (MAX.)
t _{RC} > t _{RC} (MAX.)	t _{CAC} (MAX.)	t _{RC} + t _{CAC} (MAX.)

t_{RAD} (MAX.) and t_{RC} (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions t_{RAD} ≥ t_{RAD} (MAX.) and t_{RC} ≥ t_{RC} (MAX.) will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.
3. This specification is applied only to the μPD42S16800L, 42S17800L.

Read Cycle

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		$t_{RAC} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	18	–	20	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	–	40	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	15	–	18	–	20	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	40	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	15	ns	3
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi - Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	10	–	10	–	15	–	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	10	–	10	–	15	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	20	–	20	–	20	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	15	–	15	–	15	–	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	–	0	–	0	–	ns	
Data-in Setup Time	tds	0	–	0	–	0	–	ns	3
Data-in Hold Time	tdh	10	–	15	–	15	–	ns	3

- Notes**
1. twp(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch(MIN.) should be met.
 2. If twcs $\geq$ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle.
 3. tds(MIN.) and tdh(MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	160	–	180	–	200	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	83	–	95	–	105	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	38	–	43	–	45	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	53	–	60	–	65	–	ns	1

- Note**
1. If twcs $\geq$ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If trwd $\geq$ trwd(MIN.), tcwd $\geq$ tcwd(MIN.), tawd $\geq$ tawd(MIN.) and tcpwd $\geq$ tcpwd(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t _{TRAC} = 60 ns		t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	tpc	40	–	45	–	50	–	ns	
Access Time from CAS Precharge	t _{ACP}	–	35	–	40	–	45	ns	
RAS Pulse Width	t _{RASP}	60	125 000	70	125 000	80	125 000	ns	
CAS Precharge Time	t _{CP}	10	–	10	–	10	–	ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	35	–	40	–	45	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	85	–	90	–	100	–	ns	
CAS Precharge to WE Delay Time	t _{CPWD}	58	–	65	–	70	–	ns	1

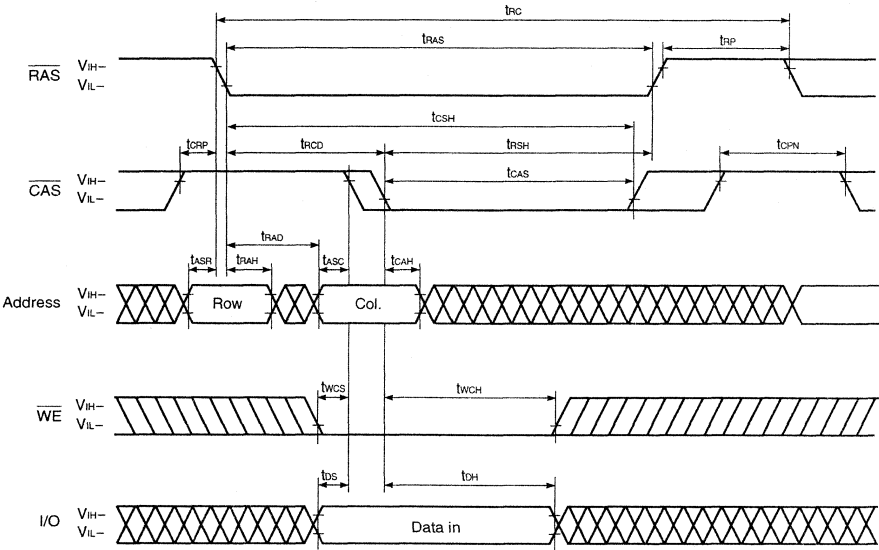
Note 1. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$ and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

Parameter	Symbol	t _{TRAC} = 60 ns		t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	–	5	–	5	–	ns	
CAS Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RASS}	100	–	100	–	100	–	μs	1
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RPS}	110	–	130	–	150	–	ns	1
CAS Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	–50	–	ns	1
WE Setup Time	t _{WSR}	10	–	10	–	10	–	ns	
WE Hold Time	t _{WHR}	15	–	15	–	15	–	ns	

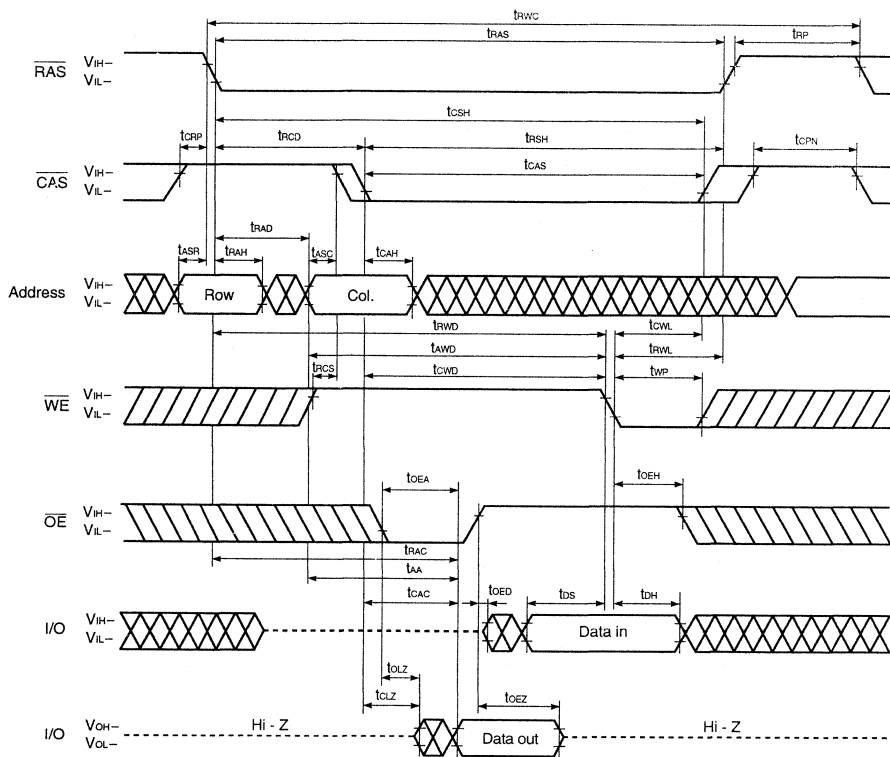
Note 1. This specification is applied only to the μPD42S16800L, 42S17800L.

Early Write Cycle



Remark OE : Don't care

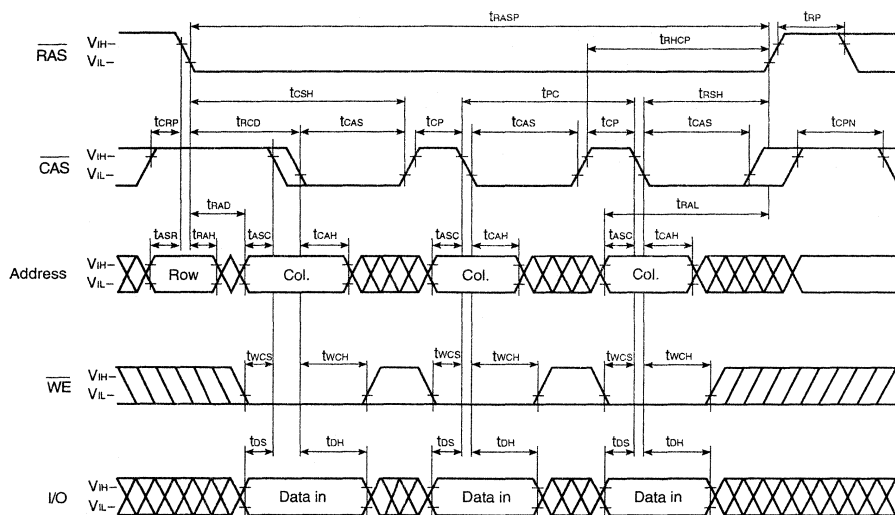
★ Read Modify Write Cycle



[illegible]

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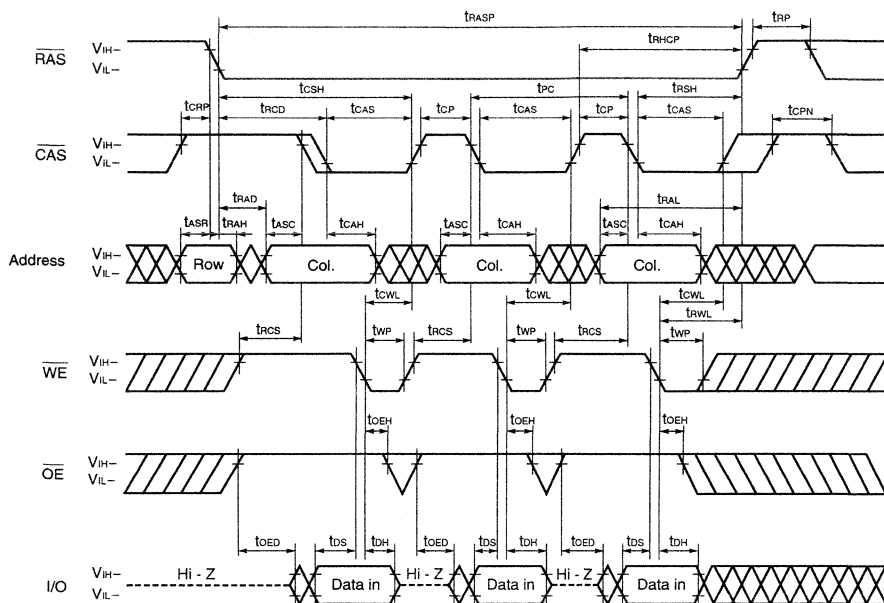
Fast Page Mode Early Write Cycle



Remark OE: Don't care

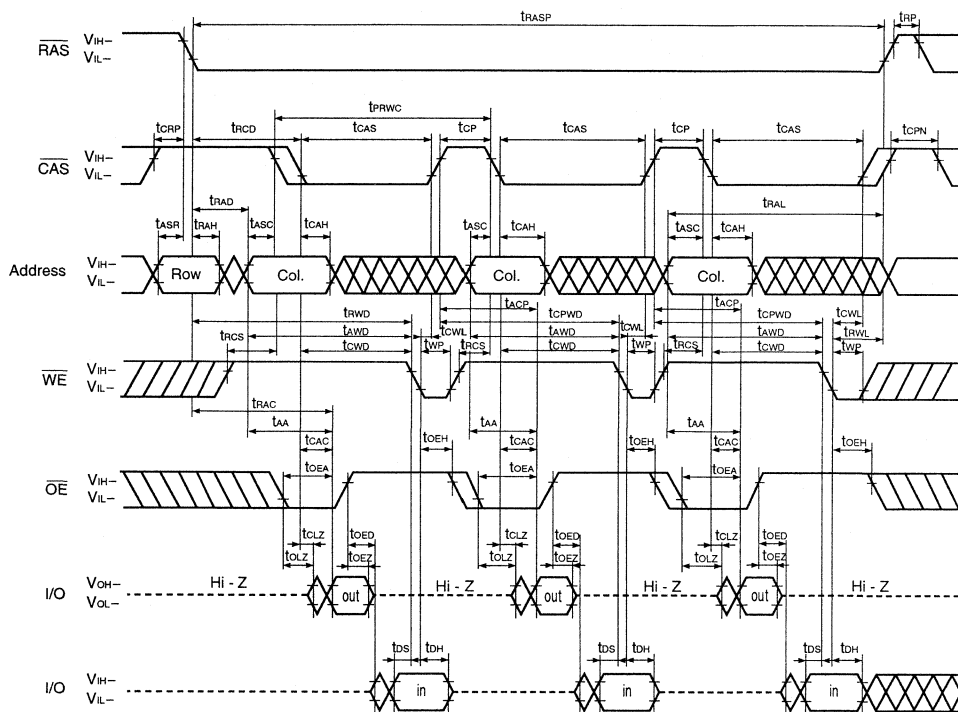
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Late Write Cycle



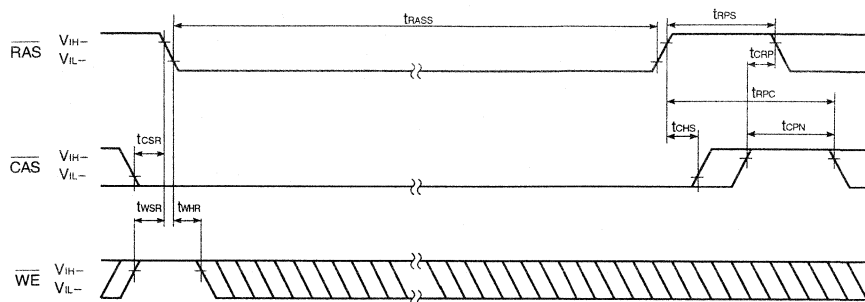
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

★ **Fast Page Mode Read Modify Write Cycle**



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle (Only for the μ PD42S16800L, 42S17800L)



Remark Address, $\overline{OE}$: Don't care I/O : Hi - Z

Cautions on Use of CAS Before RAS Self Refresh



CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16800L : 4 096 times within a 64 ms interval

μ PD42S17800L : 2 048 times within a 32 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

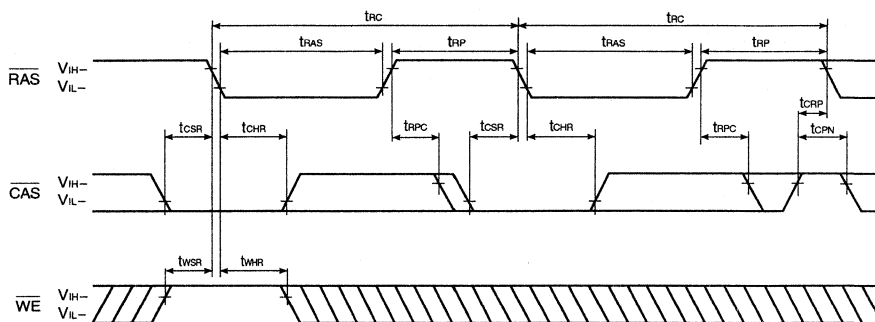
When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16800L : 4 096 times within a 64 ms interval

μ PD42S17800L : 2 048 times within a 32 ms interval

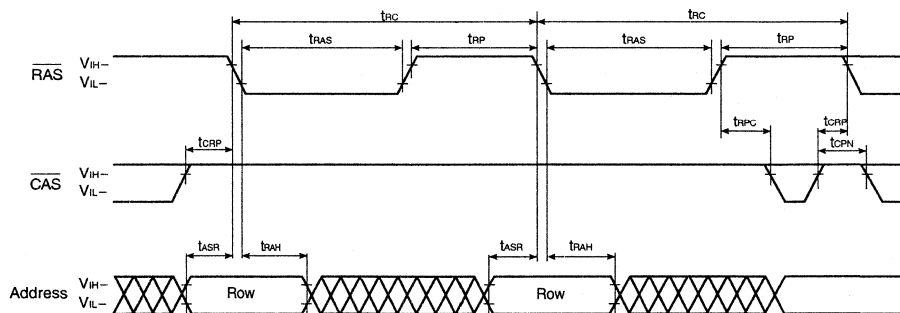
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



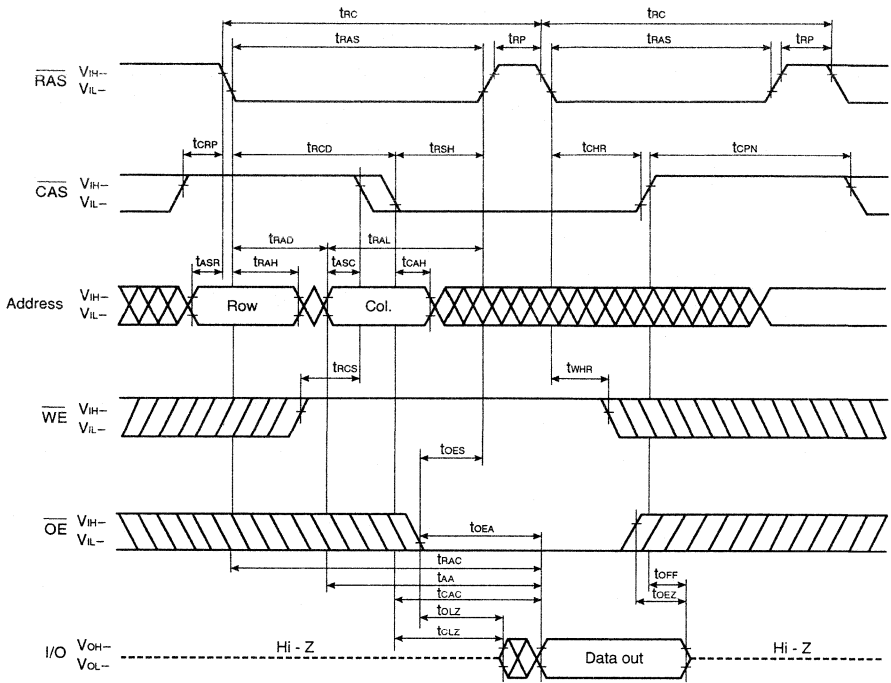
Remark Address, $\overline{OE}$: Don't care I/O: Hi - Z

RAS Only Refresh Cycle

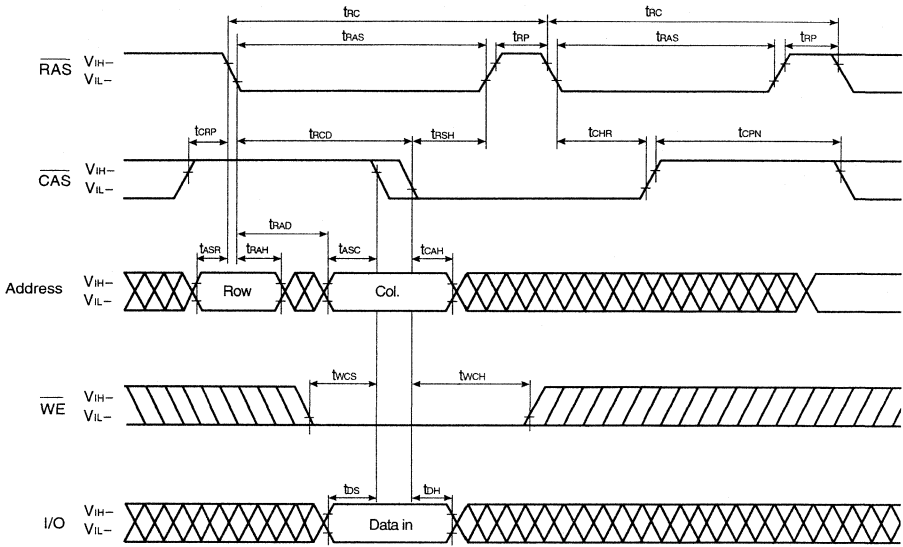


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi - Z

Hidden Refresh Cycle (Read)

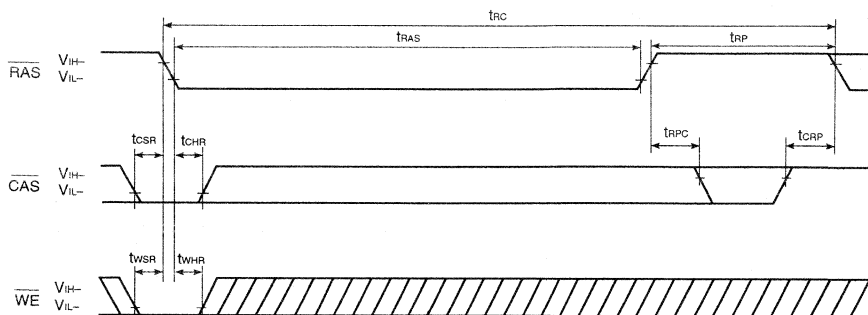


★ Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)



Remark Address, $\overline{\text{OE}}$: Don't care I/O : Hi - Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 16$ -bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output="1": Normal write (all memory cells)

Output="0": Abnormal write

(3) Refresh

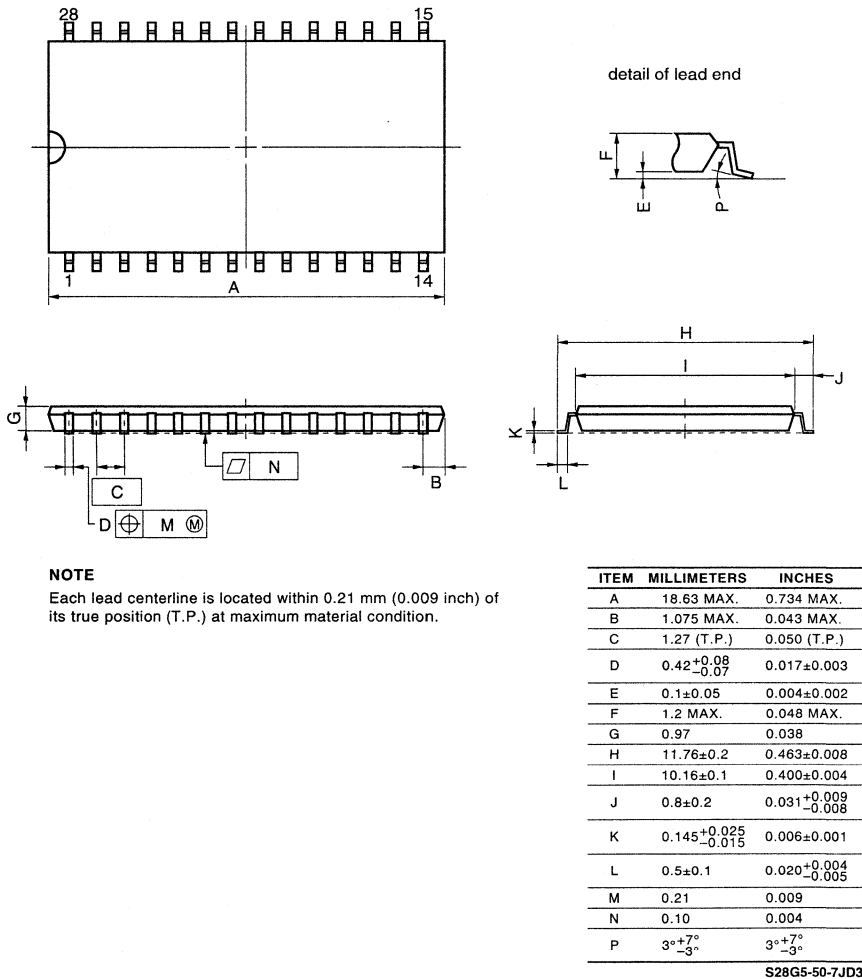
Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

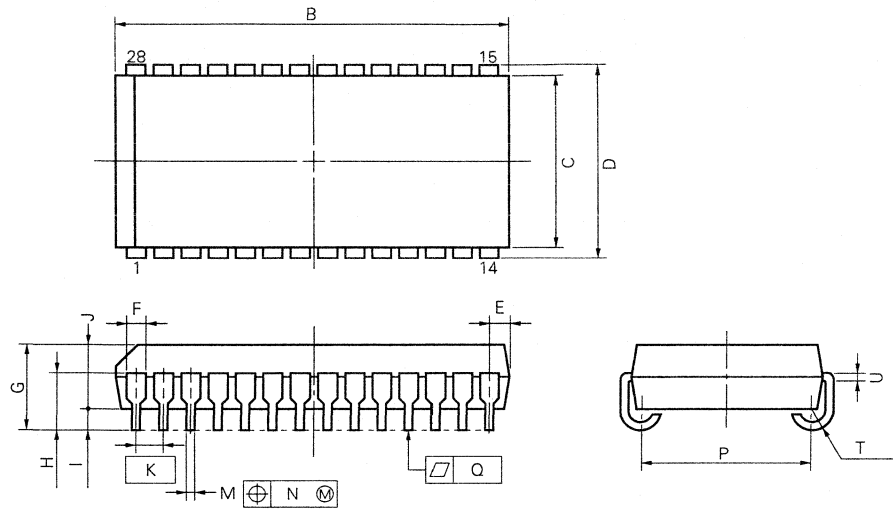
The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

★ Package Drawings

28PIN PLASTIC TSOP(II) (400 mil)



28 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LE-400A1

ITEM	MILLIMETERS	INCHES
B	18.67 ^{+0.2} _{-0.35}	0.735 ^{+0.008} _{-0.013}
C	10.16	0.400
D	11.18±0.2	0.440 ^{+0.008} _{-0.007}
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138 ^{+0.008} _{-0.007}
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.40±0.20	0.370 ^{+0.008} _{-0.007}
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

★ Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S16800L, 4216800L, 42S17800L, 4217800L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16800LG5, 4216800LG5, 42S17800LG5, 4217800LG5: 28-pin plastic TSOP(II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-107-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S16800LLE, 4216800LLE, 42S17800LLE, 4217800LLE: 28-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μ PD42S16805L, 4216805L**3.3 V OPERATION 16 M-BIT DYNAMIC RAM
2 M-WORD BY 8-BIT, HYPER PAGE MODE****Description**

The μ PD42S16805L, 4216805L are 2 097 152 words by 8 bits dynamic CMOS RAMs with optional hyper page mode.

Hyper page mode is a kind of the page mode and is useful for the read operation.

The μ PD42S16805L, 4216805L are packed in 28-pin plastic TSOP(III) and 28-pin plastic SOJ.

Features

- Hyper page mode
- Single +3.3 V $\pm$ 0.3 V power supply
- 2 097 152 words by 8 bits organization

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μ PD42S16805L-A60, 4216805L-A60	60 ns	104 ns	25 ns
μ PD42S16805L-A70, 4216805L-A70	70 ns	124 ns	30 ns

- μ PD42S16805L can execute CAS before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh
μ PD42S16805L	4 096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4216805L	4 096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh

The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD42S16805LG5-A60-7JD	60 ns	28-pin Plastic TSOP(II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S16805LG5-A70-7JD	70 ns		
μPD42S16805LG5-A60-7KD	60 ns	28-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD42S16805LG5-A70-7KD	70 ns		
μPD42S16805LLE-A60	60 ns	28-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S16805LLE-A70	70 ns		
μPD4216805LG5-A60-7JD	60 ns	28-pin Plastic TSOP (II) (400 mil)	
μPD4216805LG5-A70-7JD	70 ns		
μPD4216805LG5-A60-7KD	60 ns	28-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD4216805LG5-A70-7KD	70 ns		
μPD4216805LLE-A60	60 ns	28-pin Plastic SOJ (400 mil)	
μPD4216805LLE-A70	70 ns		

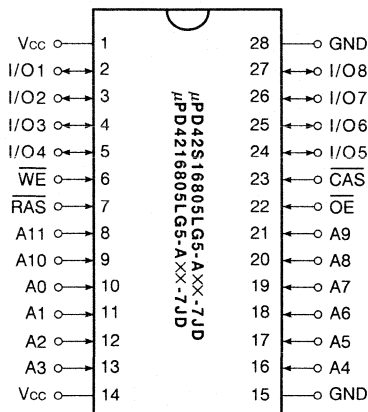
Quality Grade

Standard

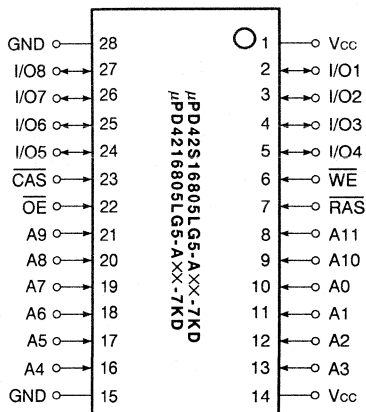
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number I EI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking side)

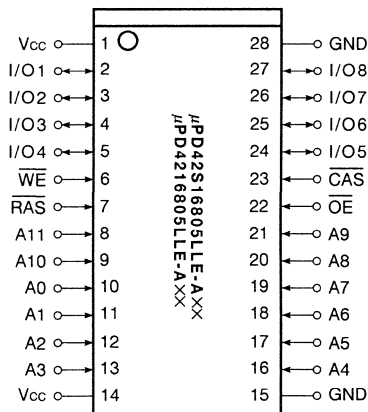
28-pin Plastic TSOP (II) (400 mil)



Reverse bent

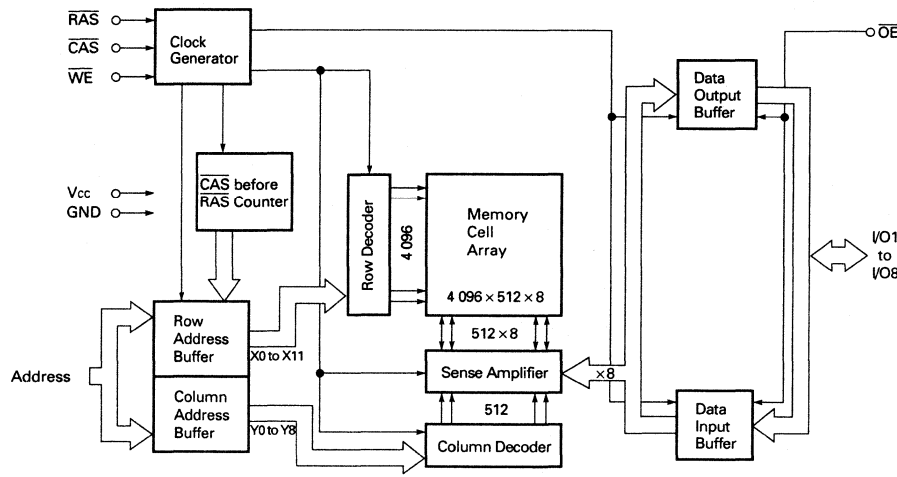


28-pin Plastic SOJ (400 mil)



- A0 to A11 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground

Block Diagram



Input/Output Pin Functions

The μPD42S16805L, 4216805L have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11 and input/output pins I/O1 to I/O8.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)		Address bus. Input total 21-bit of address signal, upper 12-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 2 097 152-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input/ Output	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)		8-bit data bus. I/O1 to I/O8 are used to input/output data.

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

In the hyper page mode, the output data is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

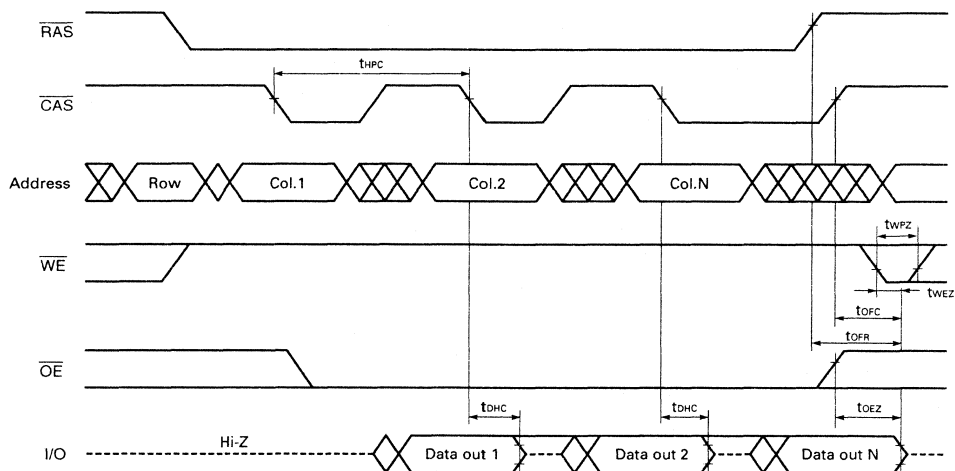
2. The $\overline{\text{CAS}}$ cycle time in the hyper page mode is shorter than that in the fast page mode.

In the hyper page mode, due to the data extend function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{\text{CAS}}$ cycle time in the hyper page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{\text{RAS}}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

Hyper Page Mode Read Cycle



To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.

- (1) $\overline{\text{RAS}}$, $\overline{\text{CAS}}$: inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

- (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$: active, $\overline{\text{OE}}$: active... t_{WEZ} , t_{WPZ} are effective.

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: inactive... t_{OEZ} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-0.5 to +4.6	V
Supply Voltage	V_{CC}		-0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55 to +125	$^{\circ}\text{C}$

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low Level Input Voltage	V_{IL}		-0.3		+0.8	V
Ambient Temperature	T_a		0		70	$^{\circ}\text{C}$

Capacitance ($T_a = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

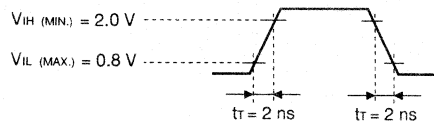
Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		80	mA	1,2,3
				$t_{\text{RAC}} = 70 \text{ ns}$		70		
Standby current	$\mu\text{PD42S16805L}$	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), I_o = 0 \text{ mA}$			0.5	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_o = 0 \text{ mA}$			0.15		
	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), I_o = 0 \text{ mA}$			2				
	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_o = 0 \text{ mA}$			0.5				
$\overline{\text{RAS}}$ only refresh current		I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		80	mA	1,2,3,4
				$t_{\text{RAC}} = 70 \text{ ns}$		70		
Operating current (Hyper page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ $\overline{\text{CAS}}$ Cycling $t_{\text{HPC}} = t_{\text{HPC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		90	mA	1,2,5
				$t_{\text{RAC}} = 70 \text{ ns}$		80		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		80	mA	1,2
				$t_{\text{RAC}} = 70 \text{ ns}$		70		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (4 096 Cycles / 128 ms, only for the $\mu\text{PD42S16805L}$)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: 4 096 Cycles / 128 ms $\overline{\text{RAS}}, \overline{\text{CAS}} :$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby : $\overline{\text{RAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : V_{IH} or V_{IL} $\overline{\text{WE}}, \overline{\text{OE}} : V_{\text{IH}}$ $I_o = 0 \text{ mA}$		$t_{\text{RAS}} \leq 1 \mu\text{s}$	220	μA	1,2
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for the $\mu\text{PD42S16805L}$)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}} :$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$			150	μA	2
Input leakage current		I _{I (L)}	$V_i = 0 \text{ to } 3.6 \text{ V}$ all other pins not under test = 0 V		-5	+5	μA	
Output leakage current		I _{O (L)}	$V_o = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)		-5	+5	μA	
High level output voltage		V _{OH}	$I_o = -2.0 \text{ mA}$		2.4		V	
Low level output voltage		V _{OL}	$I_o = +2.0 \text{ mA}$			0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

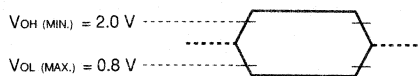
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	trAC = 60 ns		trAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		trC	104	–	124	–	ns	
RAS Precharge Time		trP	40	–	50	–	ns	
CAS Precharge Time		tCPN	10	–	10	–	ns	
RAS Pulse Width		trAS	60	10 000	70	10 000	ns	
CAS Pulse Width		tCAS	10	10 000	12	10 000	ns	
RAS Hold Time		trSH	10	–	12	–	ns	
CAS Hold Time		tCSH	40	–	50	–	ns	
RAS to CAS Delay Time		trCD	14	45	14	52	ns	1
RAS to Column Address Delay Time		trAD	12	30	12	35	ns	1
CAS to RAS Precharge Time		tCRP	5	–	5	–	ns	2
Row Address Setup Time		tASR	0	–	0	–	ns	
Row Address Hold Time		trAH	10	–	10	–	ns	
Column Address Setup Time		tASC	0	–	0	–	ns	
Column Address Hold Time		tCAH	10	–	12	–	ns	
OE Lead Time Referenced to RAS		tOES	0	–	0	–	ns	
CAS to Data Setup Time		tCLZ	0	–	0	–	ns	
OE to Data Setup Time		tOLZ	0	–	0	–	ns	
OE to Data Delay Time		tOED	13	–	15	–	ns	
Transition Time (Rise and Fall)		tT	1	50	1	50	ns	
Refresh Time	μPD42S16805L	tREF	–	128	–	128	ms	3
	μPD4216805L		–	64	–	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD (MAX.) and trCD (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

2. tCRP (MIN.) requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
3. This specification is applied only to the μ PD42S16805L.

Read Cycle

Parameter	Symbol	$\text{trAC} = 60 \text{ ns}$		$\text{trAC} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	trAC	–	60	–	70	ns	1
Access Time from $\overline{\text{CAS}}$	tCAC	–	15	–	18	ns	1
Access Time from Column Address	tAA	–	30	–	35	ns	1
Access Time from $\overline{\text{OE}}$	tOEA	–	15	–	18	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	trAL	30	–	35	–	ns	
Read Command Setup Time	trCS	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	trRH	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	trCH	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD (MAX.) and trCD (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

2. Either trCH (MIN.) or trRH (MIN.) should be met in read cycles.
3. tOEZ (MAX.) defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
WE Hold Time Referenced to $\overline{\text{CAS}}$	twCH	10	–	10	–	ns	1
WE Pulse Width	tWP	10	–	10	–	ns	1
WE Lead Time Referenced to $\overline{\text{RAS}}$	trWL	10	–	12	–	ns	
WE Lead Time Referenced to $\overline{\text{CAS}}$	tcWL	10	–	12	–	ns	
WE Setup Time	twCS	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toEH	0	–	0	–	ns	
Data-in Setup Time	tDS	0	–	0	–	ns	3
Data-in Hold Time	tDH	10	–	10	–	ns	3

- Notes**
1. tWP(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twCH(MIN.) should be met.
 2. If twCS $\geq$ twCS(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. tDS(MIN.) and tDH(MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the WE falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trWC	133	–	157	–	ns	
$\overline{\text{RAS}}$ to WE Delay Time	trWD	77	–	89	–	ns	1
$\overline{\text{CAS}}$ to WE Delay Time	tcWD	32	–	37	–	ns	1
Column Address to WE Delay Time	tAWD	47	–	54	–	ns	1

- Note 1.** If twCS $\geq$ twCS(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trWD $\geq$ trWD(MIN.), tcWD $\geq$ tcWD(MIN.), tAWD $\geq$ tAWD(MIN.), and tcpWD $\geq$ tcpWD(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{HPC}	25	–	30	–	ns	
RAS Pulse Width	t _{RASP}	60	125 000	70	125 000	ns	
CAS Pulse Width	t _{HCAS}	10	10 000	12	10 000	ns	
CAS Precharge Time	t _{CP}	10	–	10	–	ns	
Access Time from CAS Precharge	t _{ACP}	–	35	–	40	ns	
CAS Precharge to $\overline{WE}$ Delay Time	t _{CPWD}	52	–	59	–	ns	1
RAS Hold Time from CAS Precharge	t _{RHCP}	35	–	40	–	ns	
Read Modify Write Cycle Time	t _{HPRWC}	66	–	75	–	ns	
Data Output Hold Time	t _{DHC}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t _{WEZ}	0	13	0	15	ns	2,3
$\overline{WE}$ Pulse Width	t _{WPZ}	10	–	10	–	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t _{OFR}	0	13	0	15	ns	2,3
Output Buffer Turn-off Delay from $\overline{CAS}$	t _{OFc}	0	13	0	15	ns	2,3

Notes 1. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RDW} \geq t_{RDW(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$, and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

2. $t_{OFc(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)

$\overline{WE}$: inactive, $\overline{OE}$: active

t_{OFc} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)

$\overline{WE}$: active, $\overline{OE}$: active ... t_{WEZ}, t_{WPZ} are effective.

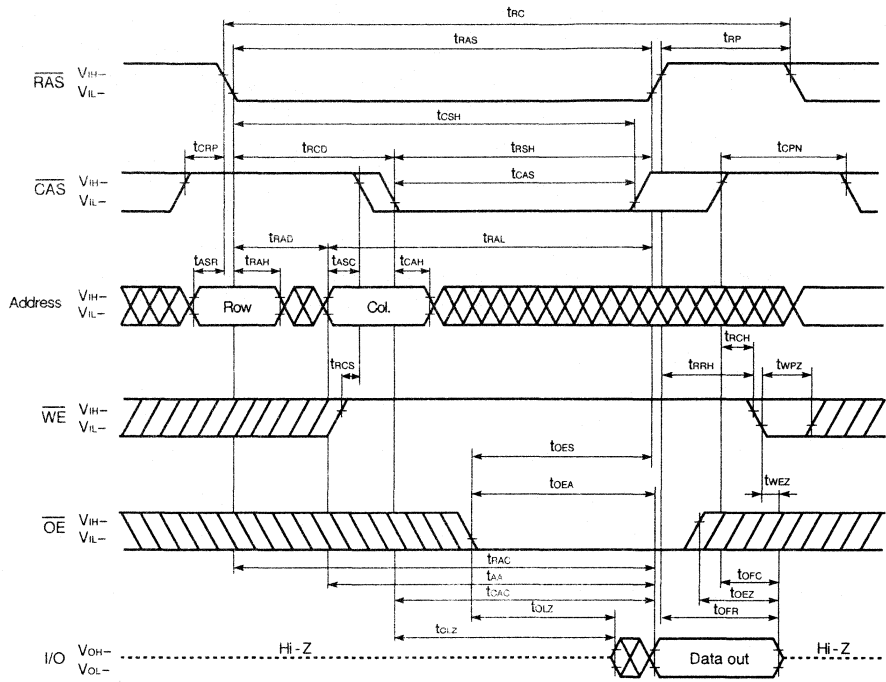
$\overline{WE}$: inactive, $\overline{OE}$: inactive ... t_{OEZ} is effective.

Refresh Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	–	5	–	ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10	–	10	–	ns	
RAS Precharge CAS Hold Time	t _{RPC}	5	–	5	–	ns	
RAS Pulse Width (CAS before RAS Self Refresh)	t _{RASS}	100	–	100	–	μ s	1
RAS Precharge Time (CAS before RAS Self Refresh)	t _{RPS}	110	–	130	–	ns	1
CAS Hold Time (CAS before RAS Self Refresh)	t _{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ Setup Time	t _{WSR}	10	–	10	–	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t _{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μ PD42S16805L.

Read Cycle



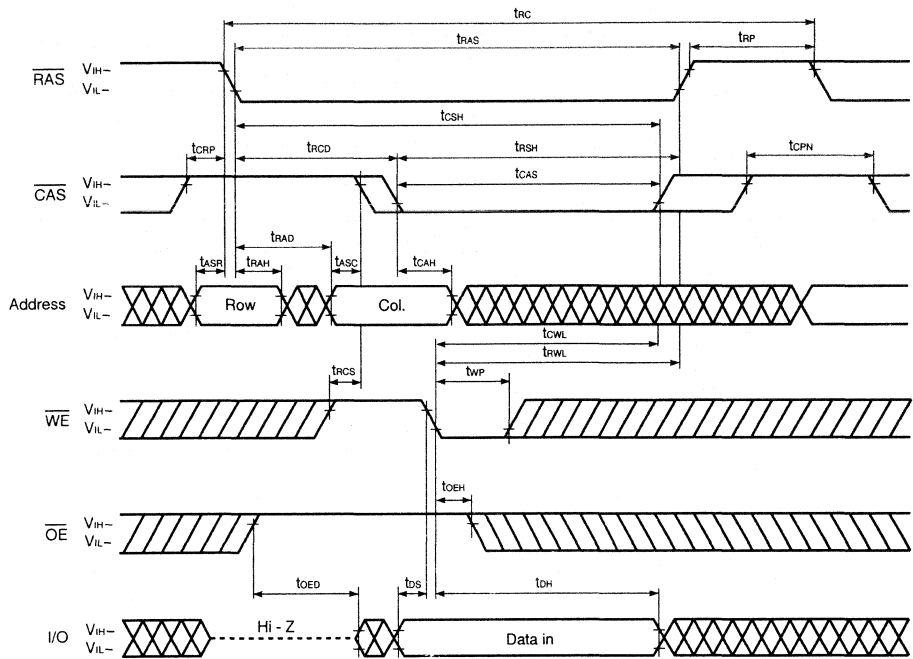
The diagram illustrates the timing relationships for a 256Kbit DRAM. The signals shown are RAS, CAS, Address, WE, and I/O. The timing parameters are defined as follows:

- RAS:** t_{RAS} (RAS access time), t_{RSH} (RAS hold time), t_{RCP} (RAS precharge time), t_{RPH} (RAS precharge hold time).
- CAS:** t_{CAS} (CAS access time), t_{CSH} (CAS hold time), t_{CPH} (CAS precharge hold time), t_{CRP} (CAS precharge time).
- Address:** t_{ASR} (Address setup time), t_{AH} (Address hold time), t_{ASC} (Address setup time to CAS), t_{CAH} (CAS hold time).
- WE:** t_{WCS} (Write enable setup time), t_{WH} (Write enable hold time).
- I/O:** t_{DS} (Data setup time), t_{DH} (Data hold time).

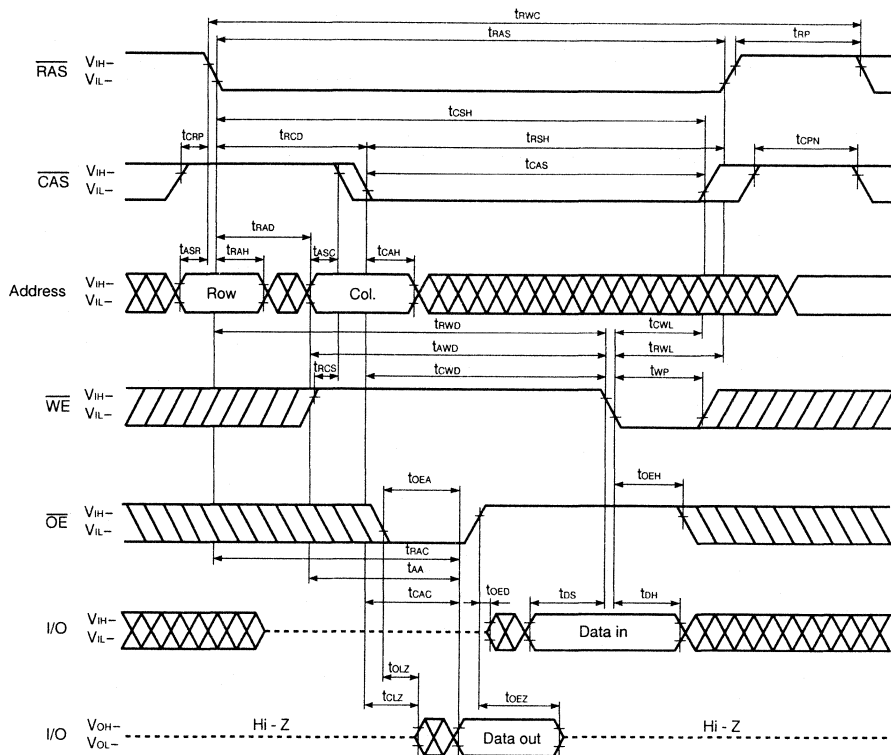
The diagram also shows the internal structure of the DRAM, including the Row and Column address decoders, and the Data in signal.

Remark $\overline{OE}$: Don't care

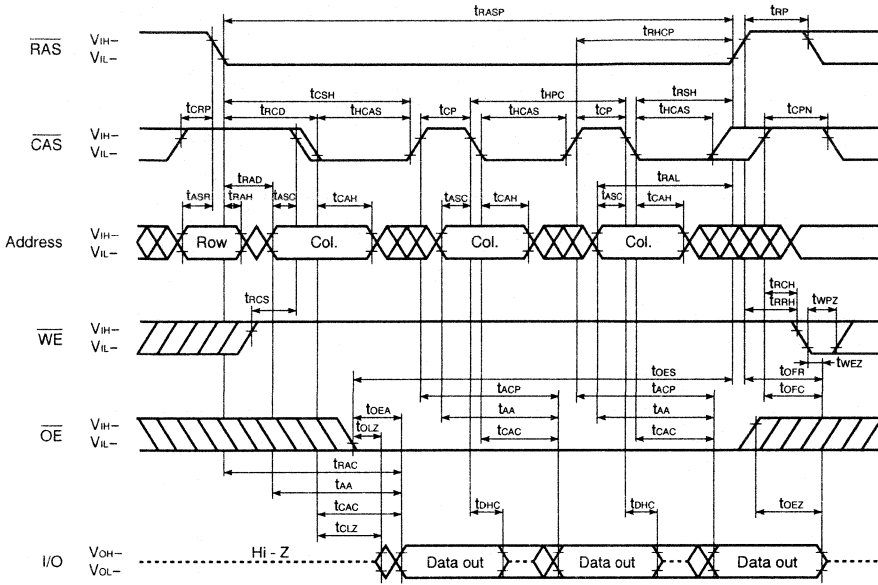
Late Write Cycle



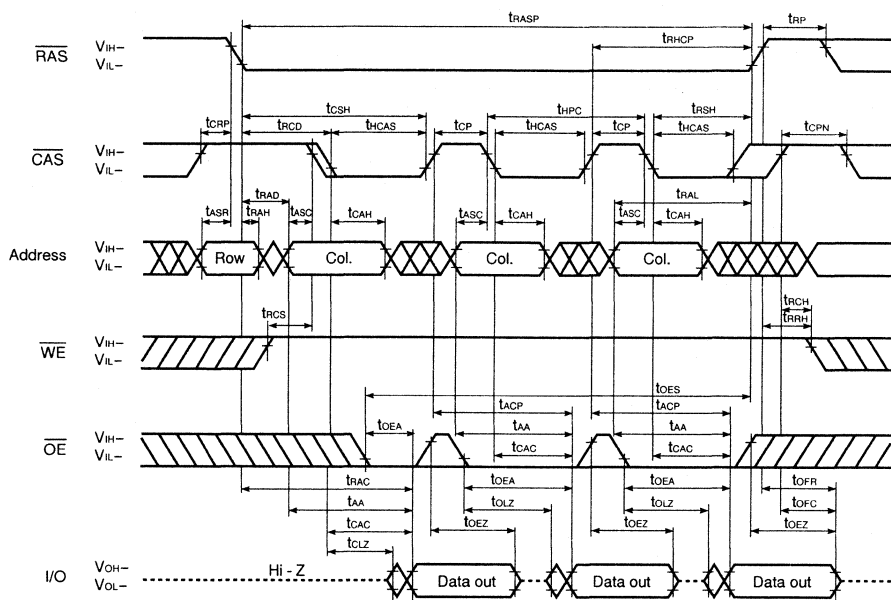
Read Modify Write Cycle



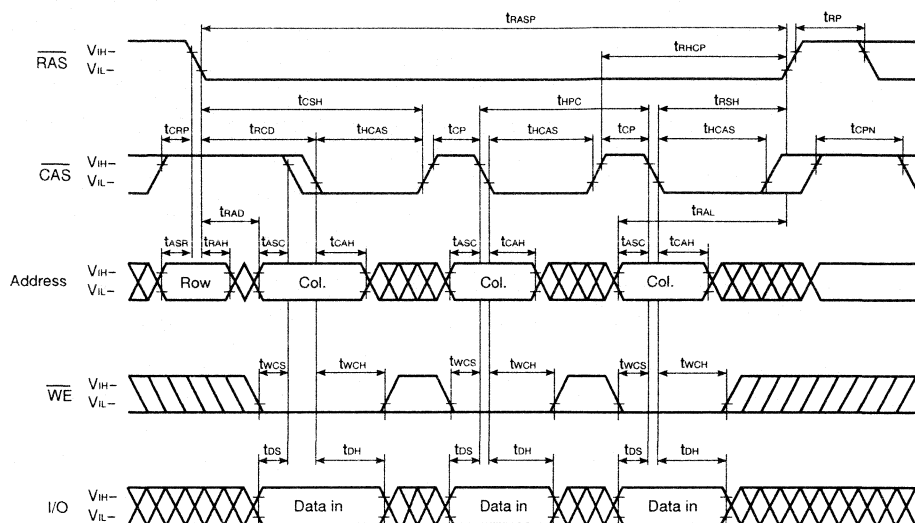
Hyper Page Mode Read Cycle



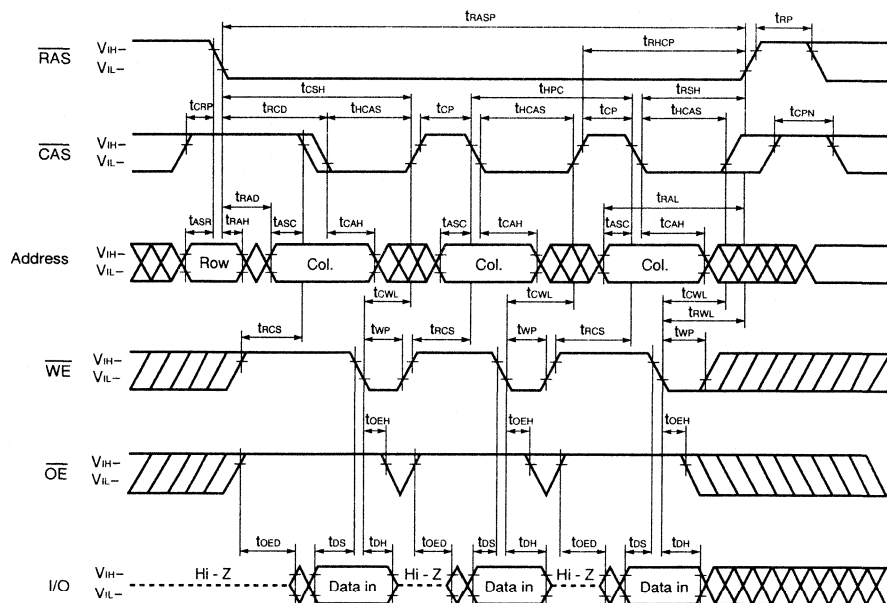
Hyper Page Mode Read Cycle ($\overline{\text{OE}}$ Control)

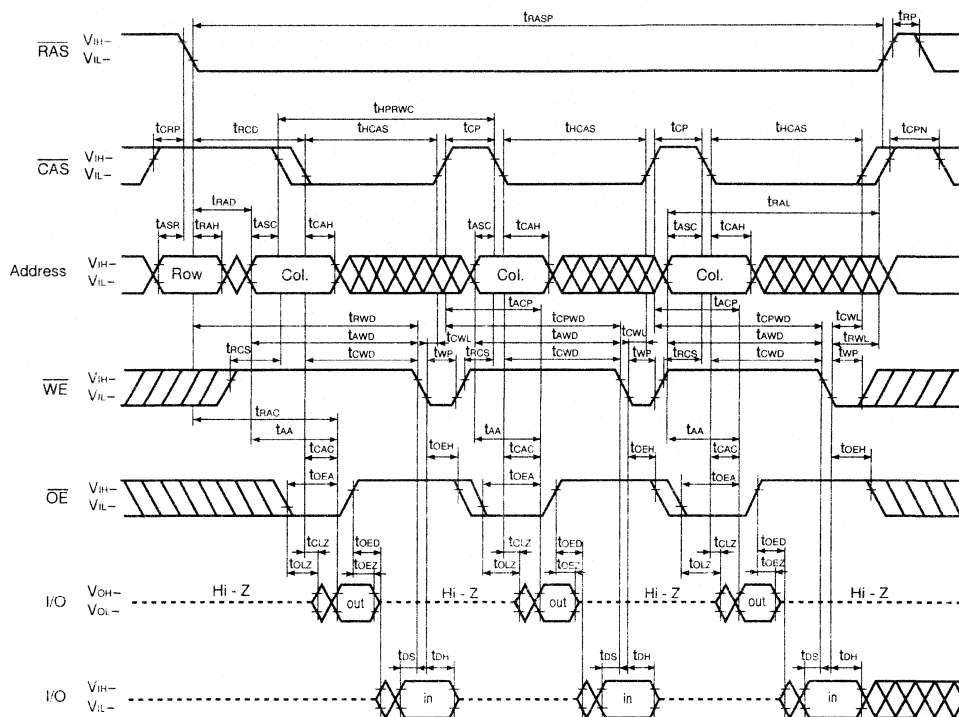


Hyper Page Mode Early Write Cycle

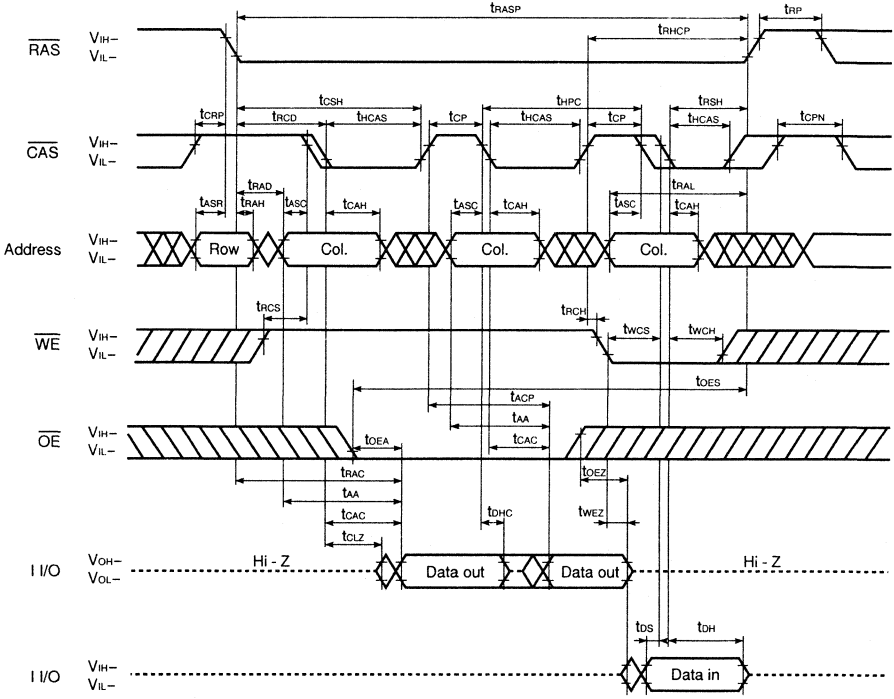


Remark $\overline{\text{OE}}$: Don't care

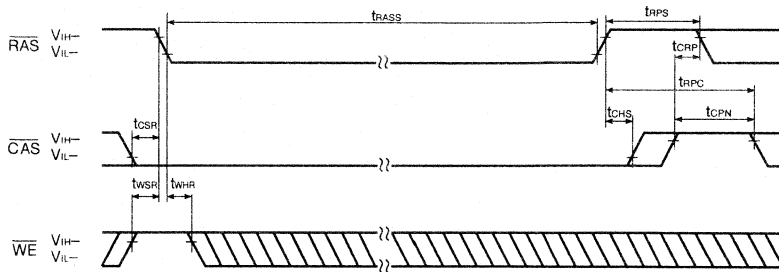




Hyper Page Mode Read and Write Cycle



CAS Before RAS Self Refresh Cycle (Only for the μPD42S16805L)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

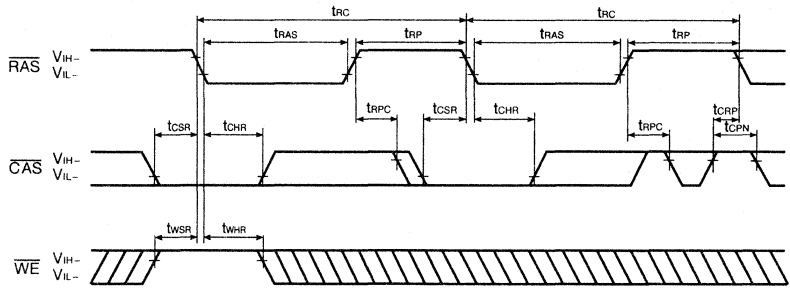
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 4 096 times within a 64 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh 4 096 times within an interval of 64 ms or less just before and after setting CAS before RAS self refresh.

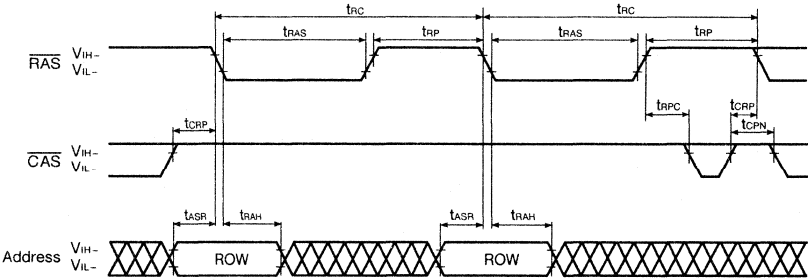
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



Remark Address, $\overline{\text{OE}}$ = Don't care I/O = Hi - Z

RAS Only Refresh Cycle



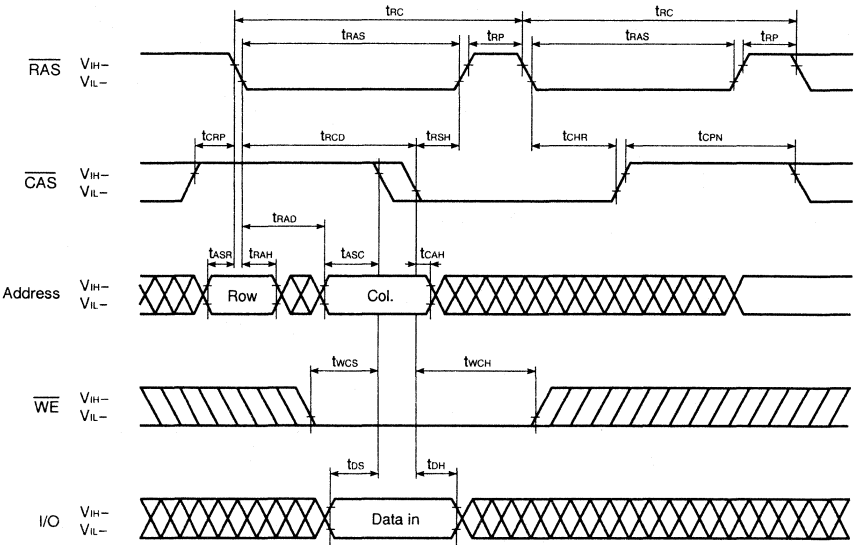
Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$ = Don't care I/O = Hi - Z

The diagram illustrates the timing relationships for a 64K16 DRAM. The signals and their timing parameters are as follows:

- RAS**: V_{IH} to V_{IL} transition. Timing parameters: t_{RAC} (Row Access Cycle), t_{RAS} (Row Access Strobe), t_{RP} (Row Precharge Time).
- CAS**: V_{IH} to V_{IL} transition. Timing parameters: t_{CRP} (Column Precharge Time), t_{RCD} (Row to Column Delay), t_{RSH} (Row to Strobe Hold), t_{CHR} (Column to Row Hold), t_{CPN} (Column Precharge Noise).
- Address**: V_{IH} to V_{IL} transition. Timing parameters: t_{ASR} (Address Strobe Rise), t_{RAH} (Row Address Hold), t_{ASC} (Address to Column), t_{CAH} (Column Address Hold).
- WE**: V_{IH} to V_{IL} transition. Timing parameters: t_{RCS} (Row to Column Strobe), t_{WHR} (Write Hold).
- OE**: V_{IH} to V_{IL} transition. Timing parameters: t_{OES} (Output Enable Strobe), t_{OEA} (Output Enable Active), t_{OFR} (Output Full Rate).
- I/O**: V_{OH} to V_{OL} transition. Timing parameters: t_{RAC} (Row Access Cycle), t_{AA} (Access to Array), t_{CAC} (Column Access Cycle), t_{CAZ} (Column Address to Z), t_{CIZ} (Column to Z), t_{FC} (Full Cycle), t_{OZ} (Output to Z).

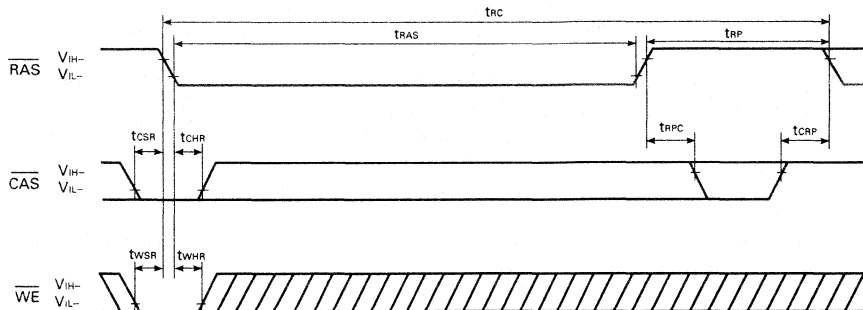
The diagram also shows the data bus state: **Hi - Z** (High Impedance) and **Data Out**.

Hidden Refresh Cycle (Write)



Remark OE : Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 16$ -bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output="1": Normal write (all memory cells)

Output="0": Abnormal write

(3) Refresh

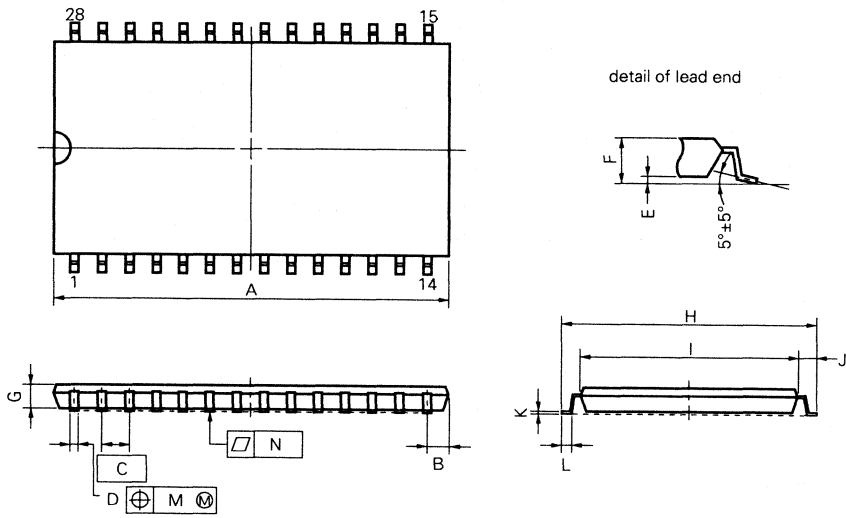
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

28 PIN PLASTIC TSOP(II) (400 mil)

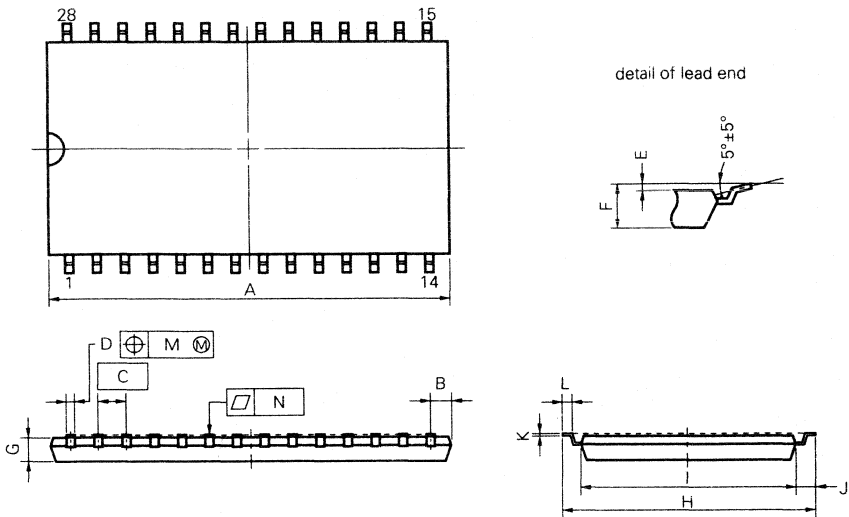


NOTE
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD2-1

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP(III) (400 mil)



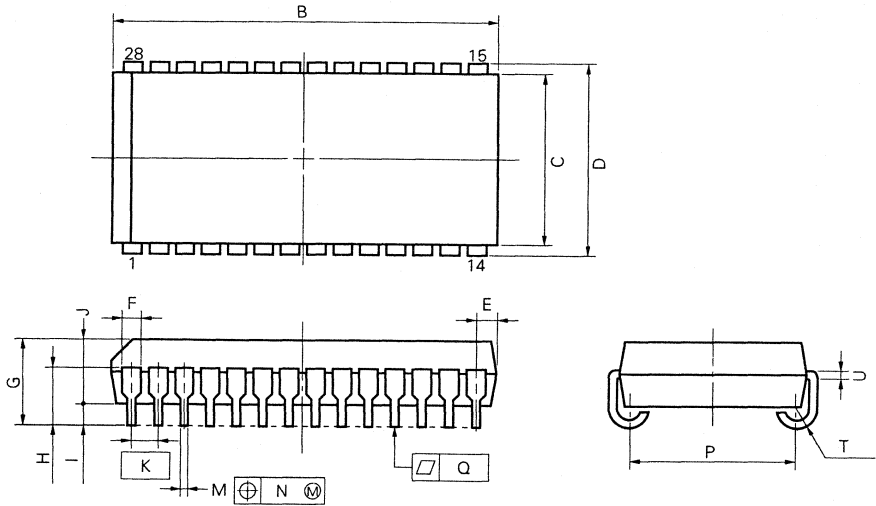
S28G5-50-7KD2-1

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LE-400A1

ITEM	MILLIMETERS	INCHES
B	18.67 ^{+0.2} _{-0.35}	0.735 ^{+0.008} _{-0.013}
C	10.16	0.400
D	11.18±0.2	0.440 ^{+0.008} _{-0.007}
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138 ^{+0.008} _{-0.007}
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.40±0.20	0.370 ^{+0.008} _{-0.007}
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD42S16805L, 4216805L.

Types of Surface Mount Device

μPD42S16805LG5-A××-7JD, 4216805LG5-A××-7JD : 28-pin Plastic TSOP (II) (400 mil)

μPD42S16805LG5-A××-7KD, 4216805LG5-A××-7KD : 28-pin Plastic TSOP (II) (400 mil) Reverse bent

μPD42S16805LLE-A××, 4216805LLE-A×× : 28-pin Plastic SOJ (400 mil)

MOS INTEGRATED CIRCUIT

μPD42S16160L, 4216160L, 42S18160L, 4218160L

3.3 V OPERATION 16M-BIT DYNAMIC RAM

1M-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

Description

The μPD42S16160L, 4216160L, 42S18160L, 4218160L are 1 048 576 words by 16 bits dynamic CMOS RAMs.

These differ in refresh cycle and the μPD42S16160L, 42S18160L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (see the table below).

These are packed in 50-pin plastic TSOP(II) and 42-pin plastic SOJ.

Features

- 1 048 576 words by 16 bits organization
- Single +3.3 V $\pm$ 0.3 V power supply
- Fast page mode
- Byte read/write mode
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S16160L-A60, 4216160L-A60	324 mW	60 ns	110 ns	40 ns
μPD42S18160L-A60, 4218160L-A60	540 mW			
μPD42S16160L-A70, 4216160L-A70	288 mW	70 ns	130 ns	45 ns
μPD42S18160L-A70, 4218160L-A70	504 mW			
μPD42S16160L-A80, 4216160L-A80	252 mW	80 ns	150 ns	50 ns
μPD42S18160L-A80, 4218160L-A80	468 mW			

- The μPD42S16160L, 42S18160L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16160L	4 096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, hidden refresh	0.54 mW (CMOS level input)
μPD42S18160L	1 024 cycles/128 ms		
μPD4216160L	4 096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, hidden refresh	1.8 mW (CMOS level input)
μPD4218160L	1 024 cycles/16 ms		

The information in this document is subject to change without notice.

The mark ★ shows revised points.



Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD42S16160LG5-A60-7JF	60 ns	50-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S18160LG5-A60-7JF			
μ PD42S16160LG5-A70-7JF	70 ns		
μ PD42S18160LG5-A70-7JF			
μ PD42S16160LG5-A80-7JF	80 ns		
μ PD42S18160LG5-A80-7JF			
μ PD42S16160LLE-A60	60 ns	42-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S18160LLE-A60			
μ PD42S16160LLE-A70	70 ns		
μ PD42S18160LLE-A70			
μ PD42S16160LLE-A80	80 ns		
μ PD42S18160LLE-A80			
μ PD4216160LG5-A60-7JF	60 ns	50-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4218160LG5-A60-7JF			
μ PD4216160LG5-A70-7JF	70 ns		
μ PD4218160LG5-A70-7JF			
μ PD4216160LG5-A80-7JF	80 ns		
μ PD4218160LG5-A80-7JF			
μ PD4216160LLE-A60	60 ns	42-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4218160LLE-A60			
μ PD4216160LLE-A70	70 ns		
μ PD4218160LLE-A70			
μ PD4216160LLE-A80	80 ns		
μ PD4218160LLE-A80			

Quality Grade

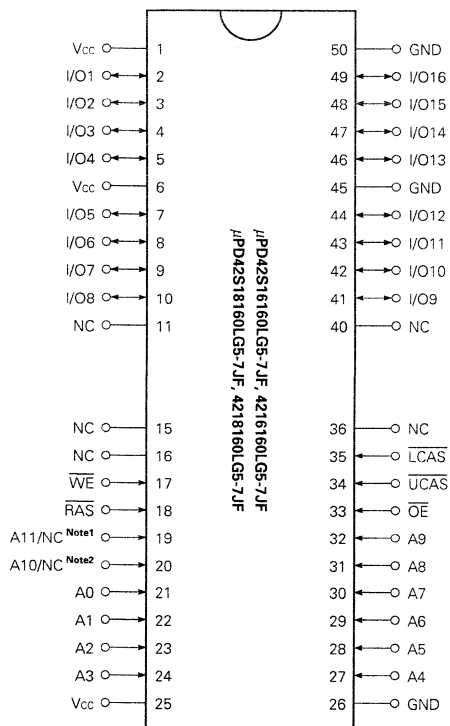
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

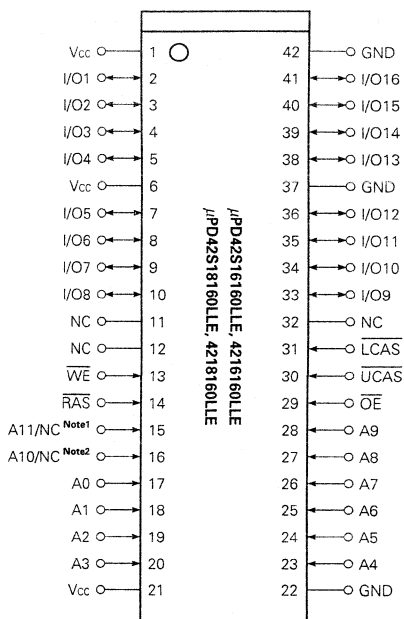
Pin Configurations (Marking Side)



50-pin Plastic TSOP (II)



42-pin Plastic SOJ

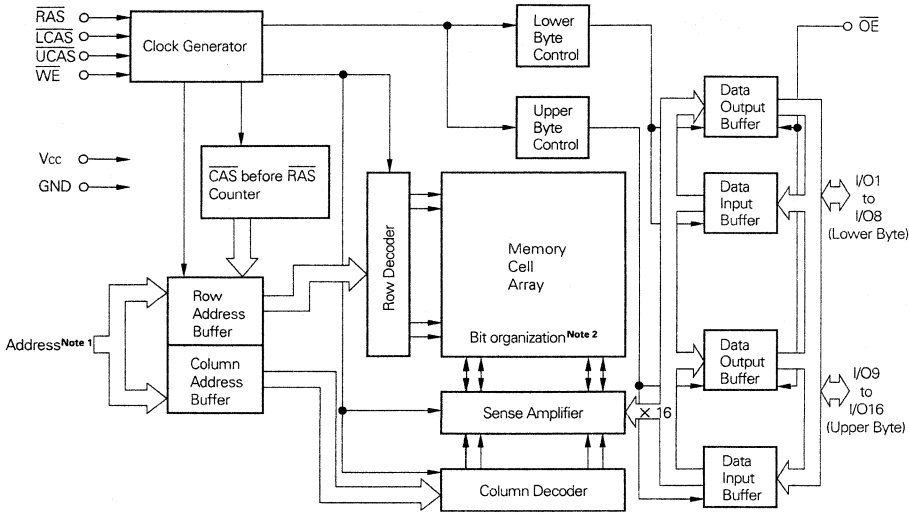


Notes 1. A11 ... μPD42S16160L, 4216160L
2. A10 ... μPD42S16160L, 4216160L

NC ... μPD42S18160L, 4218160L
NC ... μPD42S18160L, 4218160L

- A0 to A11 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
- LCAS : Column Address Strobe (lower)
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S16160L, 4216160L	A0 to A11	A0 to A7
μPD42S18160L, 4218160L	A0 to A9	A0 to A9

2. μPD42S16160L, 4216160L ... 4 096 × 256 × 16 μPD42S18160L, 4218160L ... 1 024 × 1 024 × 16

Input/Output Pin Functions

The μ PD42S16160L, 4216160L, 42S18160L, 4218160L have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ^{Note1}, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11/A9 ^{Note2} and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11/A9 ^{Note2} (Address inputs)		Address bus. Input total 20-bit of address signal, upper 12/10 ^{Note3} -bit and lower 8/10 ^{Note4} -bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t _{ASR} , t _{ASC}) and hold time (t _{RAH} , t _{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Notes 1. $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.

2. A11 ... μ PD42S16160L, 4216160L A9 ... μ PD42S18160L, 4218160L

3. 12 ... μ PD42S16160L, 4216160L 10 ... μ PD42S18160L, 4218160L

4. 8 ... μ PD42S16160L, 4216160L 10 ... μ PD42S18160L, 4218160L

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		- 0.5 to +4.6	V
Supply voltage	V_{CC}		- 0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	$^{\circ}\text{C}$
Storage temperature	T_{stg}		- 55 to +125	$^{\circ}\text{C}$

Caution Exposing the device to stress above those listed in **Absolute Maximum Ratings** could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to **Absolute Maximum Rating** conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		- 0.3		+0.8	V
Ambient temperature	T_a		0		70	$^{\circ}\text{C}$

Capacitance ($T_a = +25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A11			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1 to I/O16			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[μ PD42S16160L, 4216160L]

Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	RAS, CAS Cycling tr _C = tr _C (MIN.) I _O = 0 mA	tr _{AC} = 60 ns	90	mA	1,2,3
				tr _{AC} = 70 ns	80		
				tr _{AC} = 80 ns	70		
Standby current	μ PD42S16160L	I _{CC2}	RAS, CAS $\geq V_{IH}$ (MIN.) I _O = 0 mA		0.5	mA	
			RAS, CAS $\geq V_{CC} - 0.2$ V	I _O = 0 mA	0.15		
	μ PD4216160L		RAS, CAS $\geq V_{IH}$ (MIN.) I _O = 0 mA		2		
			RAS, CAS $\geq V_{CC} - 0.2$ V	I _O = 0 mA	0.5		
RAS only refresh current		I _{CC3}	RAS Cycling CAS $\geq V_{IH}$ (MIN.) tr _C = tr _C (MIN.) I _O = 0 mA	tr _{AC} = 60 ns	90	mA	1,2,3,4
				tr _{AC} = 70 ns	80		
				tr _{AC} = 80 ns	70		
Operating current (Fast page mode)		I _{CC4}	RAS $\leq V_{IL}$ (MAX.) CAS Cycling tr _C = tr _C (MIN.) I _O = 0 mA	tr _{AC} = 60 ns	90	mA	1,2,5
				tr _{AC} = 70 ns	80		
				tr _{AC} = 80 ns	70		
CAS before RAS refresh current		I _{CC5}	RAS Cycling tr _C = tr _C (MIN.) I _O = 0 mA	tr _{AC} = 60 ns	90	mA	1,2
				tr _{AC} = 70 ns	80		
				tr _{AC} = 80 ns	70		
CAS before RAS long refresh current (4 096 cycles / 128 ms, only for μ PD42S16160L)		I _{CC6}	CAS before RAS refresh : 4 096 cycles/128 ms RAS, CAS : $V_{CC}-0.2$ V $\leq V_{IH} \leq V_{IH(MAX)}$ 0 V $\leq V_{IL} \leq 0.2$ V Standby : RAS $\geq V_{CC}-0.2$ V Address : Don't care WE, OE : V _{IH} I _O = 0 mA	tr _{AS} ≤ 1 μ s	220	μ A	1,2
Self refresh current (CAS before RAS self refresh, only for μ PD42S16160L)		I _{CC7}	RAS, CAS : $V_{CC}-0.2$ V $\leq V_{IH} \leq V_{IH(MAX)}$ 0 V $\leq V_{IL} \leq 0.2$ V I _O = 0 mA		150	μ A	2
Input leakage current		I _{I(L)}	V _I = 0 to 3.6 V all other pins not under test = 0 V	-5	+5	μ A	
Output leakage current		I _{O(L)}	Output is disabled (Hi-Z) V _O = 0 to 3.6 V	-5	+5	μ A	
High level output voltage		V _{OH}	I _O = -2.0 mA	2.4		V	
Low level output voltage		V _{OL}	I _O = 2.0 mA		0.4	V	

[μ PD42S18160L, 4218160L]

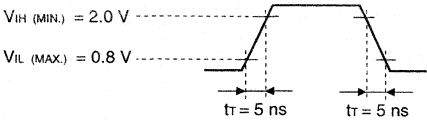
Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trAC} = 60 \text{ ns}$	150	mA	1,2,3
				$\text{trAC} = 70 \text{ ns}$	140		
				$\text{trAC} = 80 \text{ ns}$	130		
Standby current	μ PD42S18160L	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$		0.5	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ $\text{I}_\text{O} = 0 \text{ mA}$		0.15		
	μ PD4218160L		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$		2		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ $\text{I}_\text{O} = 0 \text{ mA}$		0.5		
RAS only refresh current		I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trAC} = 60 \text{ ns}$	150	mA	1,2,3,4
				$\text{trAC} = 70 \text{ ns}$	140		
				$\text{trAC} = 80 \text{ ns}$	130		
Operating current (Fast page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ $\overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trAC} = 60 \text{ ns}$	90	mA	1,2,5
				$\text{trAC} = 70 \text{ ns}$	80		
				$\text{trAC} = 80 \text{ ns}$	70		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trAC} = 60 \text{ ns}$	150	mA	1,2
				$\text{trAC} = 70 \text{ ns}$	140		
				$\text{trAC} = 80 \text{ ns}$	130		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (1 024 cycles / 128 ms, only for μ PD42S18160L)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : 1 024 cycles/128 ms $\overline{\text{RAS}}, \overline{\text{CAS}} : V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby : $\overline{\text{RAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : Don't care $\overline{\text{WE}}, \overline{\text{OE}} : V_{\text{IH}}$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trAS} \leq 1 \mu\text{s}$	180	μA	1,2
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for μ PD42S18160L)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}} : V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $\text{I}_\text{O} = 0 \text{ mA}$		150	μA	2
Input leakage current		I _{I(L)}	$V_{\text{I}} = 0 \text{ to } 3.6 \text{ V}$ all other pins not under test = 0 V	-5	+5	μA	
Output leakage current		I _{O(L)}	Output is disabled (Hi-Z) $V_{\text{O}} = 0 \text{ to } 3.6 \text{ V}$	-5	+5	μA	
High level output voltage		V _{OH}	$\text{I}_\text{O} = -2.0 \text{ mA}$	2.4		V	
Low level output voltage		V _{OL}	$\text{I}_\text{O} = 2.0 \text{ mA}$		0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (trc and tpc).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

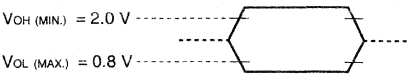
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		tRC	110	–	130	–	150	–	ns	
RAS Precharge Time		tRP	40	–	50	–	60	–	ns	
CAS Precharge Time		tCPN	10	–	10	–	10	–	ns	
RAS Pulse Width		tRAS	60	10 000	70	10 000	80	10 000	ns	
CAS Pulse Width		tCAS	15	10 000	20	10 000	20	10 000	ns	
RAS Hold Time		tRSH	15	–	18	–	20	–	ns	
CAS Hold Time		tCSH	60	–	70	–	80	–	ns	
RAS to CAS Delay Time		tRCD	20	45	20	50	25	60	ns	1
RAS to Column Address Delay Time		tRAD	15	30	15	35	17	40	ns	1
CAS to RAS Precharge Time		tCRP	5	–	5	–	5	–	ns	2
Row Address Setup Time		tASR	0	–	0	–	0	–	ns	
Row Address Hold Time		tRAH	10	–	10	–	12	–	ns	
Column Address Setup Time		tASC	0	–	0	–	0	–	ns	
Column Address Hold Time		tCAH	15	–	15	–	15	–	ns	
OE Lead Time Referenced to RAS		tOES	0	–	0	–	0	–	ns	
CAS to Data Setup Time		tCLZ	0	–	0	–	0	–	ns	
OE to Data Setup Time		tOLZ	0	–	0	–	0	–	ns	
OE to Data Delay Time		tOED	13	–	15	–	15	–	ns	
Masked Byte Write Hold Time Referenced to RAS		tMRH	0	–	0	–	0	–	ns	
Transition Time (Rise and Fall)		tT	3	50	3	50	3	50	ns	
Refresh Time	μPD42S16160L, 42S18160L	tREF	–	128	–	128	–	128	ms	3
	μPD4216160L		–	64	–	64				
	μPD4218160L		–	16	–	16				

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD(MAX.) and trCD(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD(MAX.)}$ and $\text{trCD} \geq \text{trCD(MAX.)}$ will not cause any operation problems.

2. tCRP(MIN.) requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
3. This specification is applied only to the μ PD42S16160L, 42S18160L.

Read Cycle

Parameter	Symbol	$\text{trAC} = 60 \text{ ns}$		$\text{trAC} = 70 \text{ ns}$		$\text{trAC} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	trAC	–	60	–	70	–	80	ns	1
Access Time from $\overline{\text{CAS}}$	tCAC	–	15	–	20	–	20	ns	1
Access Time from Column Address	tAA	–	30	–	35	–	40	ns	1
Access Time from $\overline{\text{OE}}$	tOEA	–	15	–	20	–	20	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	trAL	30	–	35	–	40	–	ns	
Read Command Setup Time	trCS	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	trRH	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	trCH	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	0	15	ns	3
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	tOFF	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD(MAX.) and trCD(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD(MAX.)}$ and $\text{trCD} \geq \text{trCD(MAX.)}$ will not cause any operation problems.

2. Either trCH(MIN.) or trRH(MIN.) should be met in read cycles.
3. tOFF(MAX.) and tOEZ(MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{WAC} = 60 ns		t _{WAC} = 70 ns		t _{WAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
WE Hold Time Referenced to $\overline{\text{CAS}}$	twch	10	–	10	–	15	–	ns	1
WE Pulse Width	twp	10	–	10	–	15	–	ns	1
WE Lead Time Referenced to $\overline{\text{RAS}}$	trwl	20	–	20	–	20	–	ns	
WE Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	15	–	15	–	15	–	ns	
WE Setup Time	twcs	0	–	0	–	0	–	ns	2
OE Hold Time	toeh	0	–	0	–	0	–	ns	
Data-in Setup Time	tds	0	–	0	–	0	–	ns	3
Data-in Hold Time	tdh	10	–	15	–	15	–	ns	3

- Notes**
1. $t_{wp}(\text{MIN.})$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{wch}(\text{MIN.})$ should be met.
 2. If $t_{wcs} \geq t_{wcs}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. $t_{ps}(\text{MIN.})$ and $t_{dh}(\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the WE falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{WAC} = 60 ns		t _{WAC} = 70 ns		t _{WAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	160	–	180	–	200	–	ns	
RAS to WE Delay Time	trwd	83	–	95	–	105	–	ns	1
CAS to WE Delay Time	tcwd	38	–	40	–	45	–	ns	1
Column Address to WE Delay Time	tawd	53	–	60	–	65	–	ns	1

- Note 1.** If $t_{wcs} \geq t_{wcs}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{awd} \geq t_{awd}(\text{MIN.})$, $t_{cwd} \geq t_{cwd}(\text{MIN.})$, $t_{awd} \geq t_{awd}(\text{MIN.})$ and $t_{cpwd} \geq t_{cpwd}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	40	–	45	–	50	–	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	–	35	–	40	–	45	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RASP}	60	125 000	70	125 000	80	125 000	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35	–	40	–	45	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	85	–	90	–	105	–	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	60	–	65	–	70	–	ns	1

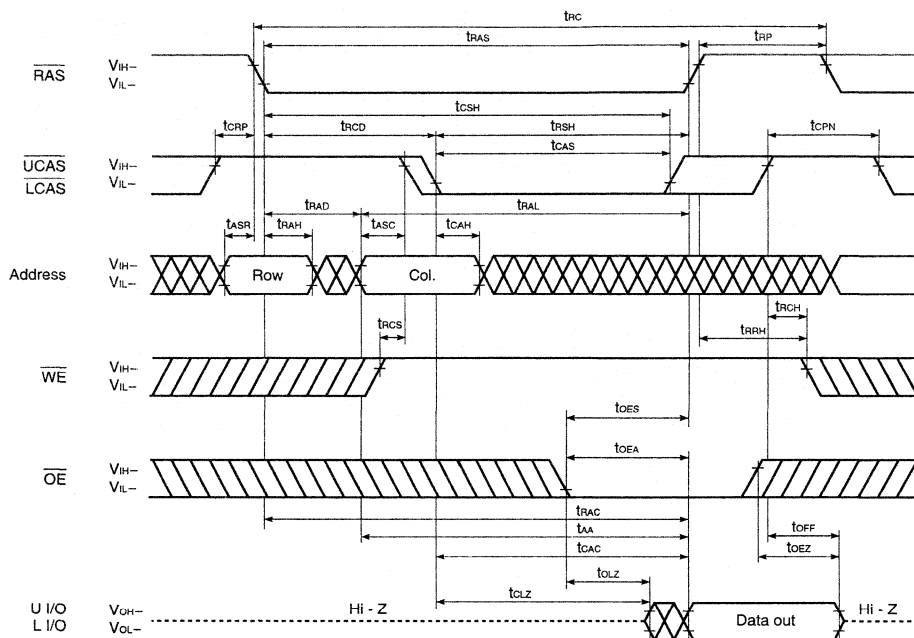
Note 1. If $\text{t}_{\text{WCS}} \geq \text{t}_{\text{WCS}}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $\text{t}_{\text{RWd}} \geq \text{t}_{\text{RWd}}(\text{MIN.})$, $\text{t}_{\text{CWd}} \geq \text{t}_{\text{CWd}}(\text{MIN.})$, $\text{t}_{\text{AWd}} \geq \text{t}_{\text{AWd}}(\text{MIN.})$ and $\text{t}_{\text{CPWD}} \geq \text{t}_{\text{CPWD}}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ Setup Time	t _{CSR}	5	–	5	–	5	–	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RASS}	100	–	100	–	100	–	μ s	1
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RPS}	110	–	130	–	150	–	ns	1
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ Hold Time (Hidden Refresh Cycle)	t _{WHR}	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μ PD42S16160L, 42S18160L.

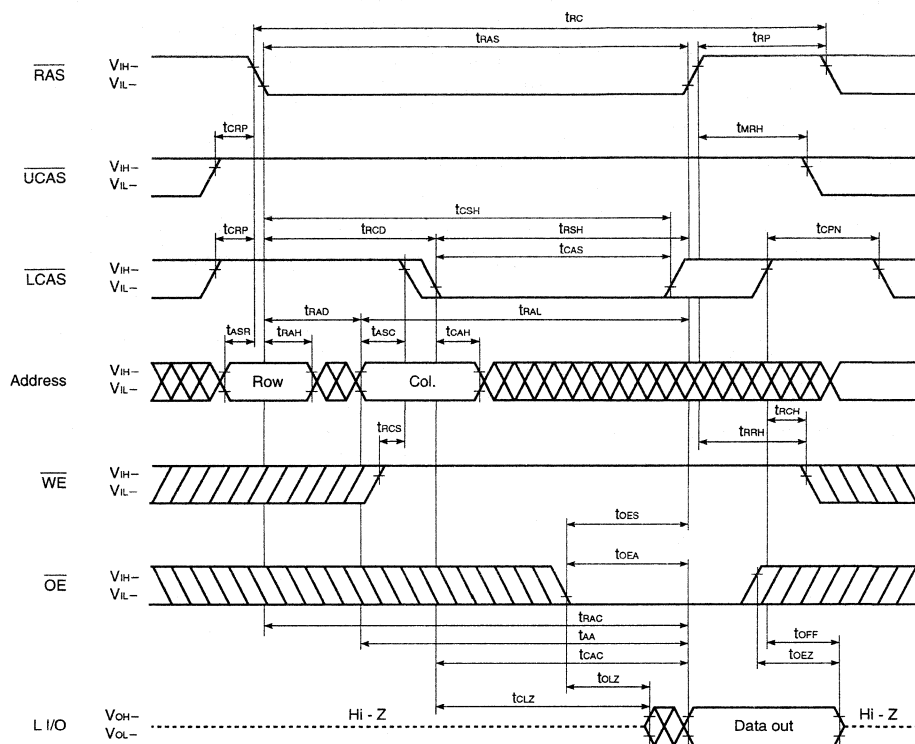
Read Cycle



[illegible]

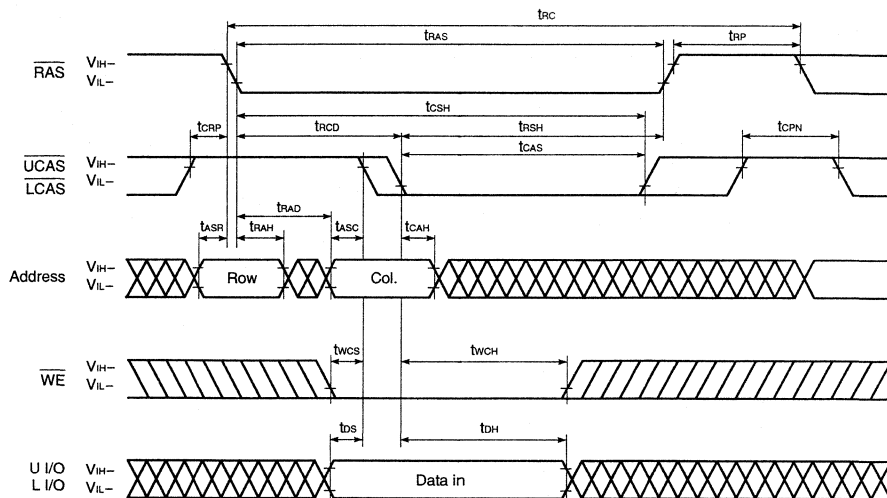
Remark L I/O : Hi-Z

Lower Byte Read Cycle



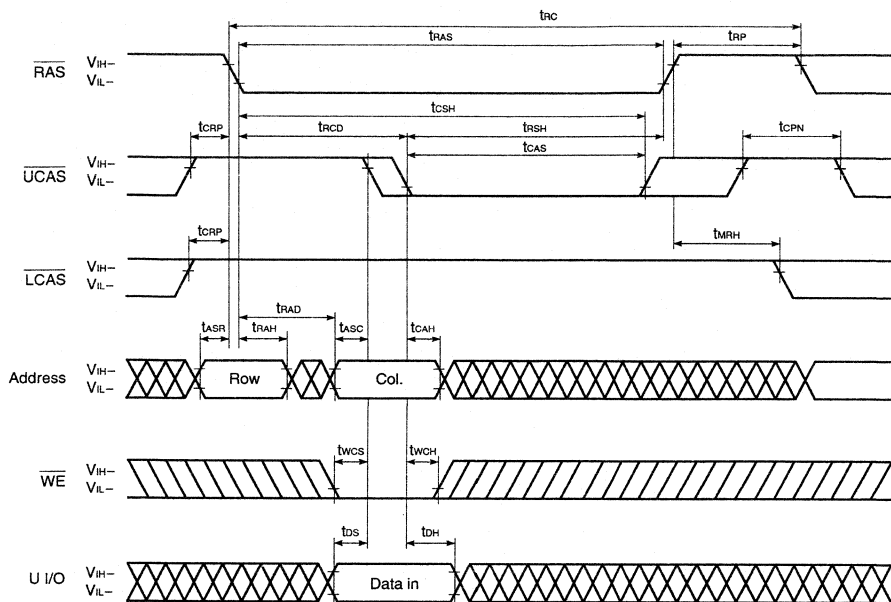
Remark U I/O : Hi-Z

Early Write Cycle



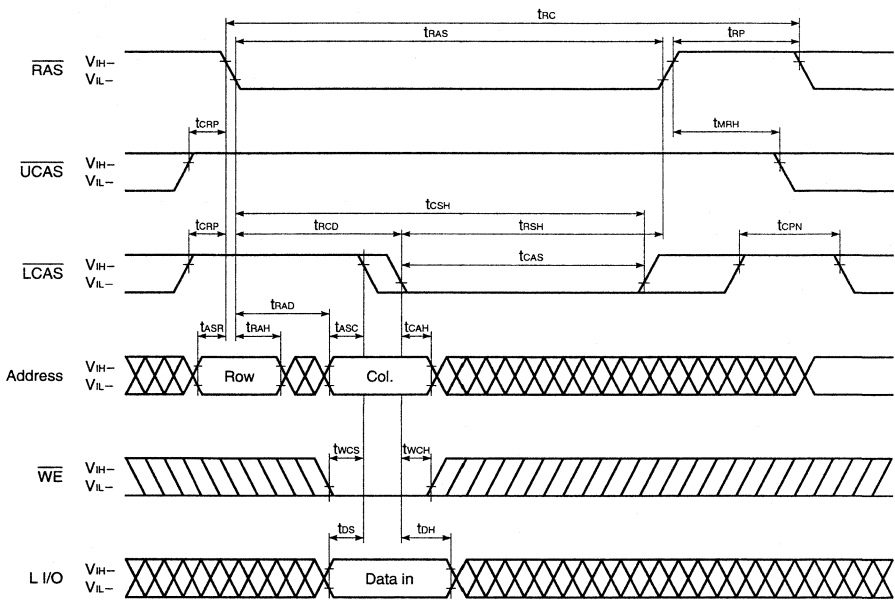
Remark $\overline{\text{OE}}$: Don't care

Upper Byte Early Write Cycle



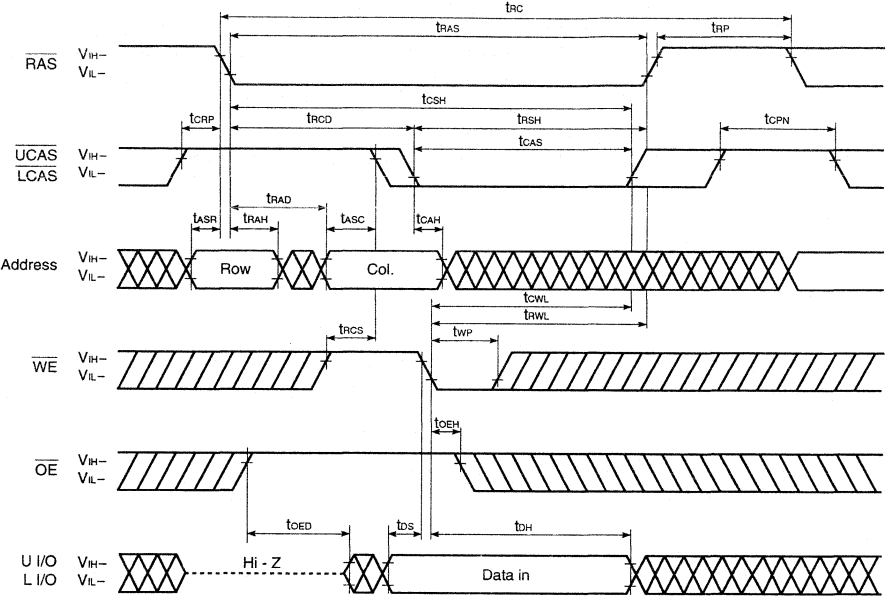
Remark $\overline{\text{OE}}$, L I/O : Don't care

Lower Byte Early Write Cycle

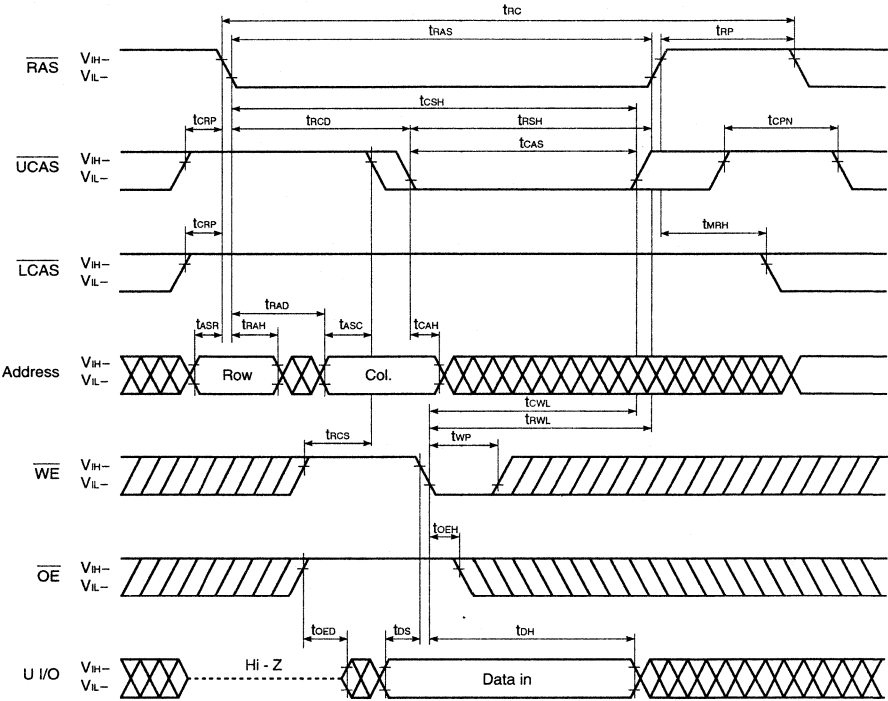


Remark $\overline{\text{OE}}$, U I/O : Don't care

Late Write Cycle

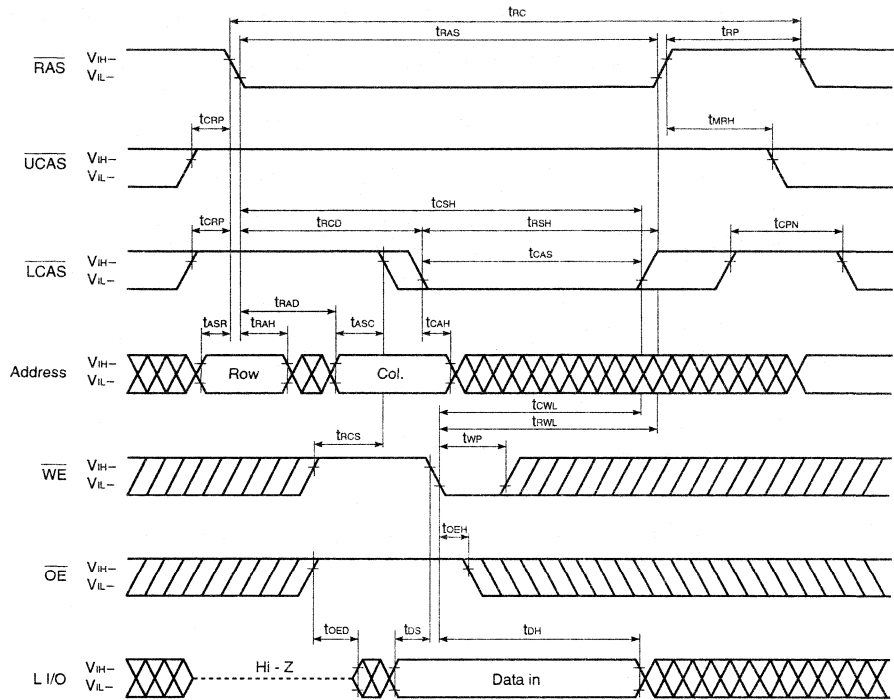


Upper Byte Late Write Cycle



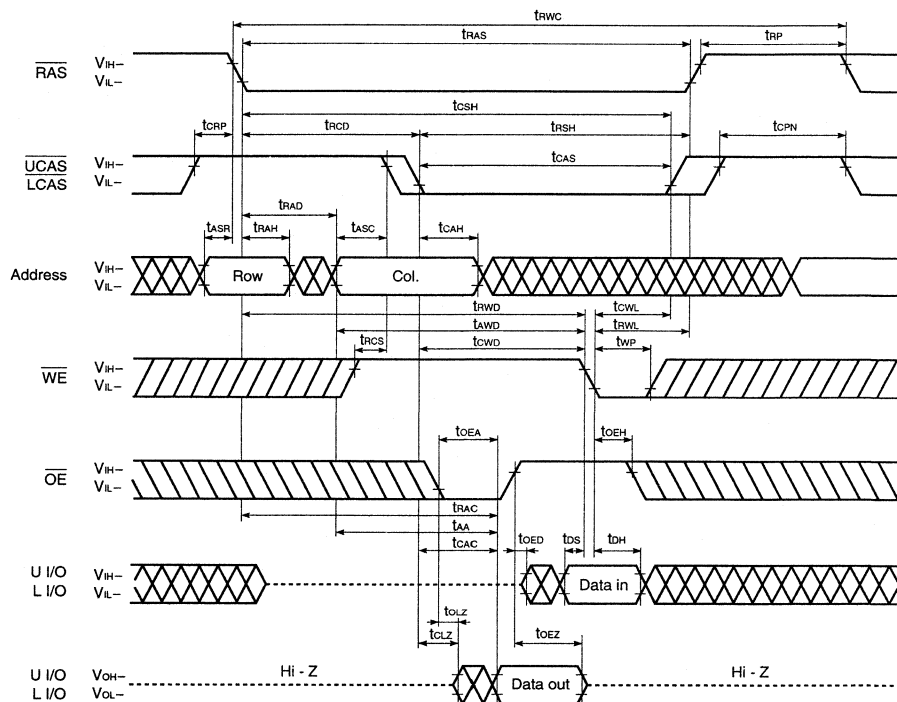
Remark L I/O : Don't care

Lower Byte Late Write Cycle

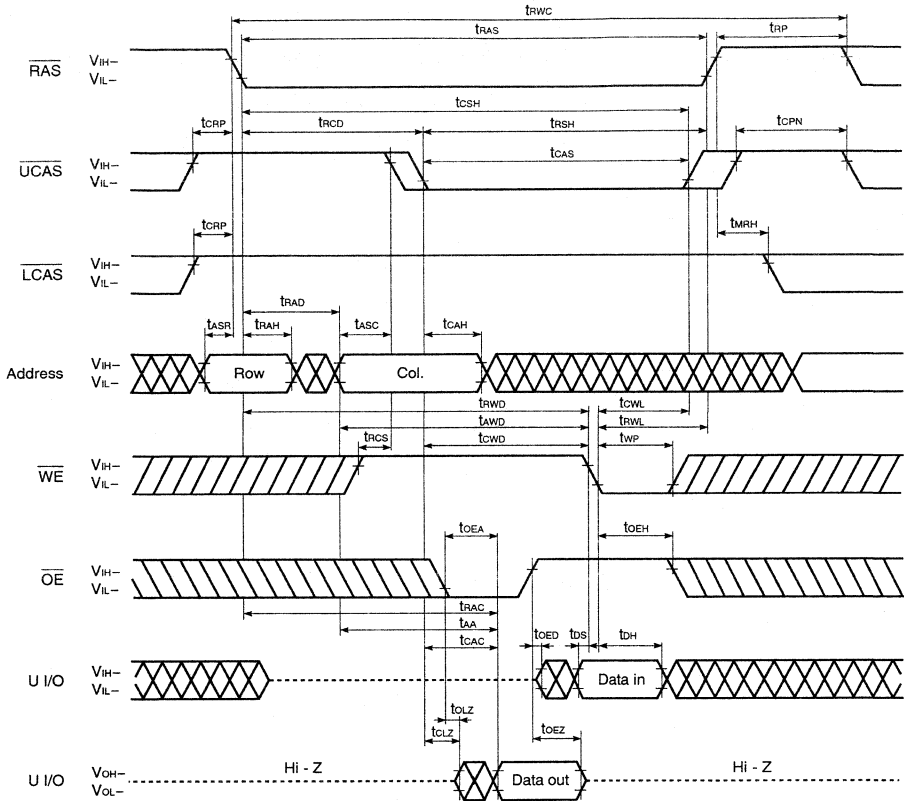


Remark U I/O : Don't care

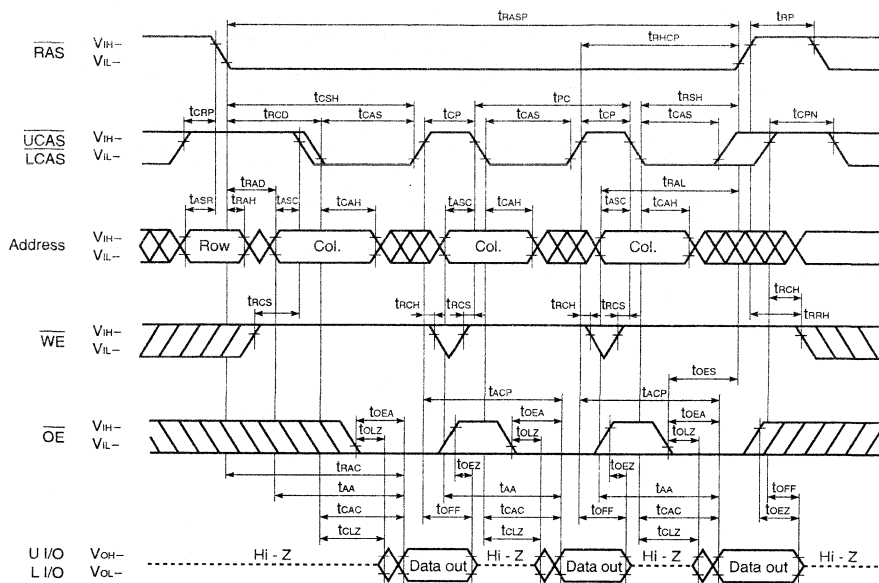
Read Modify Write Cycle



Upper Byte Read Modify Write Cycle



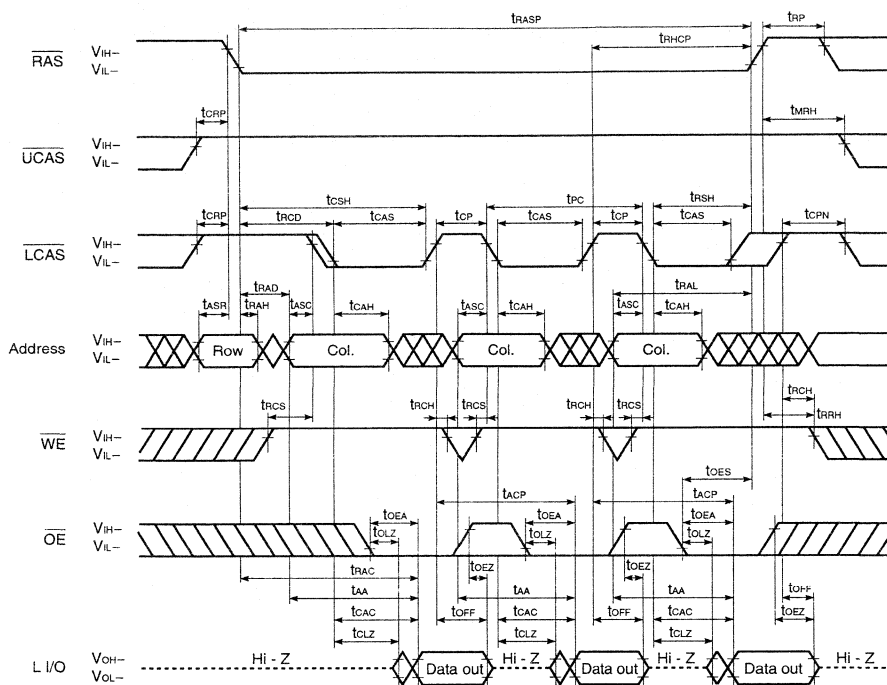
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.



[illegible]

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

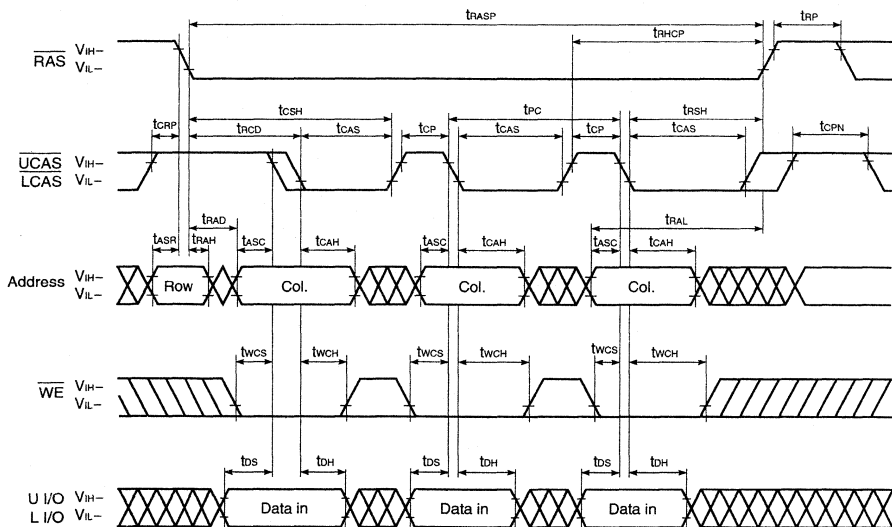
Fast Page Mode Lower Byte Read Cycle



Remark U I/O : Hi-Z

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

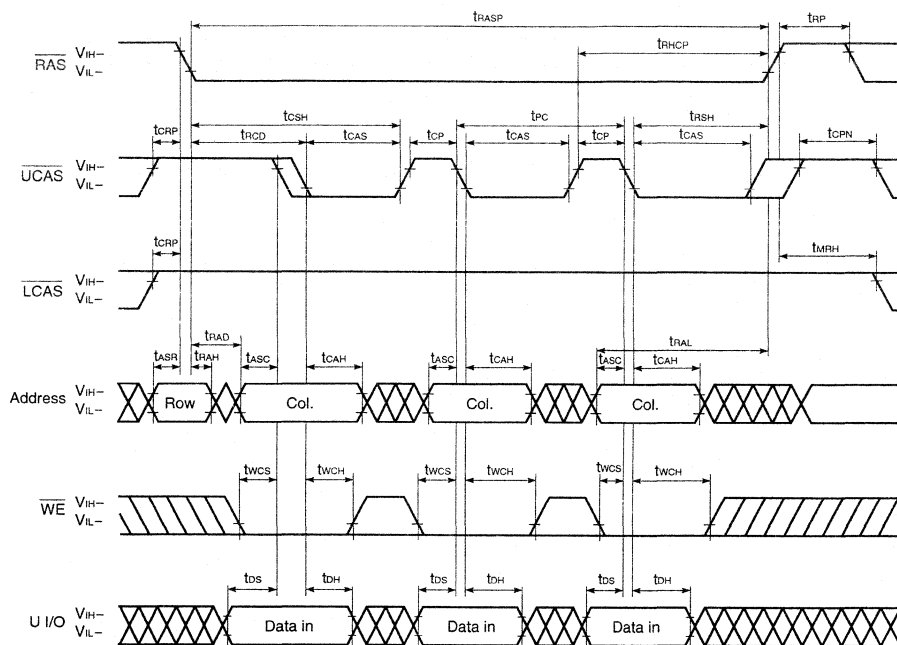
Fast Page Mode Early Write Cycle



Remark $\overline{\text{OE}}$: Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

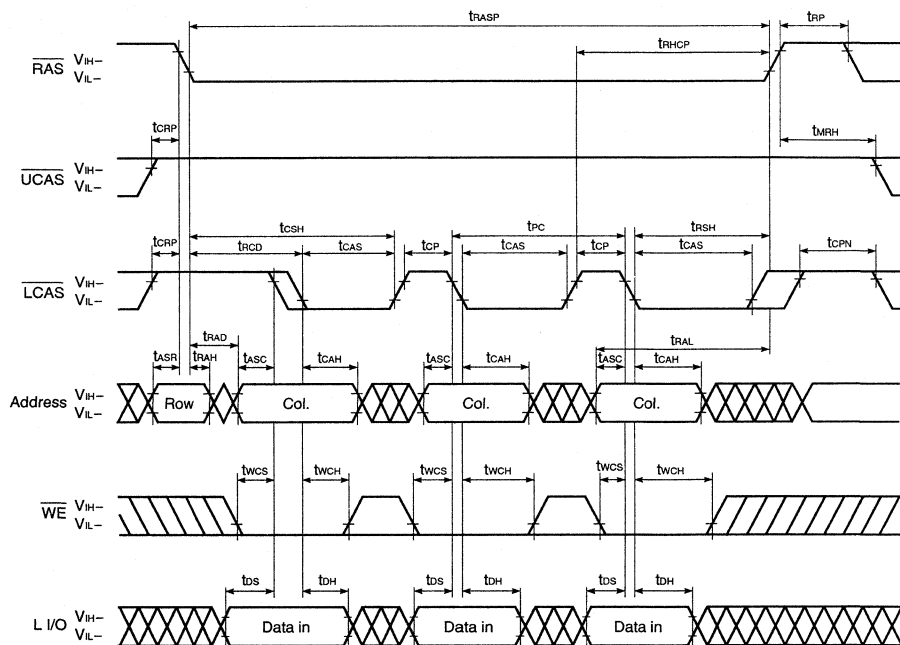
Fast Page Mode Upper Byte Early Write Cycle



Remark $\overline{\text{OE}}$, L I/O : Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Lower Byte Early Write Cycle



Remark $\overline{OE}$, U I/O : Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

The diagram illustrates the timing relationships between several control and data signals during memory access operations. The signals shown are:

- RAS**: Row Address Strobe, active low.
- UCAS**: User Chip Address Strobe, active low.
- LCAS**: Local Chip Address Strobe, active low.
- Address**: Bus address signal, alternating between Row and Column addresses.
- WE**: Write Enable, active low.
- OE**: Output Enable, active low.
- L I/O**: Local Input/Output bus signal.
- U I/O**: User Input/Output bus signal.

Key timing parameters labeled include:

- tRASP**, **tRHCP**, **tRP**: RAS-related delays.
- tCRP**, **tCSD**, **tCAS**, **tCP**, **tPC**, **tRSH**, **tCPN**: UCAS and LCAS setup and hold times.
- tMRH**: Memory Refresh Hold time.
- tASR**, **tRAH**, **tASC**, **tCAH**: Address Setup and Hold times.
- tTWC**, **tTWS**, **tTWP**: Write Enable timing parameters.
- tTOEH**: Output Enable delay from address strobe.
- tTOED**: Data output delay from enable.
- tDS**, **tDH**: Data Setup and Hold times relative to enable.

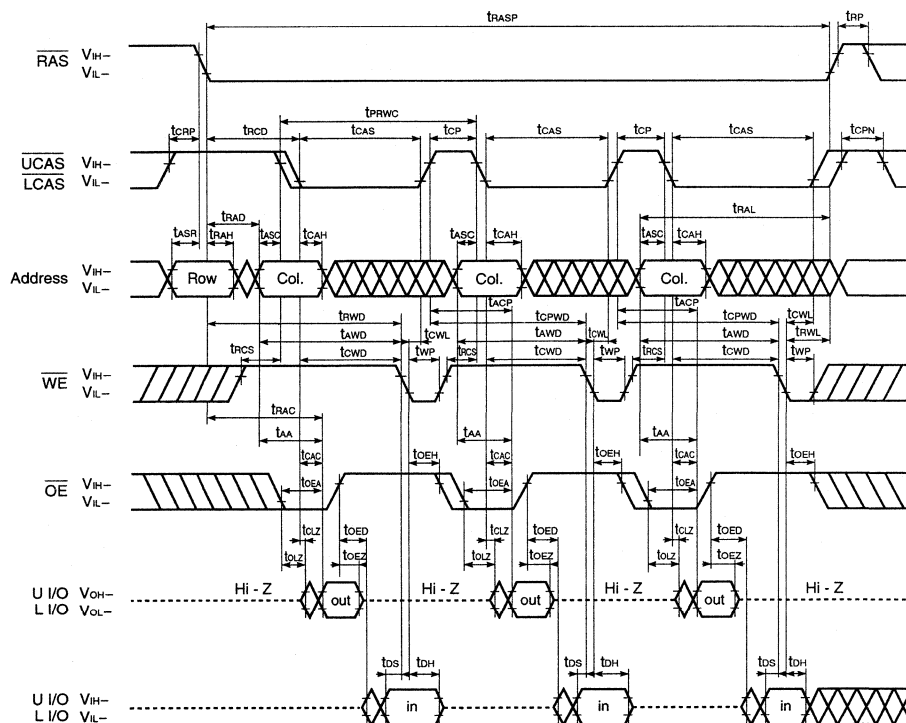
Remark In this cycle, the input data to Lower I/O is ineffective.
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

The timing diagram illustrates the relationship between various signals and their timing parameters. The signals shown are RAS, UCAS, LCAS, Address, WE, OE, L I/O, and U I/O. The timing parameters are defined as follows:

- t_{RASP} : RAS pulse width (high to low)
- t_{RHP} : RAS pulse width (low to high)
- t_{RP} : RAS pulse width (high to low)
- t_{MRH} : Memory refresh time (high to low)
- t_{CRP} : Column refresh pulse width (high to low)
- t_{CSD} : Column refresh delay (high to low)
- t_{CAS} : Column refresh delay (low to high)
- t_{CP} : Column refresh delay (high to low)
- t_{PC} : Column refresh delay (low to high)
- t_{RSH} : Row refresh delay (high to low)
- t_{CPN} : Column refresh delay (high to low)
- t_{ASR} : Address strobe delay (high to low)
- t_{RAH} : Address strobe delay (low to high)
- t_{ASC} : Address strobe delay (high to low)
- t_{CAH} : Address strobe delay (low to high)
- t_{AL} : Address strobe delay (high to low)
- t_{RCS} : Row refresh delay (high to low)
- t_{WPL} : Row refresh delay (low to high)
- t_{RCS} : Row refresh delay (high to low)
- t_{WPL} : Row refresh delay (low to high)
- t_{RCS} : Row refresh delay (high to low)
- t_{WPL} : Row refresh delay (low to high)
- t_{OEH} : Output enable delay (high to low)
- t_{OEH} : Output enable delay (low to high)
- t_{OEH} : Output enable delay (high to low)
- t_{OED} : Output enable delay (high to low)
- t_{DS} : Data strobe delay (high to low)
- t_{DH} : Data strobe delay (low to high)
- t_{OED} : Output enable delay (high to low)
- t_{DS} : Data strobe delay (high to low)
- t_{DH} : Data strobe delay (low to high)
- t_{OED} : Output enable delay (high to low)
- t_{DS} : Data strobe delay (high to low)
- t_{DH} : Data strobe delay (low to high)
- t_{OED} : Output enable delay (high to low)
- t_{DS} : Data strobe delay (high to low)
- t_{DH} : Data strobe delay (low to high)

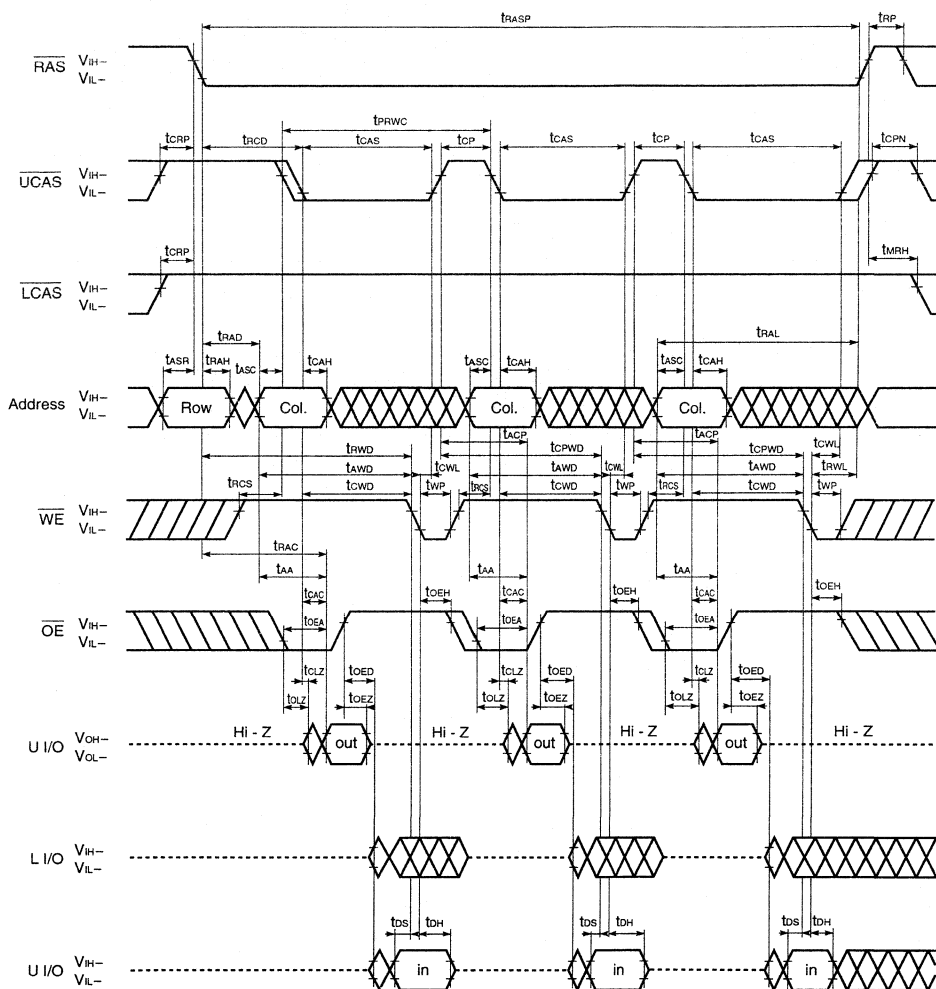
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Read Modify Write Cycle

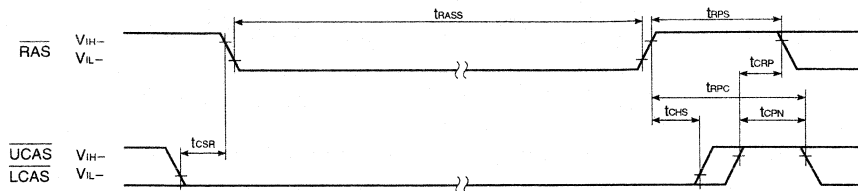


Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Upper Byte Read Modify Write Cycle



Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle (Only for the μ PD42S16160L, 42S18160L)

Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O : Hi - Z

Cautions on Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh can be used independently when used in combination with distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh; However, when used in combination with burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh or with burst long $\overline{\text{RAS}}$ only refresh, the following cautions must be observed.

(1) Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Burst $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Long Refresh

When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh are used in combination, please perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh as follows just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

μ PD42S16160L : 4 096 times within a 64 ms interval

μ PD42S18160L : 1 024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Burst Long $\overline{\text{RAS}}$ Only Refresh

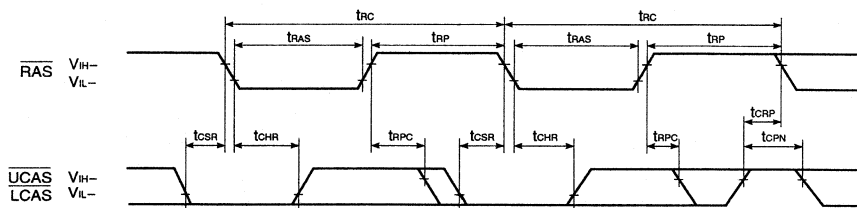
When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{RAS}}$ only refresh are used in combination, please perform $\overline{\text{RAS}}$ only refresh as follows just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

μ PD42S16160L : 4 096 times within a 64 ms interval

μ PD42S18160L : 1 024 times within a 16 ms interval

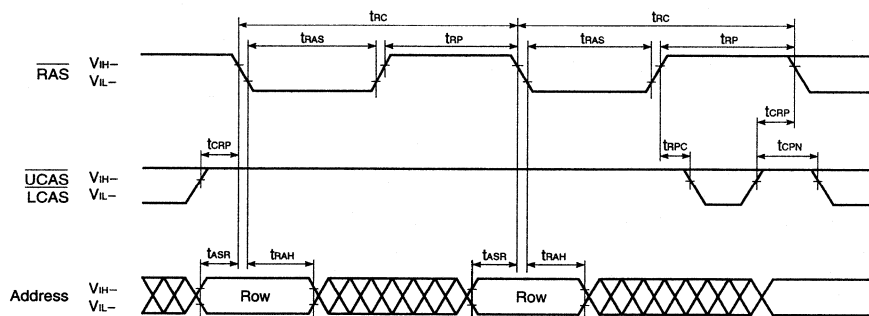
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



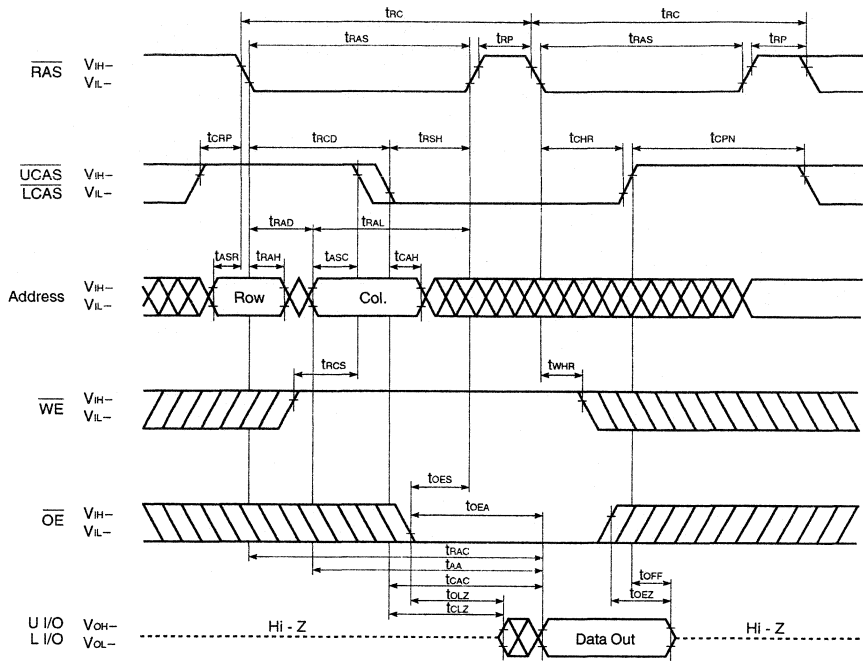
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

RAS Only Refresh Cycle

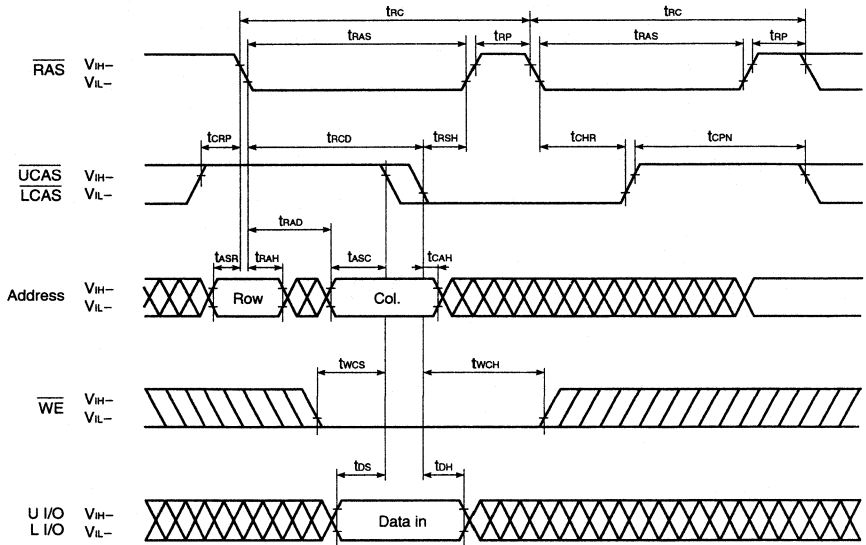


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

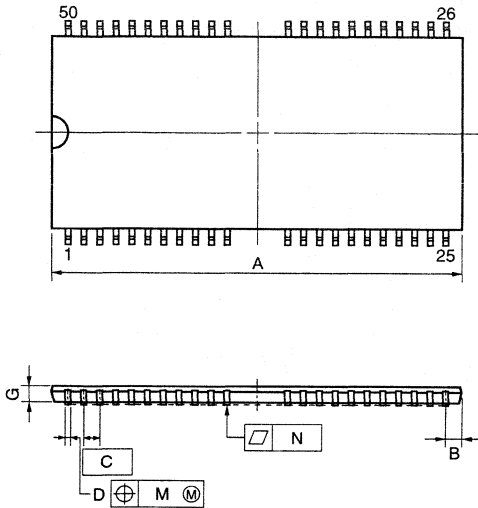


Remark $\overline{OE}$: Don't care

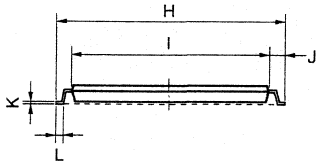
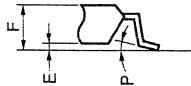
Package Drawings



50 PIN PLASTIC TSOP (II) (400 mil)



detail of lead end

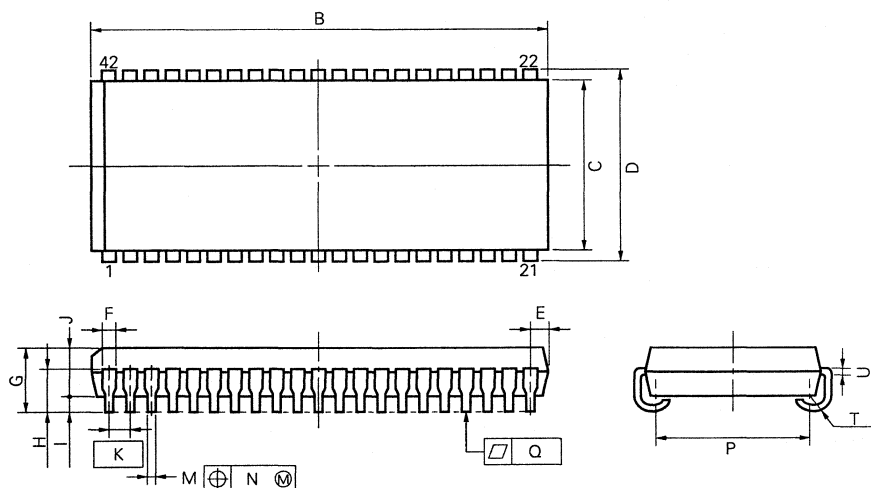


NOTE
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 ^{+0.08} _{-0.07}	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P42LE-400A

ITEM	MILLIMETERS	INCHES
B	27.56 ^{+0.2} _{-0.35}	1.085 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

Recommended Soldering Conditions



The following conditions (see tables below and next page) must be met when soldering μPD42S16160L, 4216160L, 42S18160L, 4218160L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16160LG5, 4216160LG5, 42S18160LG5, 4218160LG5 : 50-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-107-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μ PD42S16160LLE, 4216160LLE, 42S18160LLE, 4218160LLE : 42-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μ PD42S16165L, 4216165L**3.3 V OPERATION 16 M-BIT DYNAMIC RAM****1 M-WORD BY 16-BIT, HYPER PAGE MODE, BYTE READ/WRITE MODE****Description**

The μ PD42S16165L, 4216165L are 1 048 576 words by 16 bits dynamic CMOS RAMs with optional hyper page mode.

Hyper page mode is a kind of page mode and is useful for the read operation.

The μ PD42S16165L, 4216165L are packed in 50-pin plastic TSOP(II) and 42-pin plastic SOJ.

Features

- Hyper page mode
- Single +3.3 V $\pm$ 0.3 V power supply
- 1 048 576 words by 16 bits organization

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μ PD42S16165L-A60, 4216165L-A60	60 ns	104 ns	25 ns
μ PD42S16165L-A70, 4216165L-A70	70 ns	124 ns	30 ns

- μ PD42S16165L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh
μ PD42S16165L	4 096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4216165L	4 096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh

The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Refresh	
μ PD42S16165LG5-A60-7JF	60 ns	50-pin Plastic TSOP(III) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh	
μ PD42S16165LG5-A70-7JF	70 ns			
μPD42S16165LG5-A60-7KF	60 ns	50-pin Plastic TSOP (II) (400 mil) Reverse bent		
μPD42S16165LG5-A70-7KF	70 ns			
μ PD42S16165LLE-A60	60 ns	42-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh	
μ PD42S16165LLE-A70	70 ns			
μ PD4216165LG5-A60-7JF	60 ns	50-pin Plastic TSOP (II) (400 mil)		$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4216165LG5-A70-7JF	70 ns			
μPD4216165LG5-A60-7KF	60 ns	50-pin Plastic TSOP (II) (400 mil) Reverse bent		
μPD4216165LG5-A70-7KF	70 ns			
μ PD4216165LLE-A60	60 ns	42-pin Plastic SOJ (400 mil)		
μ PD4216165LLE-A70	70 ns			

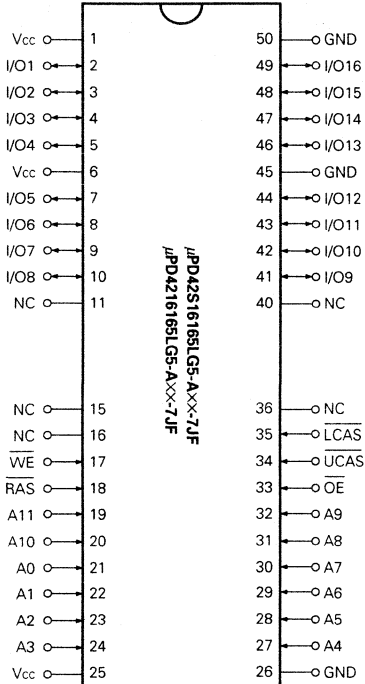
Quality Grade

Standard

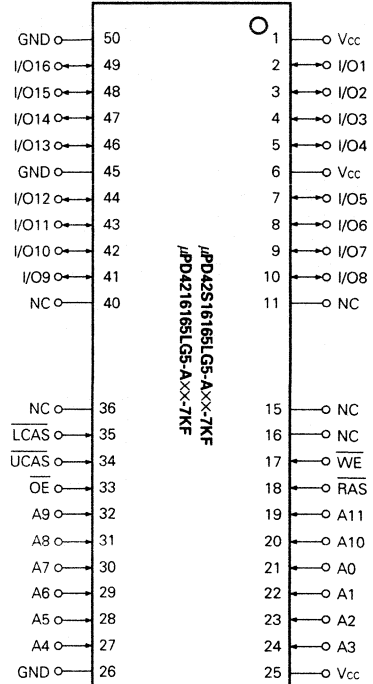
Please refer to “Quality grade on NEC Semiconductor Devices” (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II) (400 mil)

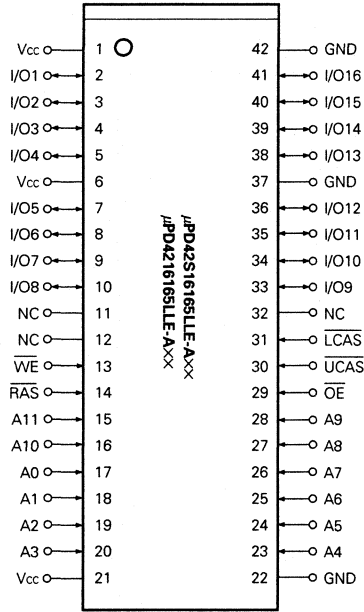


Reverse bent



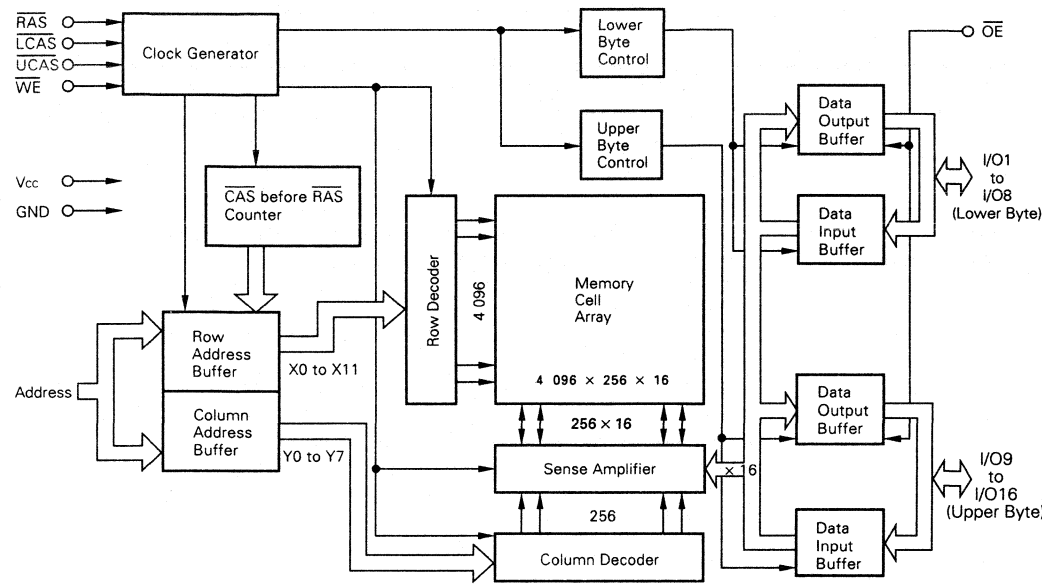
- A0 to A11 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
- LCAS : Column Address Strobe (lower)
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

42-pin Plastic SOJ (400 mil)



- A0 to A11 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{UCAS}}$: Column Address Strobe (upper)
- $\overline{\text{LCAS}}$: Column Address Strobe (lower)
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Input/Output Pin Functions

The μ PD42S16165L, 4216165L have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ **Note**, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11 and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)		Address bus. Input total 20-bit of address signal, upper 12-bit and lower 8-bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t _{ASR} , t _{ASC}) and hold time (t _{RAH} , t _{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

In the hyper page mode, the output data is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

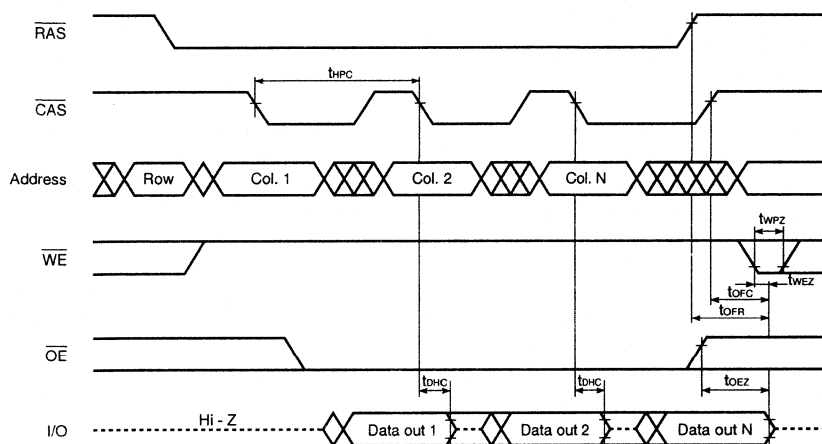
2. The $\overline{\text{CAS}}$ cycle time in the hyper page mode is shorter than that in the fast page mode.

In the hyper page mode, due to the data extend function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{\text{CAS}}$ cycle time in the hyper page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{\text{RAS}}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

Hyper Page Mode Read Cycle



To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.

- (1) $\overline{\text{RAS}}$, $\overline{\text{CAS}}$: inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

- (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$: active, $\overline{\text{OE}}$: active ... t_{WEZ} , t_{WPZ} are effective.

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: inactive ... t_{OEZ} is effective.

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-0.5 to +4.6	V
Supply Voltage	V_{CC}		-0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low Level Input Voltage	V_{IL}		-0.3		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

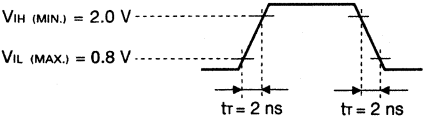
Parameter		Symbol	Test Condition		MIN.	TYP.	MAX.	Unit	Notes	
Operating current		I _{CC1}	RAS, CAS Cycling trc = trc(MIN.) I _O = 0 mA	trac = 60 ns			90	mA	1,2,3	
				trac = 70 ns			80			
Standby current	μPD42S16165L	I _{CC2}	RAS, CAS ≥ V _{IH} (MIN.), I _O = 0 mA				0.5	mA		
			RAS, CAS ≥ V _{CC} - 0.2 V, I _O = 0 mA				0.15			
	μPD4216165L		RAS, CAS ≥ V _{IH} (MIN.), I _O = 0 mA			2				
	RAS, CAS ≥ V _{CC} - 0.2 V, I _O = 0 mA				0.5					
RAS only refresh current		I _{CC3}	RAS Cycling, CAS ≥ V _{IH} (MIN.) trc = trc (MIN.), I _O = 0 mA	trac = 60 ns			90	mA	1,2,3,4	
				trac = 70 ns			80			
Operating current (Hyper page mode)		I _{CC4}	RAS ≤ V _{IL} (MAX.), CAS Cycling thpc = thpc (MIN.), I _O = 0 mA	trac = 60 ns			110	mA	1,2,5	
				trac = 70 ns			100			
CAS before RAS refresh current		I _{CC5}	RAS Cycling trc = trc (MIN.) I _O = 0 mA	trac = 60 ns			90	mA	1, 2	
				trac = 70 ns			80			
CAS before RAS long refresh current (4 096 Cycles / 128 ms, only for the μPD42S16165L)		I _{CC6}	CAS before RAS refresh : 4 096 Cycles / 128 ms RAS, CAS : V _{CC} -0.2 V ≤ V _{IH} ≤ V _{IH} (MAX.) 0 V ≤ V _{IL} ≤ 0.2 V Standby : RAS ≥ V _{CC} -0.2 V Address : V _{IH} or V _{IL} WE, OE : V _{IH} I _O = 0 mA		tras ≤ 1 μs			220	μA	1, 2
Self refresh current (CAS before RAS self refresh, only for the μPD42S16165L)		I _{CC7}	RAS, CAS : V _{CC} -0.2 V ≤ V _{IH} ≤ V _{IH} (MAX.) 0 V ≤ V _{IL} ≤ 0.2 V I _O = 0 mA					150	μA	2
Input leakage current		I _I (L)	V _I = 0 to 3.6 V All other pins not under test = 0 V		-5			+5	μA	
Output leakage current		I _O (L)	V _O = 0 to 3.6 V Output is disabled (Hi-Z)		-5			+5	μA	
High level output voltage		V _{OH}	I _O = -2.0 mA		2.4				V	
Low level output voltage		V _{OL}	I _O = +2.0 mA					0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (trc and thpc).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

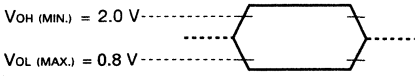
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		t _{RC}	104	–	124	–	ns	
RAS Precharge Time		t _{RP}	40	–	50	–	ns	
CAS Precharge Time		t _{CPN}	10	–	10	–	ns	
RAS Pulse Width		t _{RAS}	60	10 000	70	10 000	ns	
CAS Pulse Width		t _{CAS}	10	10 000	12	10 000	ns	
RAS Hold Time		t _{RSH}	10	–	12	–	ns	
CAS Hold Time		t _{CSH}	40	–	50	–	ns	
RAS to CAS Delay Time		t _{RCD}	14	45	14	52	ns	1
RAS to Column Address Delay Time		t _{RAD}	12	30	12	35	ns	1
CAS to RAS Precharge Time		t _{CRP}	5	–	5	–	ns	2
Row Address Setup Time		t _{ASR}	0	–	0	–	ns	
Row Address Hold Time		t _{RAH}	10	–	10	–	ns	
Column Address Setup Time		t _{ASC}	0	–	0	–	ns	
Column Address Hold Time		t _{CAH}	10	–	12	–	ns	
OE Lead Time Referenced to RAS		t _{OES}	0	–	0	–	ns	
CAS to Data Setup Time		t _{CLZ}	0	–	0	–	ns	
OE to Data Setup Time		t _{OLZ}	0	–	0	–	ns	
OE to Data Delay Time		t _{OED}	13	–	15	–	ns	
Masked Byte Write Hold Time Referenced to RAS		t _{MRH}	0	–	0	–	ns	
Transition Time (Rise and Fall)		t _T	1	50	1	50	ns	
Refresh Time	μPD42S16165L	t _{REF}	–	128	–	128	ms	3
	μPD4216165L		–	64	–	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD(MAX.) and trCD(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD(MAX.)}$ and $\text{trCD} \geq \text{trCD(MAX.)}$ will not cause any operation problems.

- tCRP(MIN.) requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
- This specification is applied only to the μPD42S16165L.

Read Cycle

Parameter	Symbol	$\text{trAC} = 60 \text{ ns}$		$\text{trAC} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	trAC	–	60	–	70	ns	1
Access Time from $\overline{\text{CAS}}$	tCAC	–	15	–	18	ns	1
Access Time from Column Address	tAA	–	30	–	35	ns	1
Access Time from $\overline{\text{OE}}$	tOEa	–	15	–	18	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	trAL	30	–	35	–	ns	
Read Command Setup Time	trCS	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	trRH	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	trCH	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD(MAX.) and trCD(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD(MAX.)}$ and $\text{trCD} \geq \text{trCD(MAX.)}$ will not cause any operation problems.

- Either trCH(MIN.) or trRH(MIN.) should be met in read cycles.
- tOEZ(MAX.) defines the time when the output achieves the condition of Hi-Z and is not referenced to VOH or VOL .

Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	10	–	10	–	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	10	–	10	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	10	–	12	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	10	–	12	–	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	–	0	–	ns	
Data-in Setup Time	tds	0	–	0	–	ns	3
Data-in Hold Time	tdh	10	–	10	–	ns	3

- Notes**
1. t_{wP(MIN.)} is applied to late write cycles or read modify write cycles. In early write cycles, t_{wCH(MIN.)} should be met.
 2. If t_{wCS} $\geq$ t_{wCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{ds(MIN.)} and t_{dh(MIN.)} are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	133	–	157	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	77	–	89	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	32	–	37	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	47	–	54	–	ns	1

- Note 1.** If t_{wCS} $\geq$ t_{wCS(MIN.)} the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{trwd} $\geq$ t_{trwd(MIN.)}, t_{tcwd} $\geq$ t_{tcwd(MIN.)}, t_{tawd} $\geq$ t_{tawd(MIN.)}, and t_{cpwd} $\geq$ t_{cpwd(MIN.)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{HPC}	25	–	30	–	ns	
RAS Pulse Width	t _{RASP}	60	125 000	70	125 000	ns	
CAS Pulse Width	t _{HCAS}	10	10 000	12	10 000	ns	
CAS Precharge Time	t _{CP}	10	–	10	–	ns	
Access Time from CAS Precharge	t _{ACP}	–	35	–	40	ns	
CAS Precharge to WE Delay Time	t _{CPWD}	52	–	59	–	ns	1
RAS Hold Time from CAS Precharge	t _{RHCP}	35	–	40	–	ns	
Read Modify Write Cycle Time	t _{HPRWC}	66	–	75	–	ns	
Data Output Hold Time	t _{DHC}	5	–	5	–	ns	
Output Buffer Turn-off Delay from WE	t _{WEZ}	0	13	0	15	ns	2,3
WE Pulse Width	t _{WPZ}	10	–	10	–	ns	3
Output Buffer Turn-off Delay from RAS	t _{OFR}	0	13	0	15	ns	2,3
Output Buffer Turn-off Delay from CAS	t _{OFC}	0	13	0	15	ns	2,3

Notes 1. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWd} \geq t_{RWd(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$, and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) $\overline{RAS}$, $\overline{CAS}$: Inactive (at the end of read cycle)

$\overline{WE}$: inactive, $\overline{OE}$: active

t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)

$\overline{WE}$: active, $\overline{OE}$: active ... t_{WEZ} , t_{WPZ} are effective.

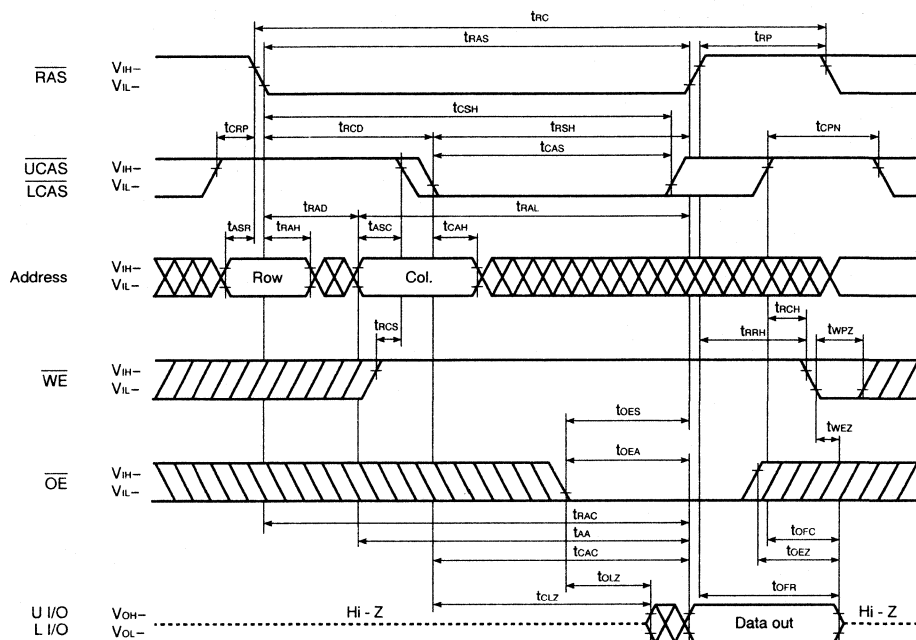
$\overline{WE}$: inactive, $\overline{OE}$: inactive ... t_{WEZ} is effective.

Refresh Cycle

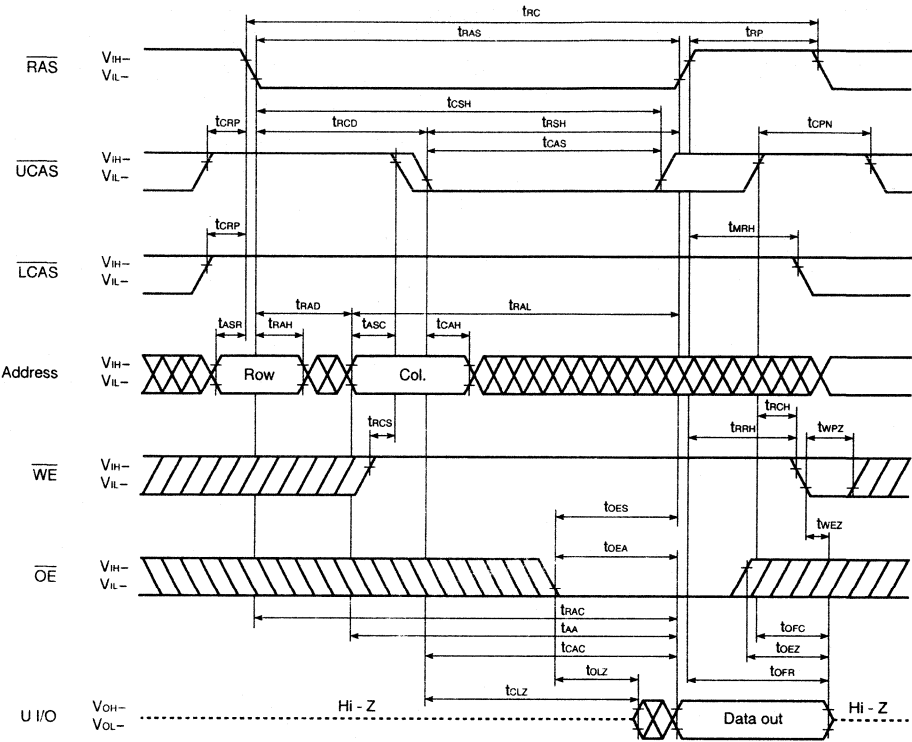
Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	–	5	–	ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10	–	10	–	ns	
RAS Precharge CAS Hold Time	t _{RPC}	5	–	5	–	ns	
RAS Pulse Width (CAS before RAS Self Refresh)	t _{RASS}	100	–	100	–	μ s	1
RAS Precharge Time (CAS before RAS Self Refresh)	t _{RPS}	110	–	130	–	ns	1
CAS Hold Time (CAS before RAS Self Refresh)	t _{CHS}	–50	–	–50	–	ns	1
WE Hold Time (Hidden Refresh Cycle)	t _{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μ PD42S16165L.

Read Cycle

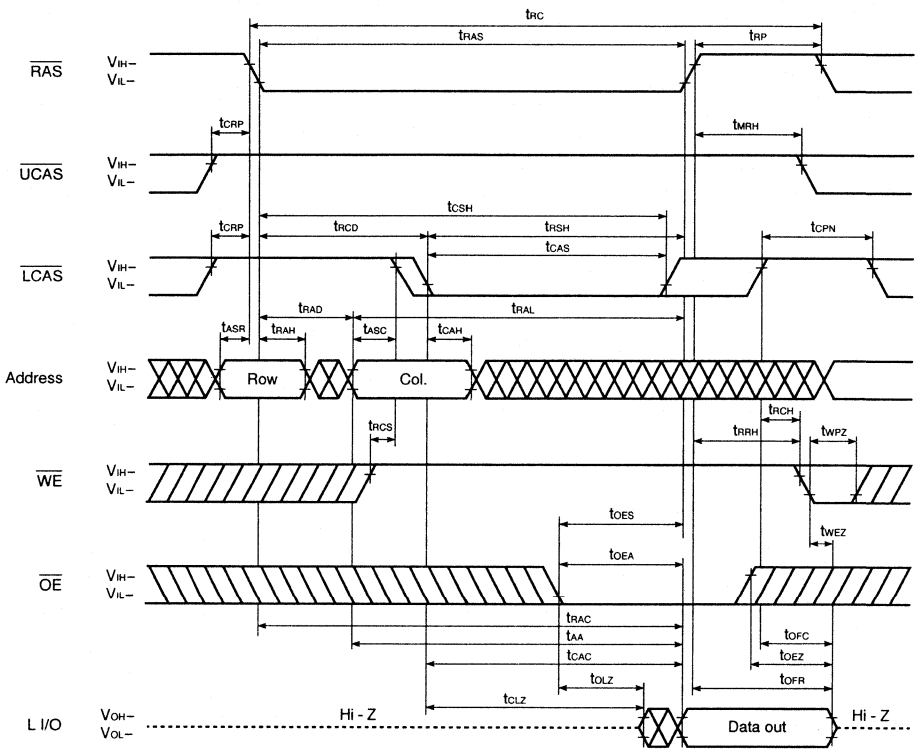


Upper Byte Read Cycle



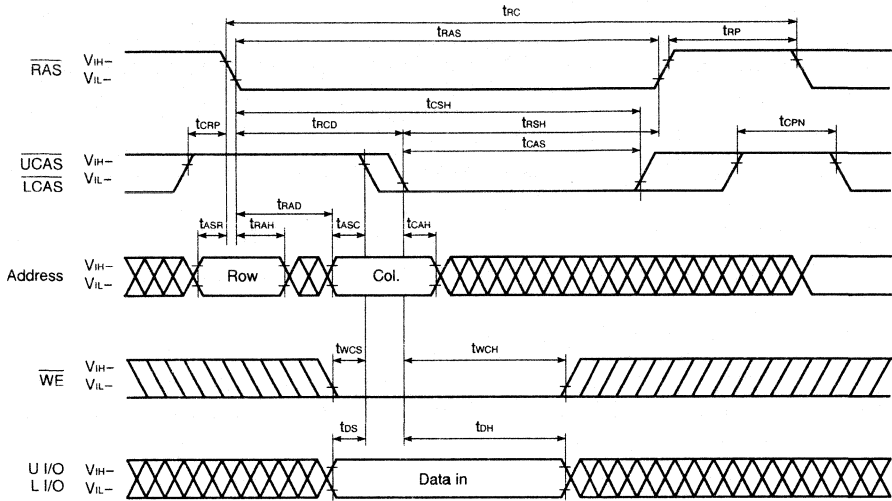
Remark L I/O : Hi-Z

Lower Byte Read Cycle



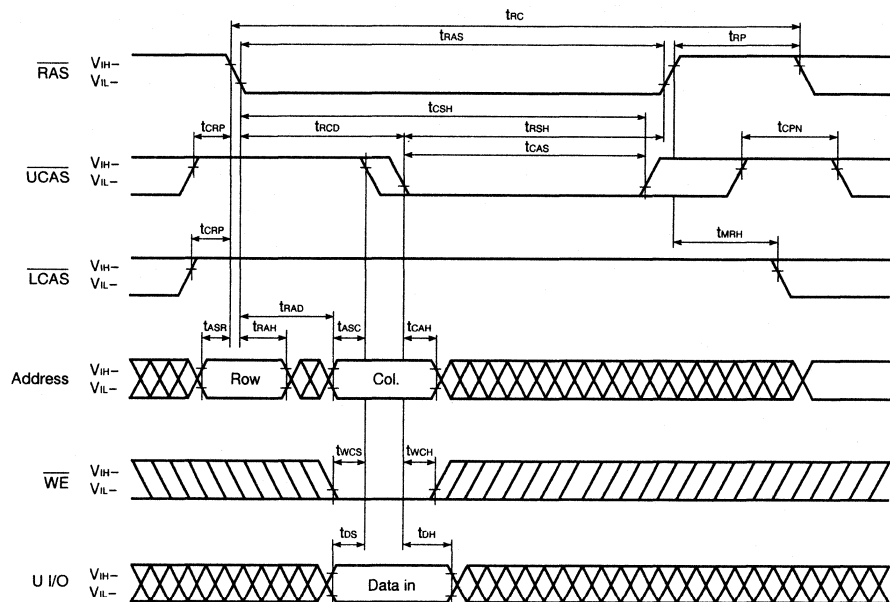
Remark U I/O : Hi-Z

Early Write Cycle



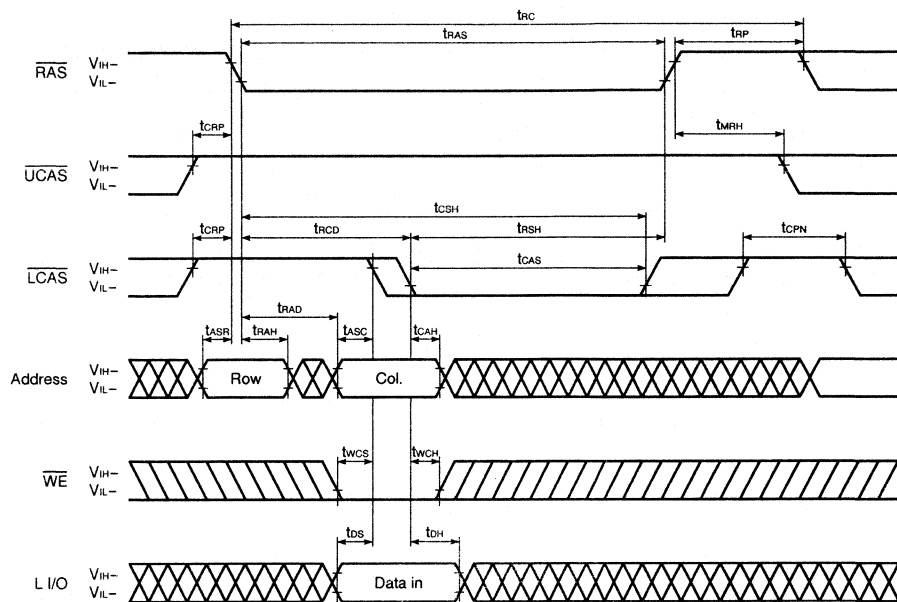
Remark $\overline{\text{OE}}$: Don't care

Upper Byte Early Write Cycle



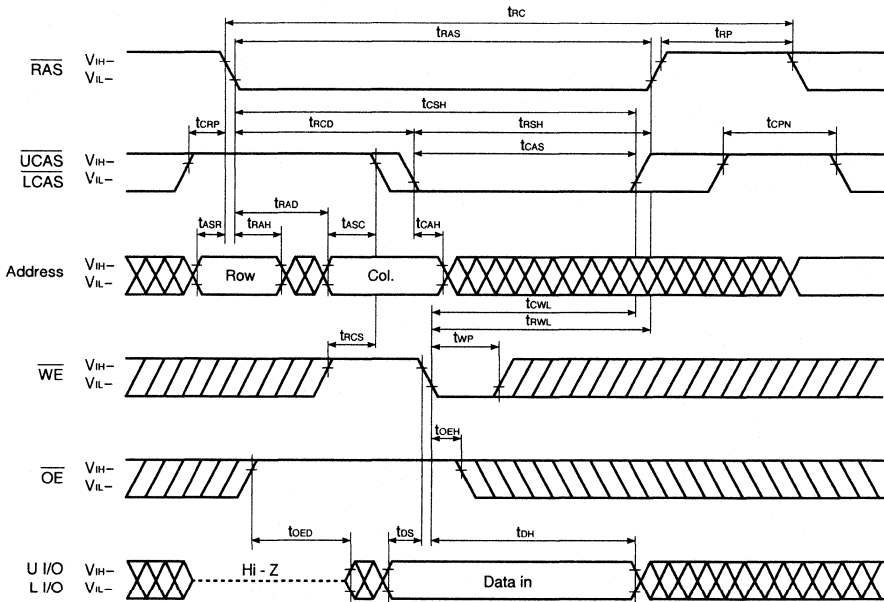
Remark $\overline{OE}$, L I/O : Don't care

Lower Byte Early Write Cycle

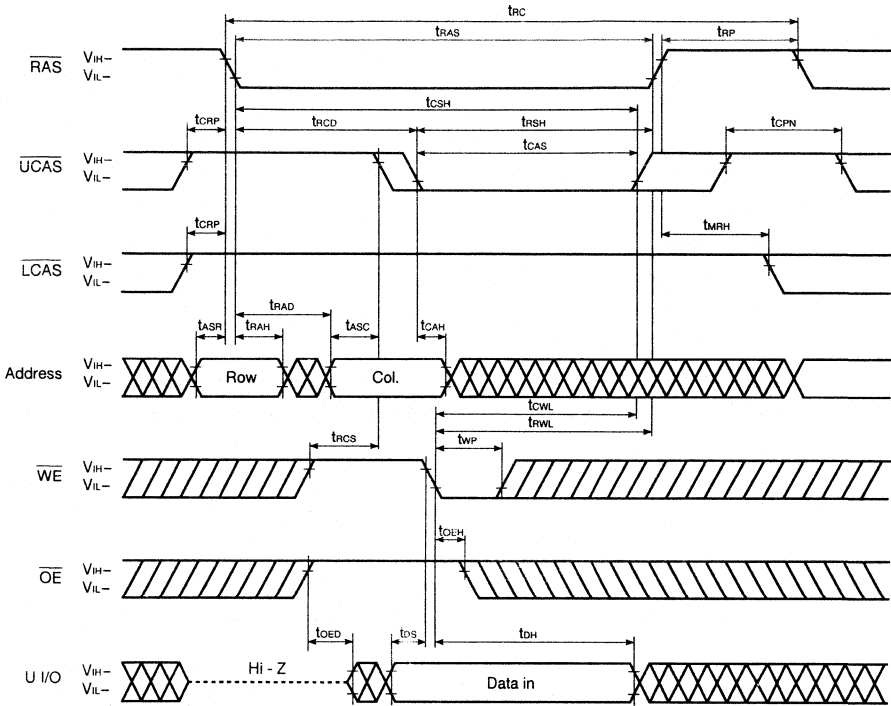


Remark $\overline{\text{OE}}$, U I/O : Don't care

Late Write Cycle

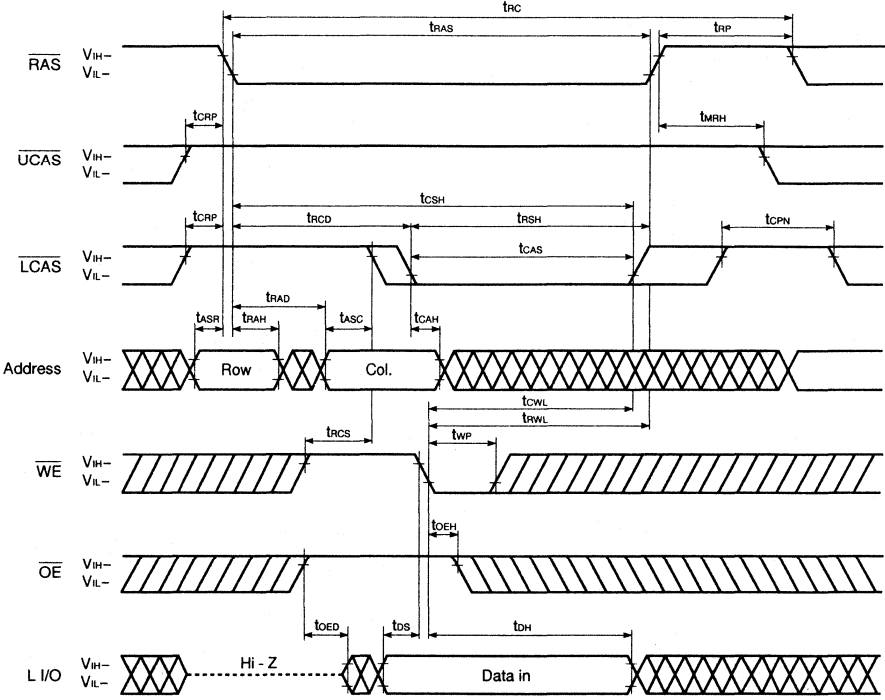


Upper Byte Late Write Cycle



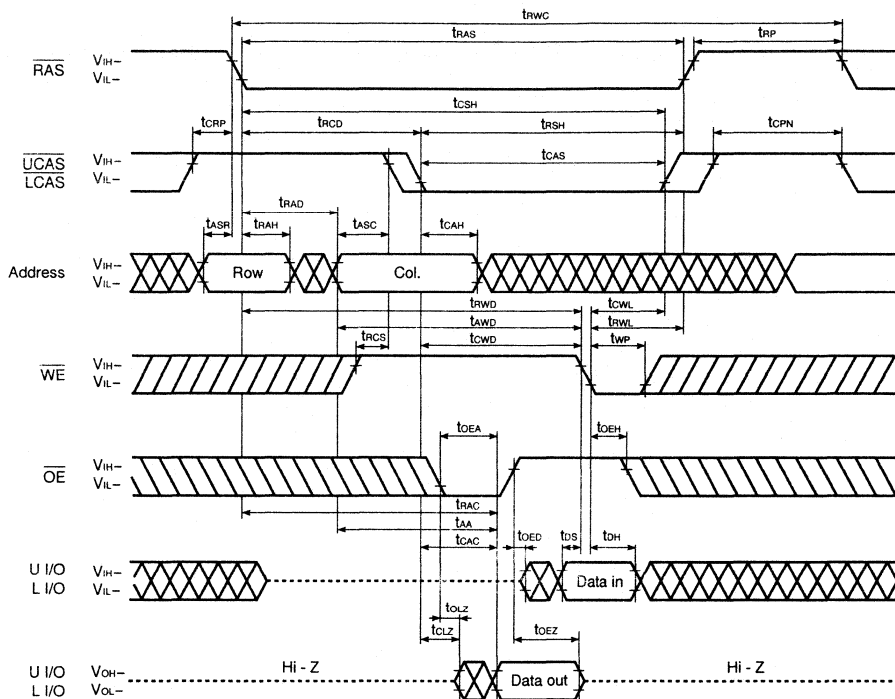
Remark L I/O : Don't care

Lower Byte Late Write Cycle

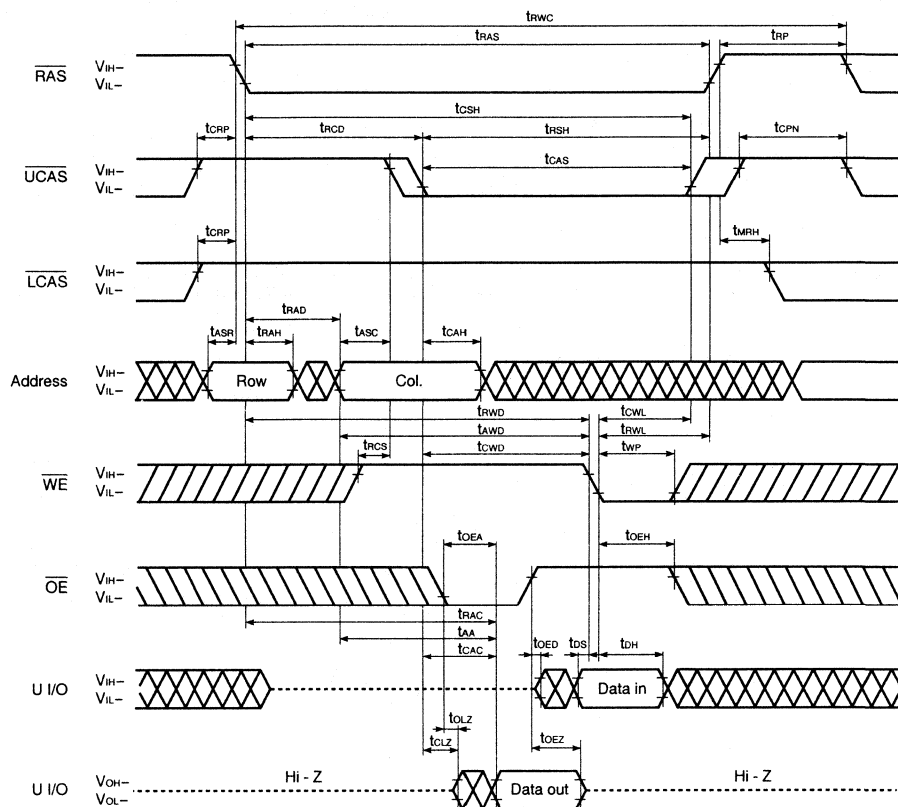


Remark U I/O : Don't care

Read Modify Write Cycle

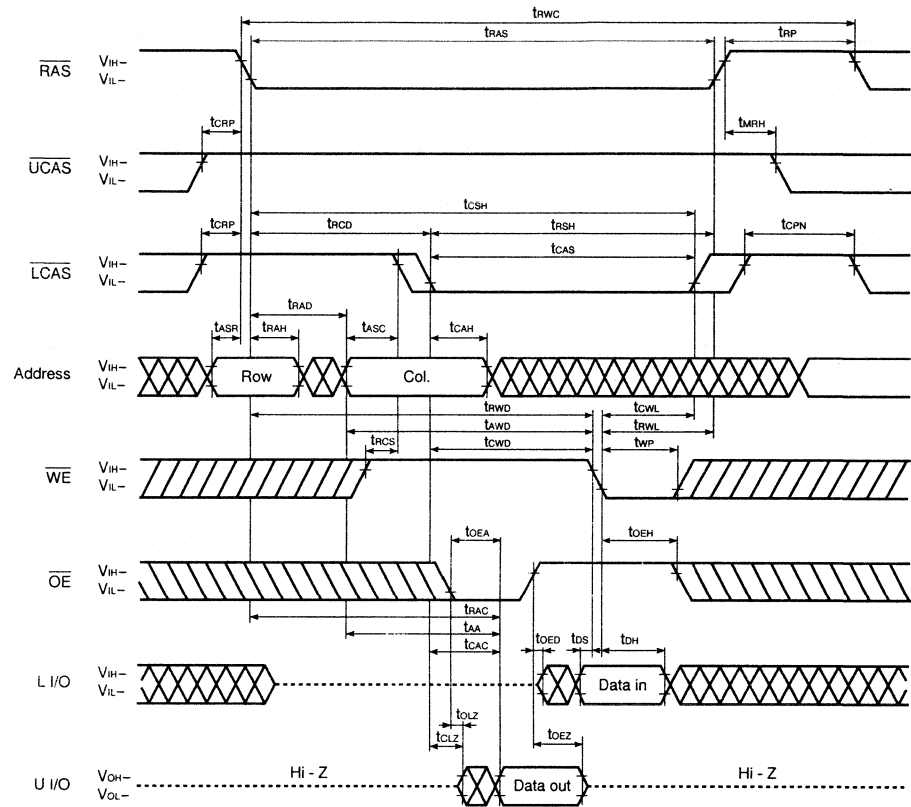


Upper Byte Read Modify Write Cycle



Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle

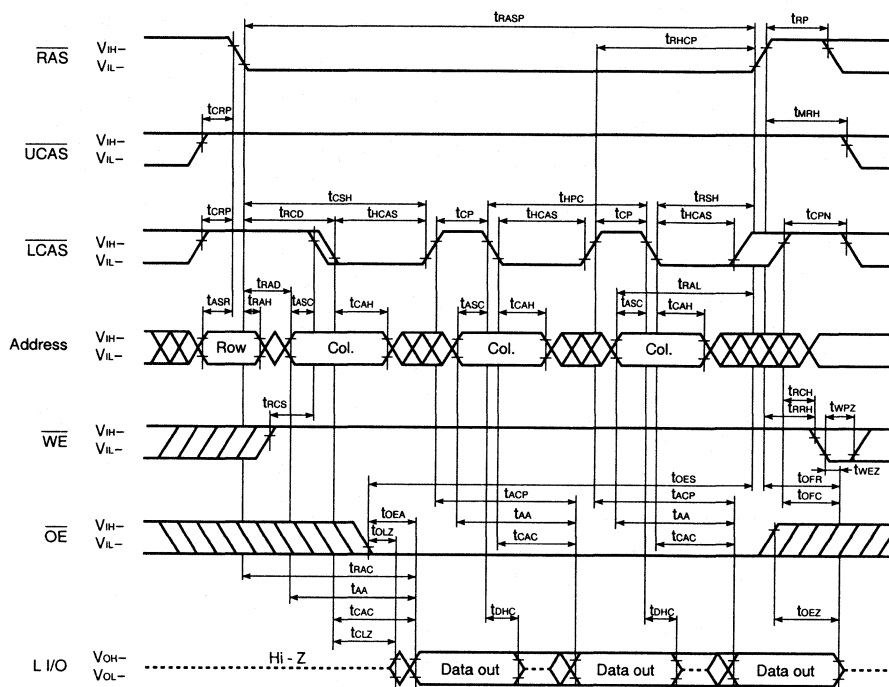


Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

[illegible]

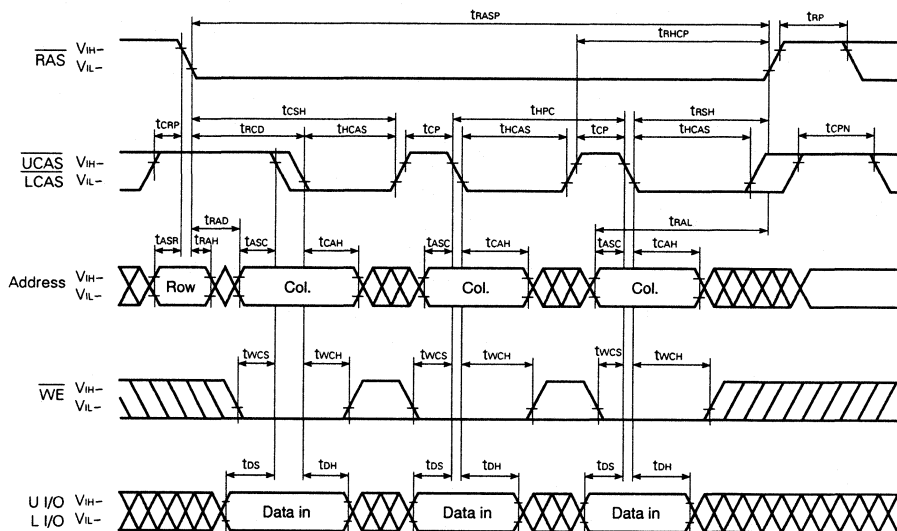
Remark L I/O : Hi-Z

Hyper Page Mode Lower Byte Read Cycle



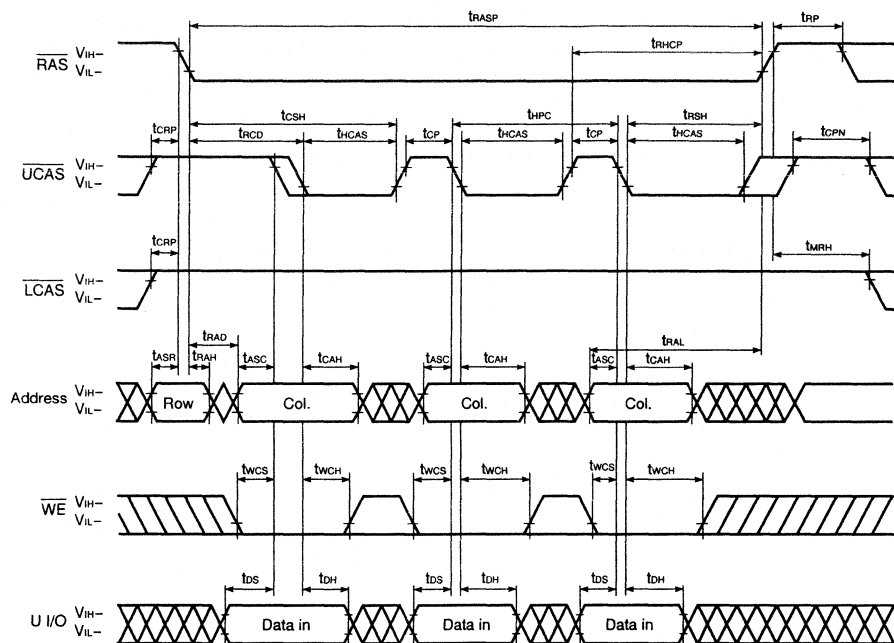
Remark U I/O : Hi-Z

Hyper Page Mode Early Write Cycle



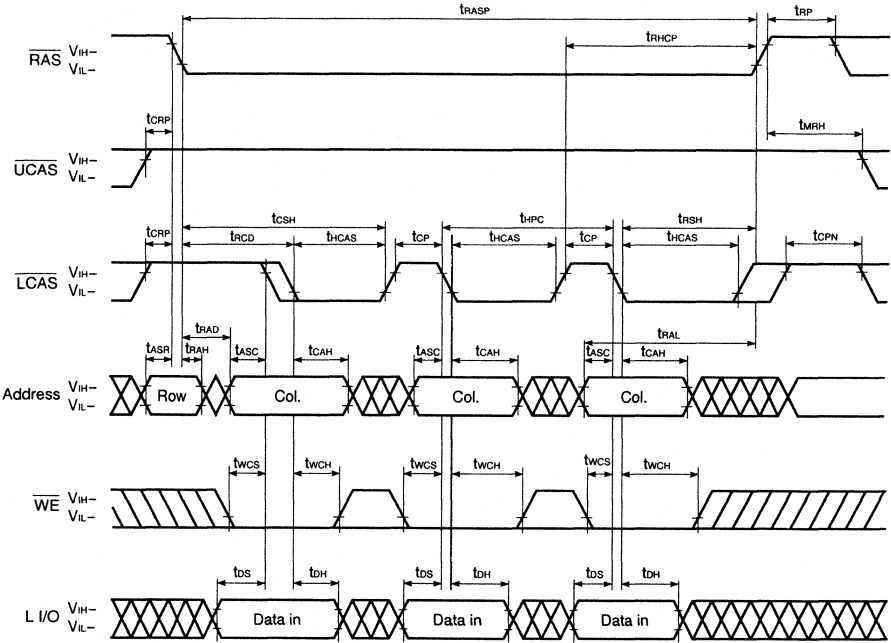
Remark $\overline{OE}$: Don't care

Hyper Page Mode Upper Byte Early Write Cycle



Remark $\overline{OE}$, L I/O : Don't care

Hyper Page Mode Lower Byte Early Write Cycle

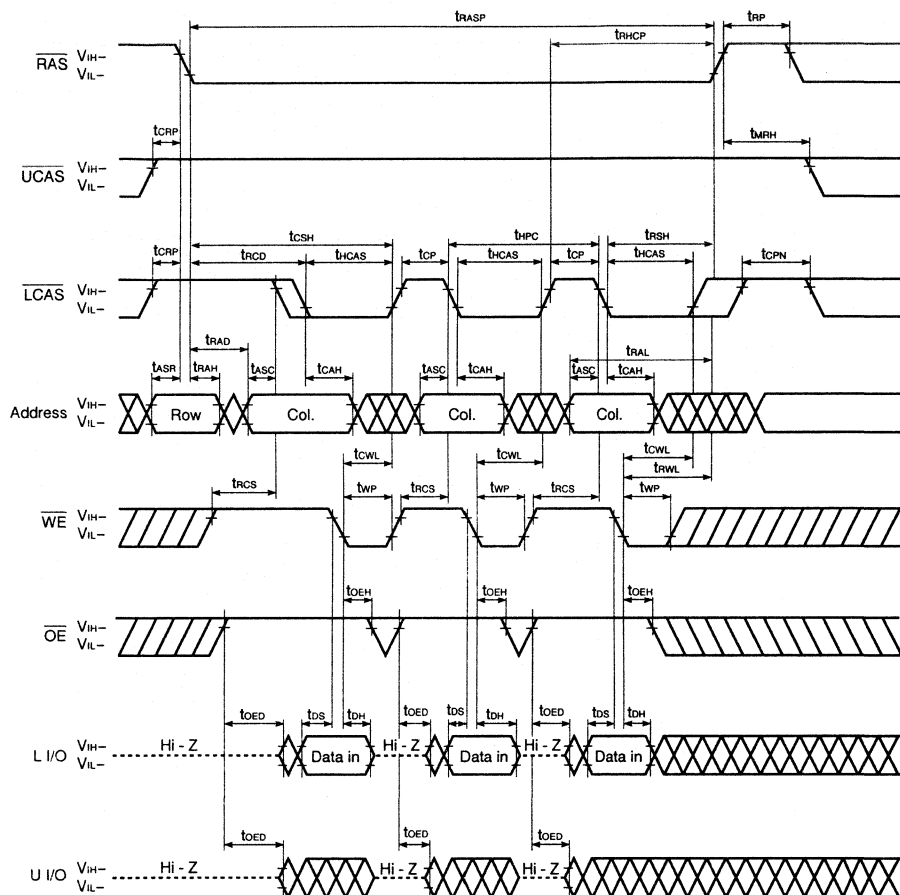


Remark $\overline{OE}$, U I/O : Don't care

[illegible]

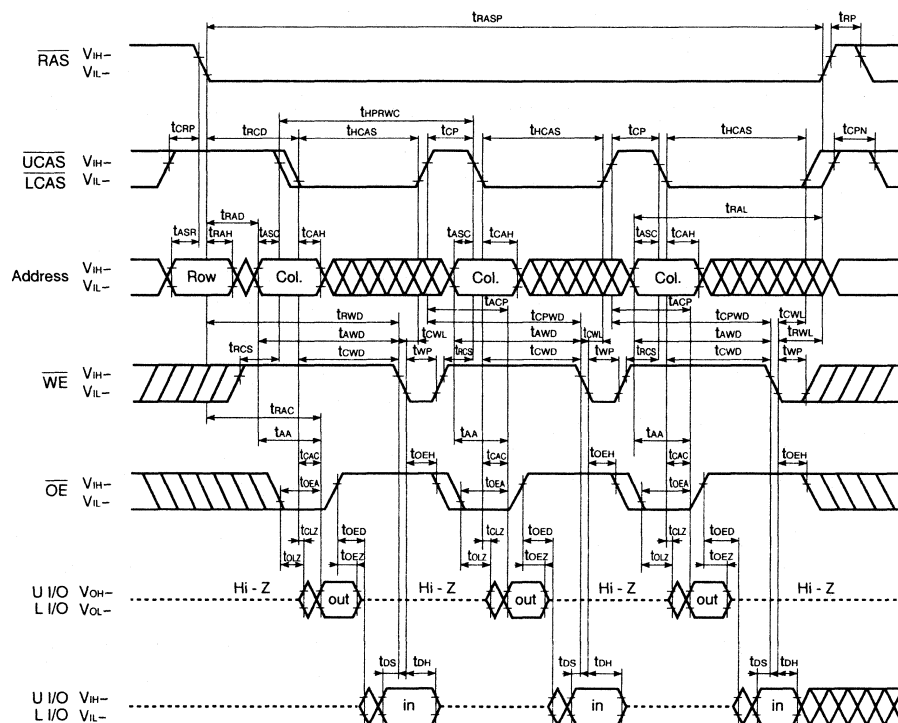
482

Hyper Page Mode Lower Byte Late Write Cycle



Remark In this cycle, the input data to Upper I/O is ineffective.

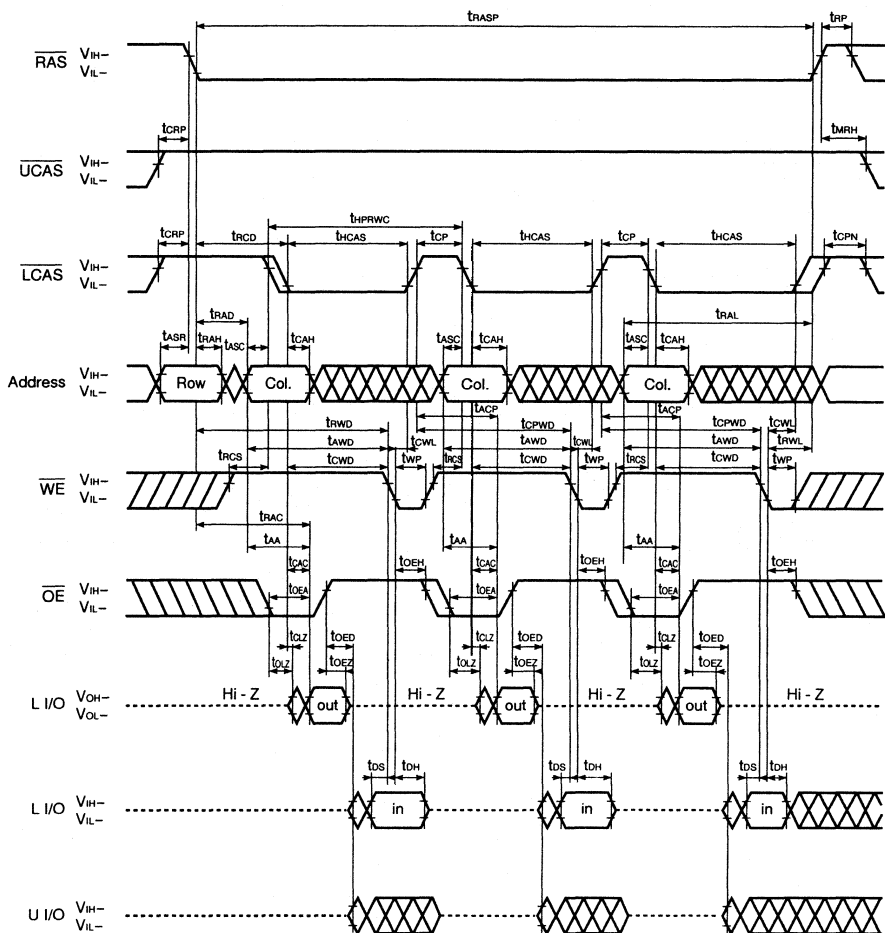
Hyper Page Mode Read Modify Write Cycle



[illegible]

Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

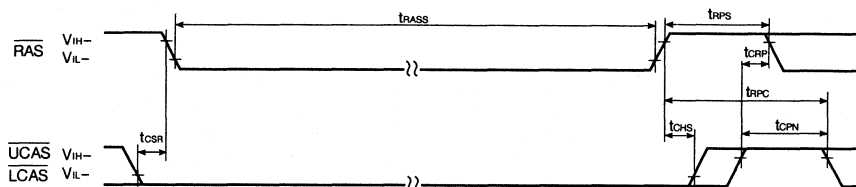
Hyper Page Mode Lower Byte Read Modify Write Cycle



Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

[illegible]

CAS Before RAS Self Refresh Cycle (Only for the μ PD42S16165L)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh

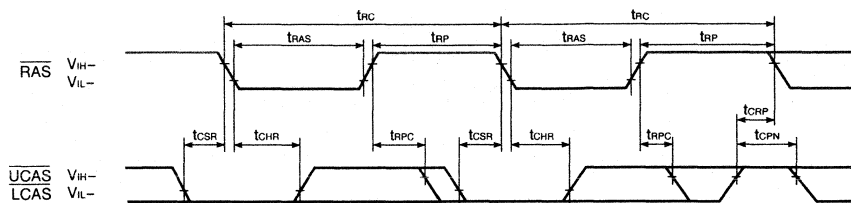
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 4 096 times within a 64 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst Long $\overline{RAS}$ Only Refresh

When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 4 096 times within a 64 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

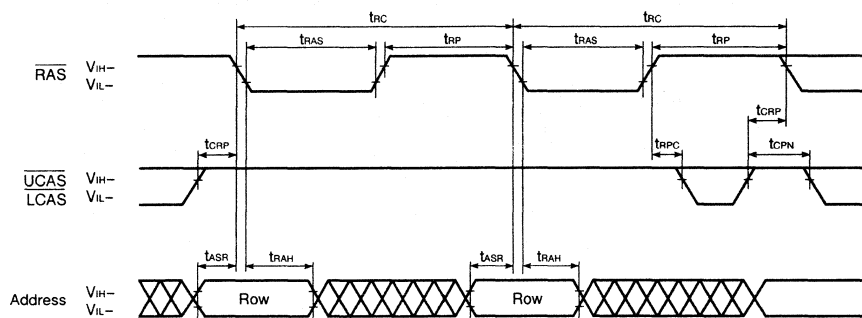
For details, please refer to **How to use DRAM User's Manual**.

CAS Before RAS Refresh Cycle



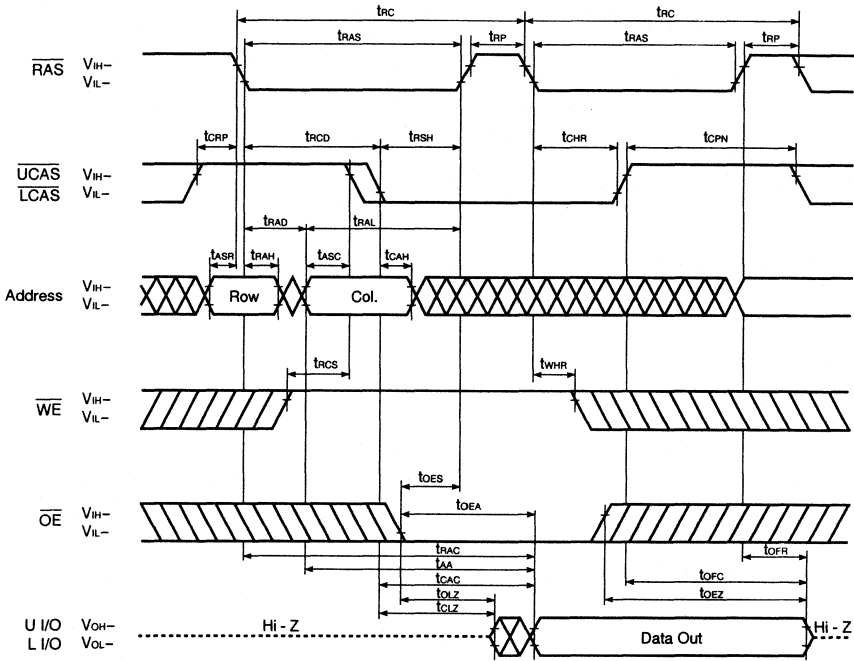
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

RAS Only Refresh Cycle

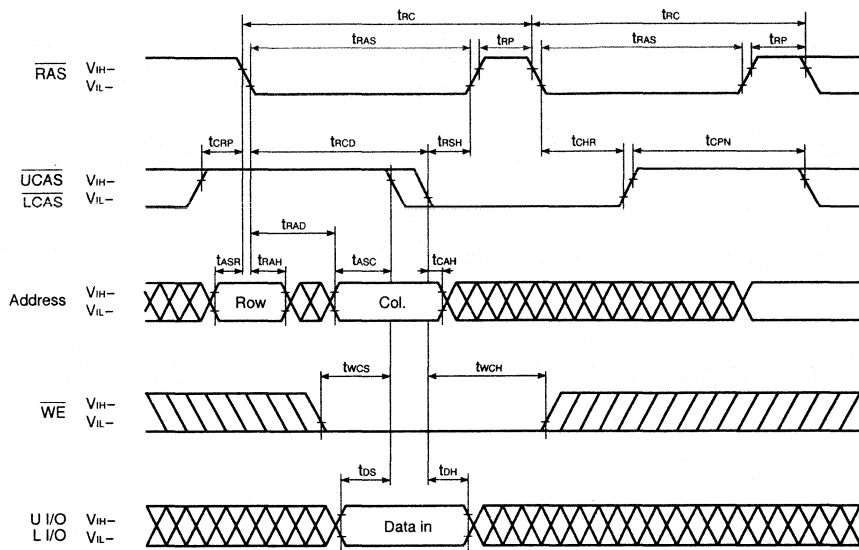


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Hidden Refresh Cycle (Read)



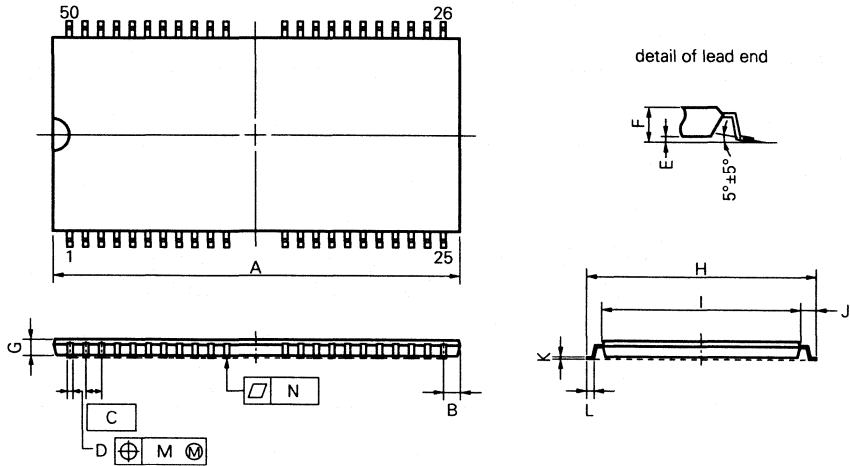
Hidden Refresh Cycle (Write)



Remark $\overline{\text{OE}}$: Don't care

Package Drawings

50 PIN PLASTIC TSOP(III) (400 mil)



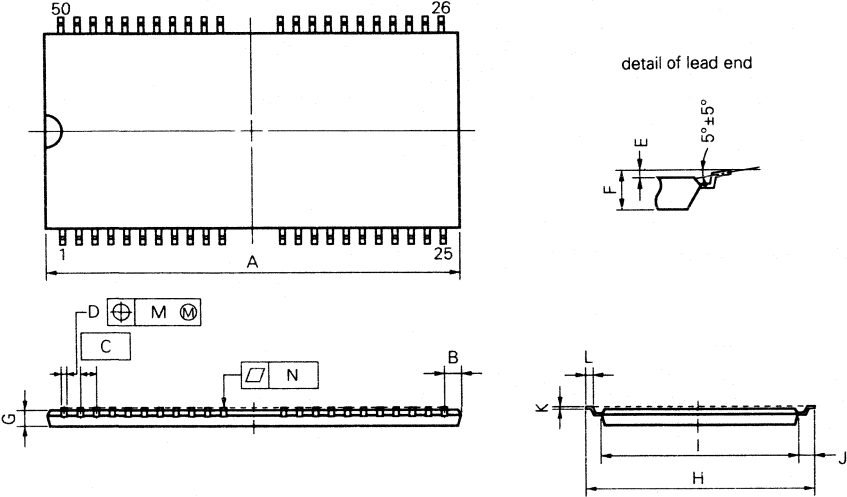
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S50G5-80-7JF-1

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004

50 PIN PLASTIC TSOP(II) (400 mil)



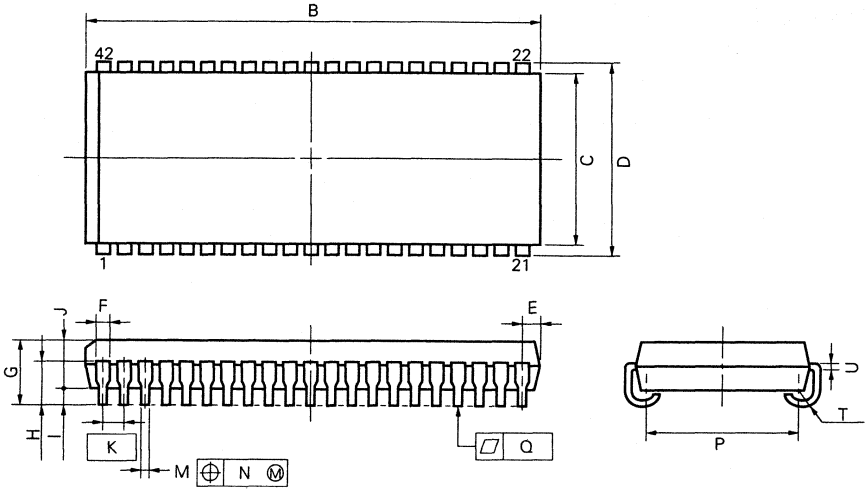
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S50G5-80-7KF-1

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004

42 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P42LE-400A

ITEM	MILLIMETERS	INCHES
B	27.56 ^{+0.2} _{-0.35}	1.085 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD42S16165L, 4216165L.

Types of Surface Mount Device

μ PD42S16165LG5-A $\times\times$ -7JF, 4216165LG5-A $\times\times$ -7JF : 50-pin Plastic TSOP (II) (400 mil)

μ PD42S16165LG5-A $\times\times$ -7KF, 4216165LG5-A $\times\times$ -7KF : 50-pin Plastic TSOP (II) (400 mil) Reverse bent

μ PD42S16165LLE-A $\times\times$, 4216165LLE-A $\times\times$: 42-pin Plastic SOJ (400 mil)

4M Dynamic RAM

[5.0V $\pm$ 10%]



MOS INTEGRATED CIRCUIT
μPD424400**4 M-BIT DYNAMIC RAM
1 M-WORD BY 4-BIT, FAST PAGE MODE****Description**

The μPD424400 is a 1 048 576 words by 4 bits dynamic CMOS RAM. The fast page mode capability realize high speed access and low power consumption.

These are packed in 26-pin plastic TSOP(III), 26-pin plastic SOJ and 20-pin plastic ZIP.

Features

- 1 048 576 words by 4 bits organization
- Single +5.0 V±10 % power supply
- Fast access and cycle time

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μPD424400-60	660 mW	5.5 mW (CMOS level input)	60 ns	120 ns	40 ns
μPD424400-70	550 mW		70 ns	140 ns	45 ns
μPD424400-80	495 mW		80 ns	160 ns	50 ns
μPD424400-10	440 mW		100 ns	190 ns	60 ns

- 1 024 refresh cycles/16 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- Multiplexed address inputs Row address : A0 to A9, Column address : A0 to A9

The information in this document is subject to change without notice.

The mark ★ shows revised points.

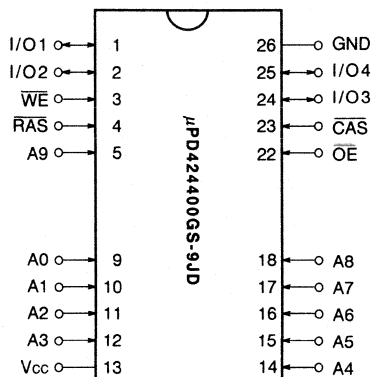
Ordering Information

Part number	Access time (MAX.)	Package	Quality grade
μPD424400GS-60-9JD	60 ns	26-pin Plastic TSOP (II) (300 mil)	Standard
μPD424400GS-70-9JD	70 ns		
μPD424400GS-80-9JD	80 ns		
μPD424400GS-100-9JD	100 ns		
μPD424400GS-60-9KD	60 ns	26-pin Plastic TSOP (II) Reverse bent (300 mil)	
μPD424400GS-70-9KD	70 ns		
μPD424400GS-80-9KD	80 ns		
μPD424400GS-100-9KD	100 ns		
μPD424400LA-60	60 ns	26-pin Plastic SOJ (300 mil)	
μPD424400LA-70	70 ns		
μPD424400LA-80	80 ns		
μPD424400LA-100	100 ns		
μPD424400V-60	60 ns	20-pin Plastic ZIP (400 mil)	
μPD424400V-70	70 ns		
μPD424400V-80	80 ns		
μPD424400V-100	100 ns		

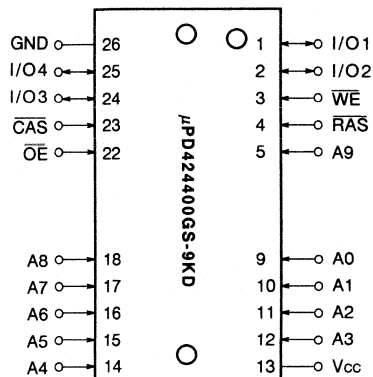
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking Side)

26-pin Plastic TSOP(II) (300 mil)

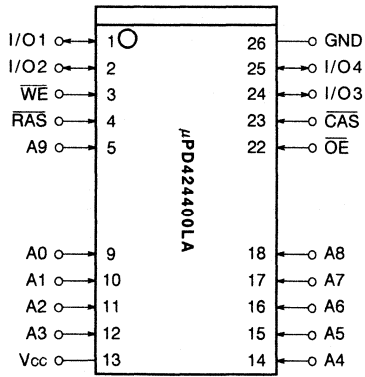


Reverse bent

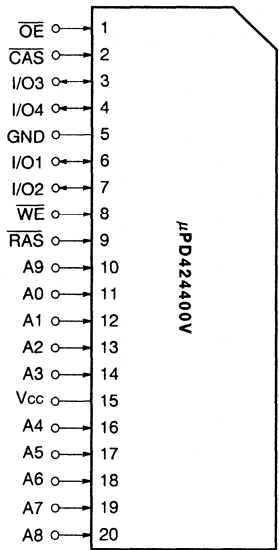


- A0 to A9 : Address Inputs
- I/O1 to I/O4 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground

26-pin Plastic SOJ (300 mil)

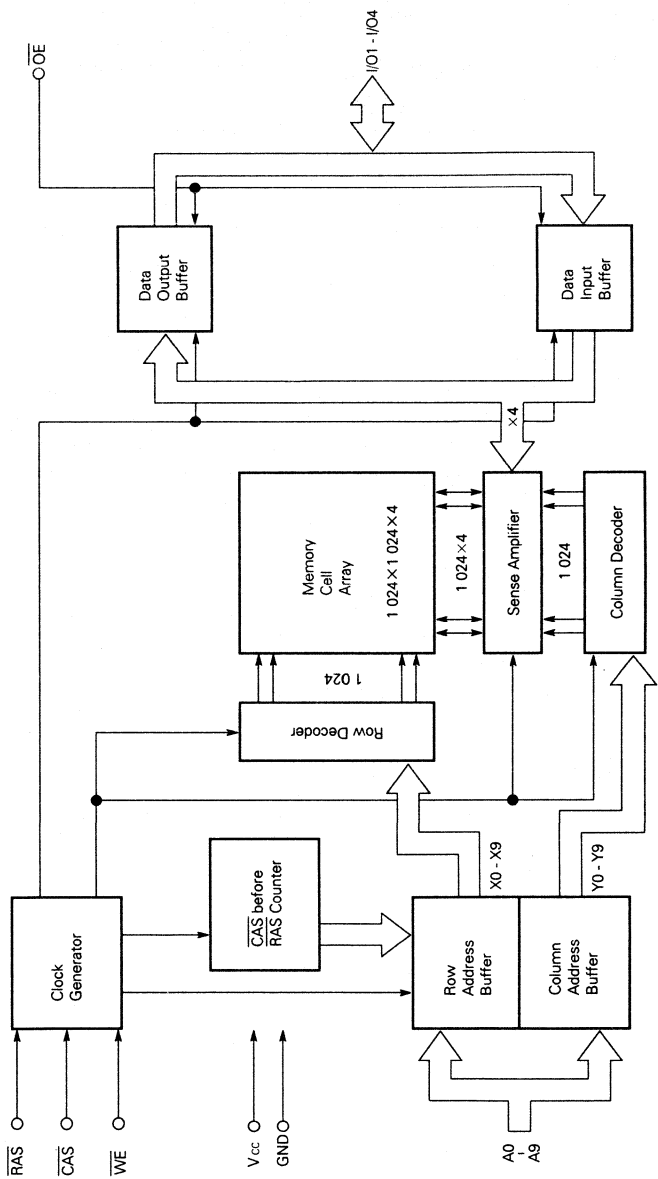


20-pin Plastic ZIP (400 mil)



- A0 to A9 : Address Inputs
- I/O1 to I/O4 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground

Block Diagram



Input/Output Pin Functions

The μ PD424400 has input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A9 and input/output pins I/O1 to I/O4.

Pin Name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address input)		Address bus. Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input/ Output	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data input/output)		4-bit data bus. I/O1 to I/O4 are used to input/output data.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		120	mA	1, 2, 3
			$t_{\text{RAC}} = 70 \text{ ns}$		100		
			$t_{\text{RAC}} = 80 \text{ ns}$		90		
			$t_{\text{RAC}} = 100 \text{ ns}$		80		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), I_o = 0 \text{ mA}$			2	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_o = 0 \text{ mA}$			1		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.}), I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		120	mA	1,2,3,4
			$t_{\text{RAC}} = 70 \text{ ns}$		100		
			$t_{\text{RAC}} = 80 \text{ ns}$		90		
			$t_{\text{RAC}} = 100 \text{ ns}$		80		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.}), I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		90	mA	1, 2, 5
			$t_{\text{RAC}} = 70 \text{ ns}$		80		
			$t_{\text{RAC}} = 80 \text{ ns}$		70		
			$t_{\text{RAC}} = 100 \text{ ns}$		60		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		120	mA	1, 2
			$t_{\text{RAC}} = 70 \text{ ns}$		100		
			$t_{\text{RAC}} = 80 \text{ ns}$		90		
			$t_{\text{RAC}} = 100 \text{ ns}$		80		
Input leakage current	I _{I (L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10		+10	μA	
Output leakage current	I _{O (L)}	$V_o = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10		+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4			V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$			0.4	V	

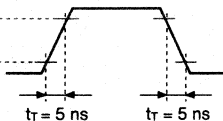
- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)**AC Characteristics Test Conditions**

(1) Input timing specification

$V_{IH} (\text{MIN.}) = 2.4 \text{ V}$

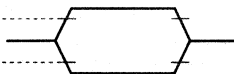
$V_{IL} (\text{MAX.}) = 0.8 \text{ V}$



(2) Output timing specification

$V_{OH} (\text{MIN.}) = 2.4 \text{ V}$

$V_{OL} (\text{MAX.}) = 0.4 \text{ V}$



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{RC}	120	–	140	–	160	–	190	–	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	50	–	60	–	70	–	80	–	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20	–	20	–	20	–	25	–	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60	–	70	–	80	–	100	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	25	75	ns	1
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	17	50	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10	–	10	–	10	–	10	–	ns	2
Row Address Setup Time	t _{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t _{RAH}	10	–	10	–	12	–	12	–	ns	
Column Address Setup Time	t _{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t _{CAH}	15	–	15	–	15	–	20	–	ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{OES}	0	–	0	–	0	–	0	–	ns	
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0	–	0	–	0	–	0	–	ns	
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0	–	0	–	0	–	0	–	ns	
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	15	–	15	–	20	–	25	–	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
Refresh Time	t _{REF}	–	16	–	16	–	16	–	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
t _{RAD} ≤ t _{RAD} (MAX.) and t _{RCD} ≤ t _{RCD} (MAX.)	t _{RAC} (MAX.)	t _{RAC} (MAX.)
t _{RAD} > t _{RAD} (MAX.) and t _{RCD} ≤ t _{RCD} (MAX.)	t _{AA} (MAX.)	t _{RAD} + t _{AA} (MAX.)
t _{RCD} > t _{RCD} (MAX.)	t _{CAC} (MAX.)	t _{RCD} + t _{CAC} (MAX.)

t_{RAD}(MAX.) and t_{RCD}(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions t_{RAD} ≥ t_{RAD}(MAX.) and t_{RCD} ≥ t_{RCD}(MAX.) will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied for $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycle.

Read Cycle

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		$t_{RAC} = 80 \text{ ns}$		$t_{RAC} = 100 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	–	100	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	20	–	20	–	25	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	–	40	–	50	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	20	–	20	–	20	–	25	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	40	–	50	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	3
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	0	25	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi - Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	15	–	15	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	15	–	15	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	20	–	20	–	20	–	25	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	15	–	15	–	15	–	20	–	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	–	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	–	0	–	0	–	0	–	ns	
Data-in Setup Time	t _{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in Hold Time	t _{DH}	15	–	15	–	15	–	20	–	ns	3

- Notes**
1. t_{WP(MIN.)} is applied for late write cycles or read modify write cycles. In early write cycles, t_{WCH(MIN.)} should be met.
 2. If t_{WCS} $\geq$ t_{WCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle.
 3. t_{DS(MIN.)} and t_{DH(MIN.)} are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	165	–	185	–	210	–	250	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	80	–	90	–	105	–	130	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	40	–	40	–	45	–	55	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	50	–	55	–	65	–	80	–	ns	1

- Note**
1. If t_{WCS} $\geq$ t_{WCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If t_{trwd} $\geq$ t_{trwd(MIN.)}, t_{tcwd} $\geq$ t_{tcwd(MIN.)}, t_{tawd} $\geq$ t_{tawd(MIN.)}, and t_{tcpwd} $\geq$ t_{tcpwd(MIN.)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

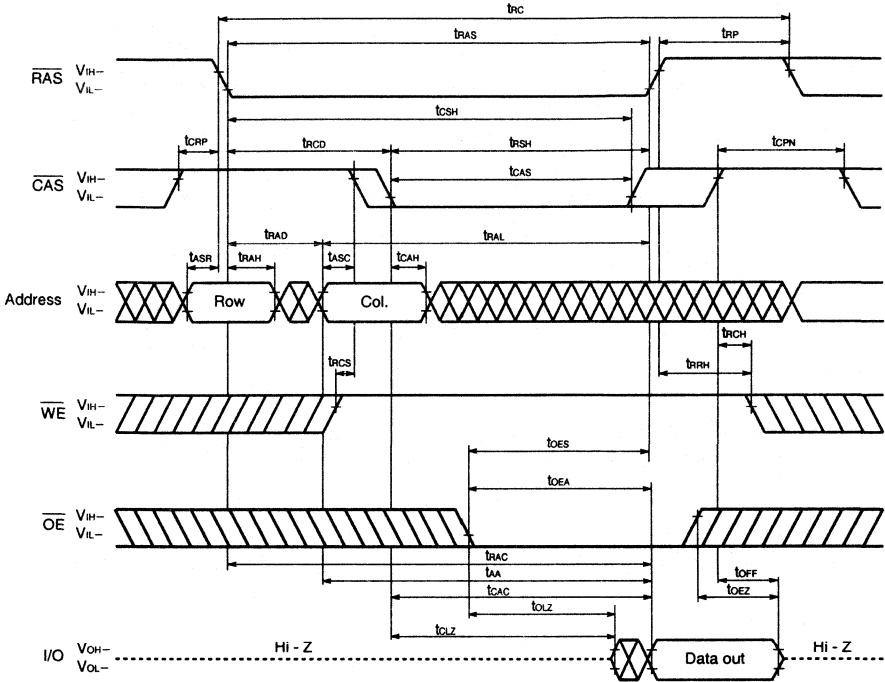
Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{FC}	40	–	45	–	50	–	60	–	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	–	35	–	40	–	45	–	55	ns	
RAS Pulse Width	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	–	10	–	10	–	10	–	ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35	–	40	–	45	–	55	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	85	–	90	–	100	–	120	–	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	55	–	60	–	70	–	85	–	ns	1

Note 1. If $t_{\text{WCS}} \geq t_{\text{WCS(MIN.)}}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD(MIN.)}}$, $t_{\text{CWD}} \geq t_{\text{CWD(MIN.)}}$, $t_{\text{AWD}} \geq t_{\text{AWD(MIN.)}}$, and $t_{\text{CPWD}} \geq t_{\text{CPWD(MIN.)}}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

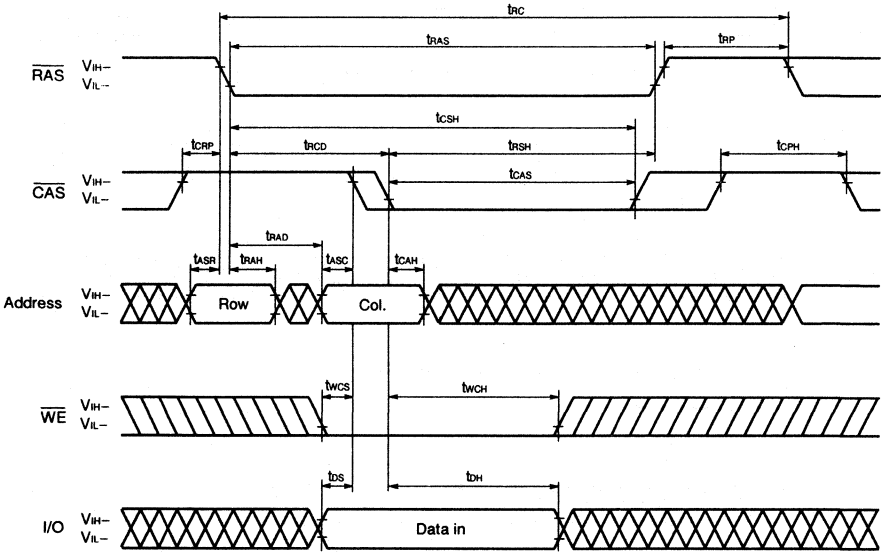
Refresh Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ Setup Time	t _{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	15	–	15	–	15	–	20	–	ns	
RAS Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15	–	15	–	15	–	20	–	ns	

Read Cycle

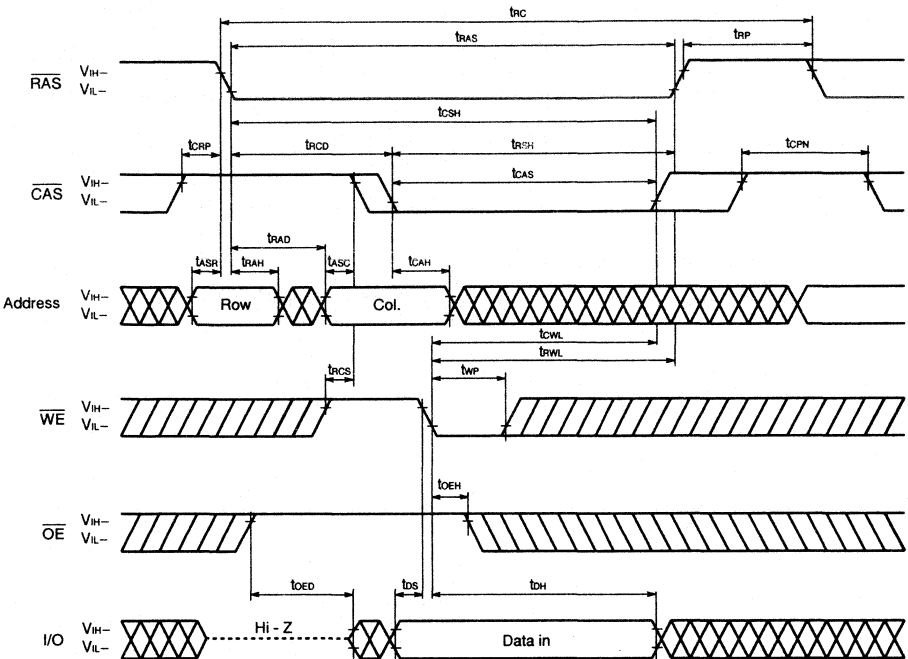


Early Write Cycle

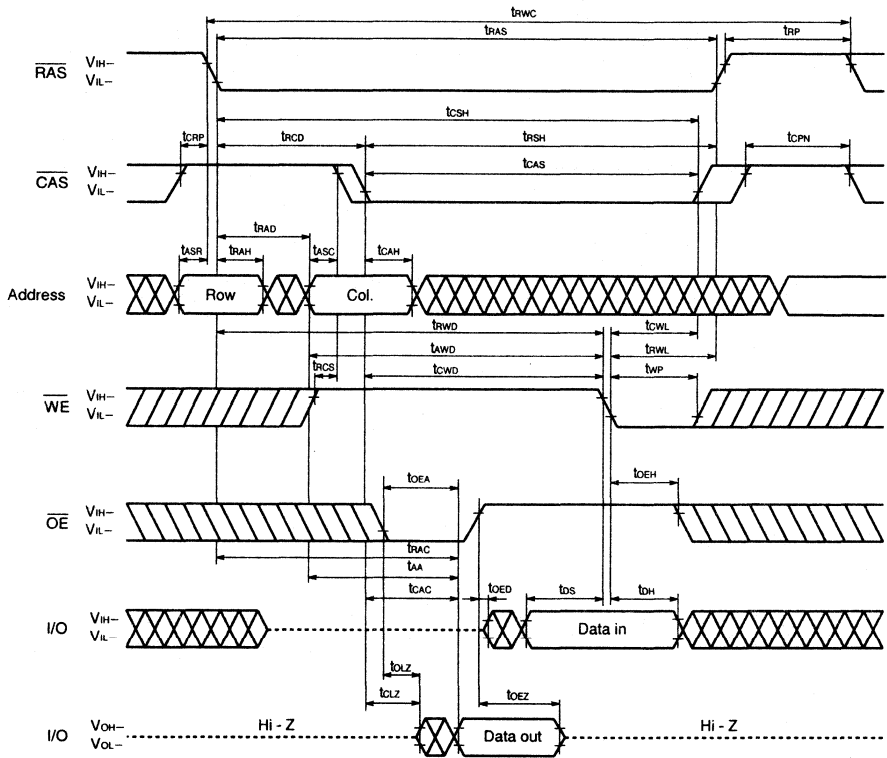


Remark $\overline{OE}$: Don't care

Late Write Cycle



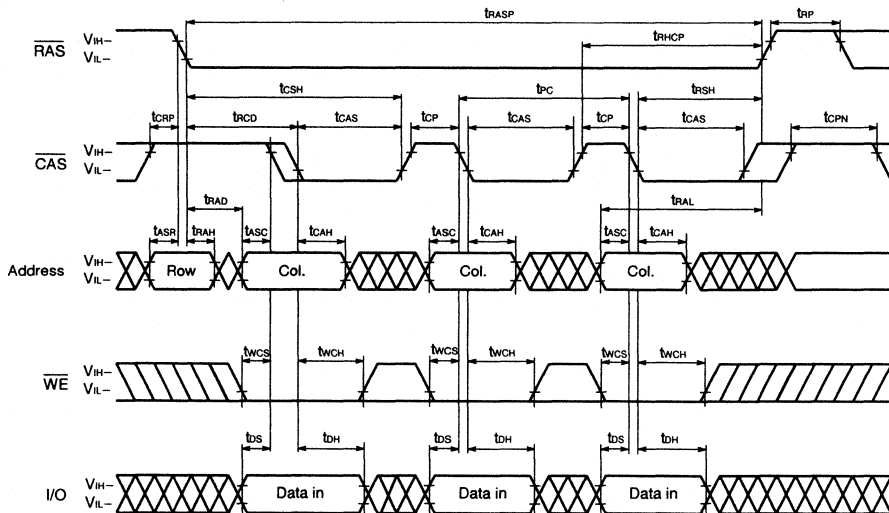
★ Read Modify Write Cycle



[illegible]

515

Fast Page Mode Early Write Cycle



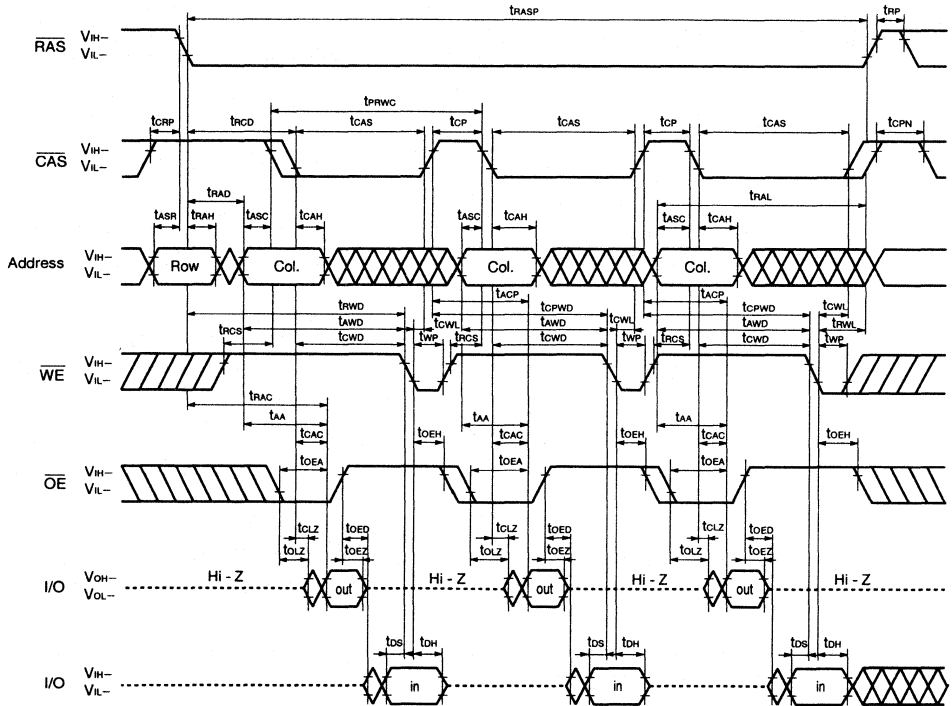
Remark $\overline{OE}$: Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

[illegible]

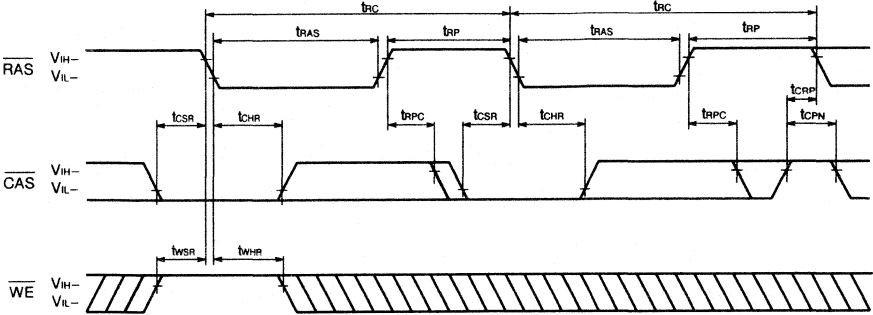
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

★ Fast Page Mode Read Modify Write Cycle



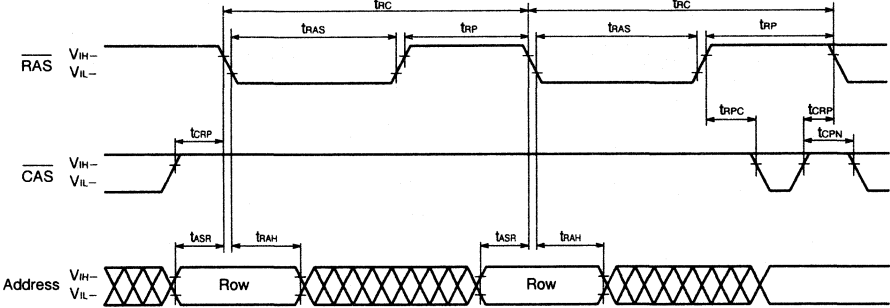
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



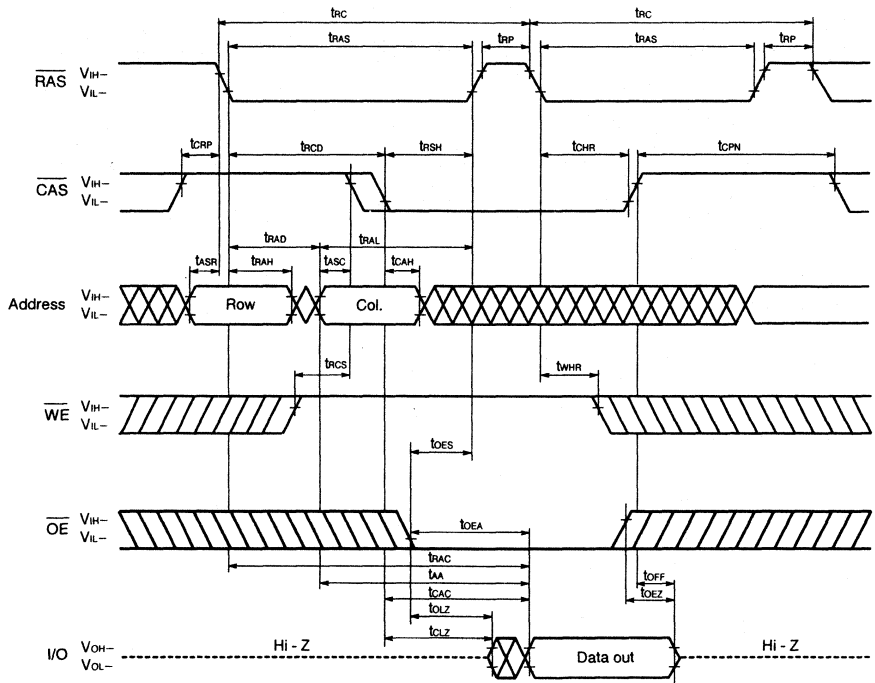
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

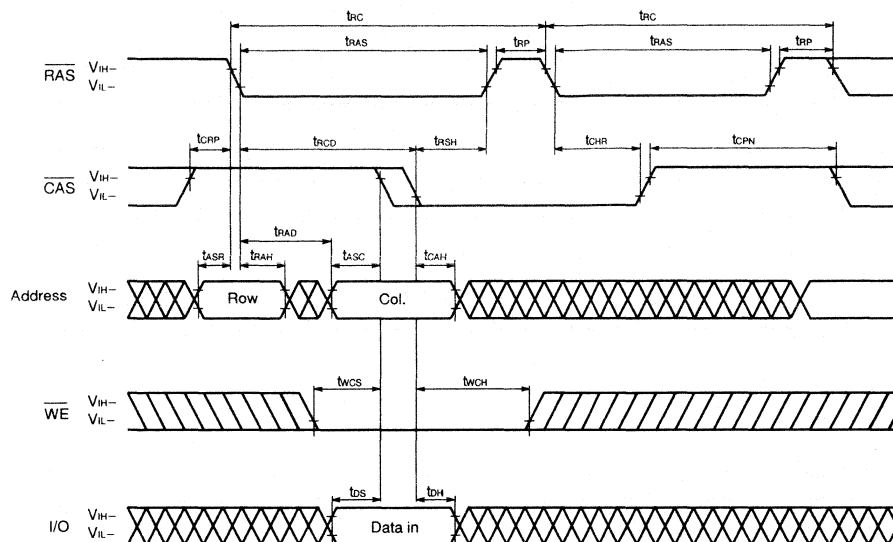


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

★ Hidden Refresh Cycle (Read)

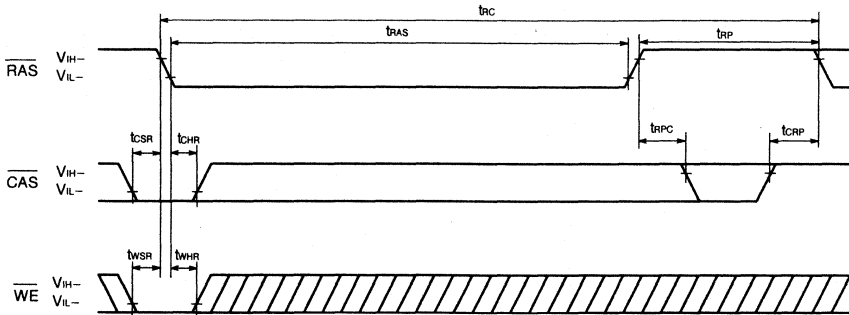


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)



Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 8$ -bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 8 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output="1": Normal write (all memory cells)

Output="0": Abnormal write

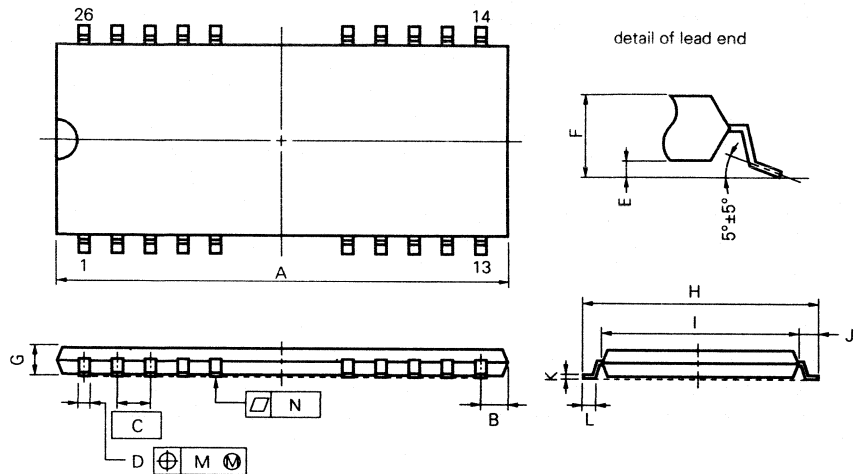
(3) Refresh

Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

Package Drawings
26 PIN PLASTIC TSOP(III) (300 mil)

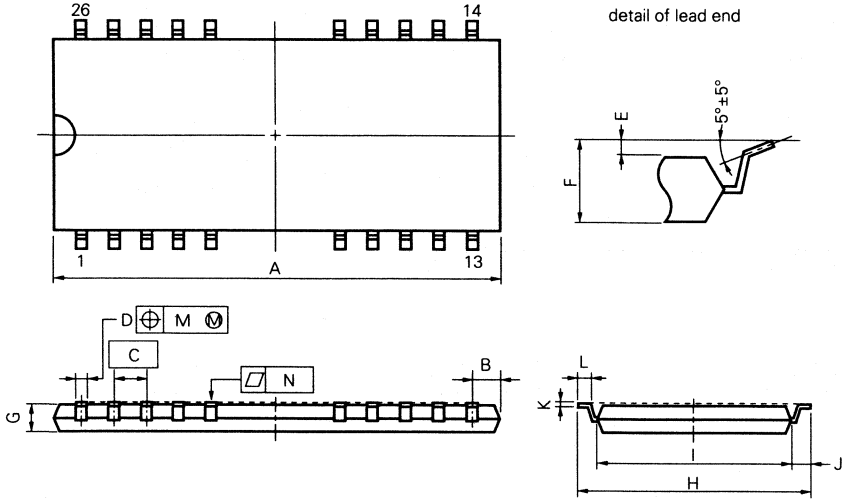


NOTE
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S26GS-50-9JD-2

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0.691 MAX.
B	1.18 MAX.	0.047 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.13 MAX.	0.045 MAX.
G	1.0	0.039
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

26 PIN PLASTIC TSOP(II) (300 mil)



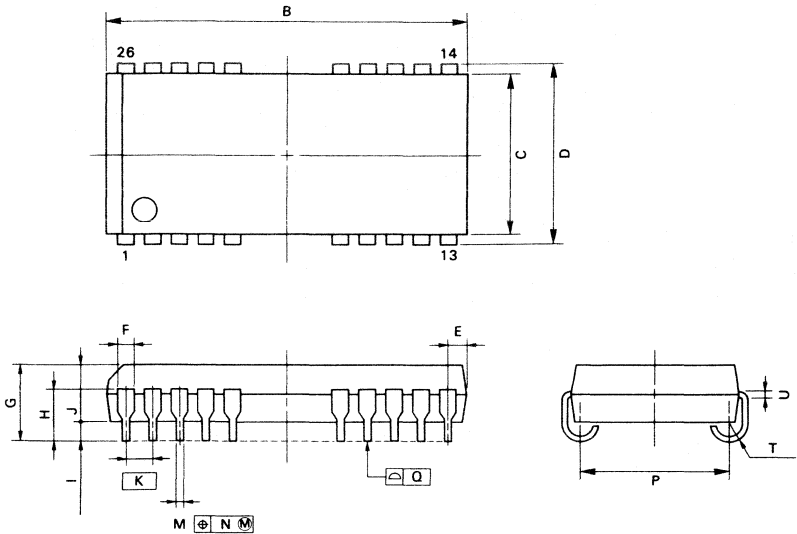
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S26GS-50-9KD-2

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0.691 MAX.
B	1.18 MAX.	0.047 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.13 MAX.	0.045 MAX.
G	1.0	0.039
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

26PIN PLASTIC SOJ (300 mil)

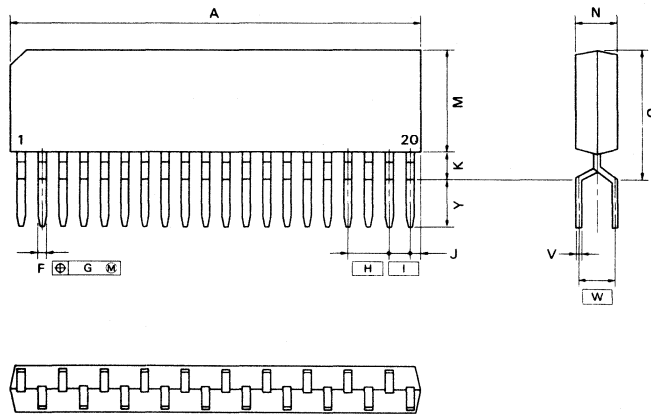


P26LA-50A-1

NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	17.4 ^{+0.2} _{-0.35}	0.685 ^{+0.008} _{-0.013}
C	7.57	0.298
D	8.47 ^{+0.2}	0.333 ^{+0.008} _{-0.008}
E	1.08 ^{+0.15}	0.043 ^{+0.006} _{-0.007}
F	0.6	0.024
G	3.5 ^{+0.2}	0.138 ^{+0.008}
H	2.4 ^{+0.2}	0.094 ^{+0.009} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40 ^{+0.10}	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73 ^{+0.20}	0.265 ^{+0.008}
Q	0.15	0.006
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

20PIN PLASTIC ZIP (400 mil)



NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P20V-254-400A-1

ITEM	MILLIMETERS	INCHES
A	26.67 MAX.	1.050 MAX.
F	$0.5^{+0.1}$	$0.020^{+0.008}_{-0.008}$
G	$\phi 0.25$	$\phi 0.010$
H	2.54	0.100
I	1.27	0.050
J	1.27 MAX.	0.050 MAX.
K	1.0 MIN.	0.039 MIN.
M	8.9 MAX.	0.350 MAX.
N	$2.8^{+0.2}$	$0.110^{+0.008}_{-0.008}$
Q	10.16 MAX.	0.400 MAX.
V	$0.25^{+0.10}_{-0.08}$	$0.010^{+0.008}_{-0.008}$
W	2.54	0.100
Y	$3.3^{+0.5}$	$0.130^{+0.02}$

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD424400.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD424400GS : 26-pin plastic TSOP(II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD424400LA : 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit^{Note}: 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit^{Note}: 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

★ **Type of Through Hole Mount Device**

μPD424400V : 26-pin plastic ZIP (400 mil)

Soldering process	Soldering conditions
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below
Partial heating method	Terminal temperature : 260 °C below, Time : 10 seconds or below

Caution Do not jet molten solder on the surface of package.

MOS INTEGRATED CIRCUIT
 μ PD424400-L**4 M-BIT DYNAMIC RAM
1 M-WORD BY 4-BIT, FAST PAGE MODE****Description**

The μ PD424400-L is a 1 048 576 words by 4 bits dynamic CMOS RAM. The fast page mode capability realize high speed access and low power consumption.

These are packed in 26-pin plastic TSOP(II), 26-pin plastic SOJ and 20-pin plastic ZIP.

Features

- 1 048 576 words by 4 bits organization • Single +5.0 V $\pm$ 10 % power supply
- Fast access and cycle time

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μ PD424400-60L	660 mW	1.1 mW (CMOS level input)	60 ns	120 ns	40 ns
μ PD424400-70L	550 mW		70 ns	140 ns	45 ns
μ PD424400-80L	495 mW		80 ns	160 ns	50 ns
μ PD424400-10L	440 mW		100 ns	190 ns	60 ns

- 1 024 refresh cycles/128 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- Multiplexed address inputs Row address : A0 to A9, Column address : A0 to A9

The information in this document is subject to change without notice.

The mark ★ shows revised points.

★ Ordering Information

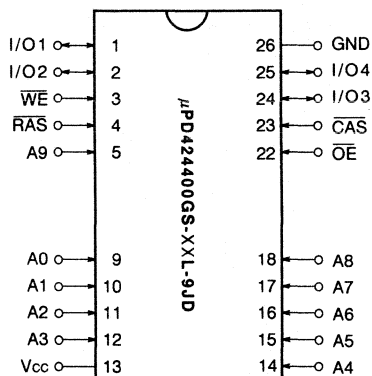
Part number	Access time (MAX.)	Package	Quality grade
μPD424400GS-60L-9JD	60 ns	26-pin Plastic TSOP(II) (300 mil)	Standard
μPD424400GS-70L-9JD	70 ns		
μPD424400GS-80L-9JD	80 ns		
μPD424400GS-10L-9JD	100 ns		
μPD424400GS-60L-9KD	60 ns	26-pin Plastic TSOP(II) Reverse bent (300 mil)	
μPD424400GS-70L-9KD	70 ns		
μPD424400GS-80L-9KD	80 ns		
μPD424400GS-10L-9KD	100 ns		
μPD424400LA-60L	60 ns	26-pin Plastic SOJ (300 mil)	
μPD424400LA-70L	70 ns		
μPD424400LA-80L	80 ns		
μPD424400LA-10L	100 ns		
μPD424400V-60L	60 ns	20-pin Plastic ZIP (400 mil)	
μPD424400V-70L	70 ns		
μPD424400V-80L	80 ns		
μPD424400V-10L	100 ns		

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

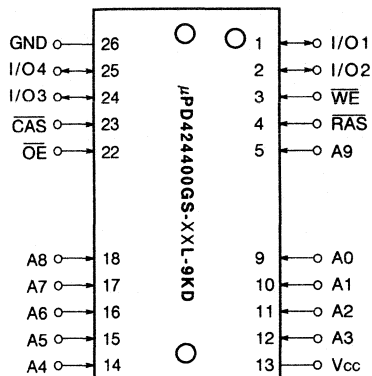
Pin Configurations (Marking Side)



26-pin Plastic TSOP(II) (300 mil)



Reverse bent



A0 to A9 : Address Inputs

I/O1 to I/O4 : Data Inputs/Outputs

RAS : Row Address Strobe

CAS : Column Address Strobe

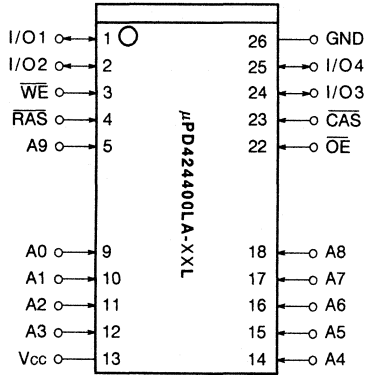
WE : Write Enable

OE : Output Enable

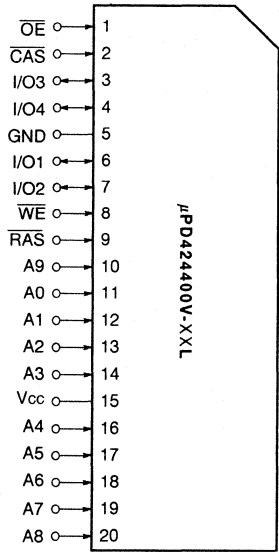
Vcc : Power Supply

GND : Ground

26-pin Plastic SOJ (300 mil)

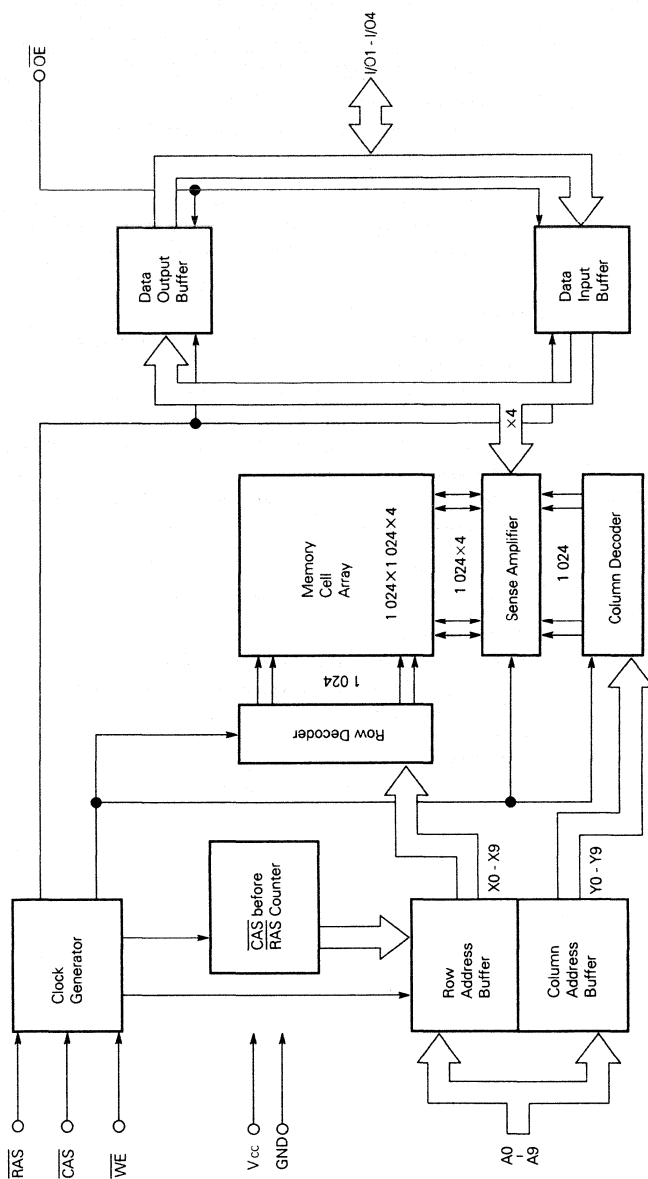


20-pin Plastic ZIP (400 mil)



- A0 to A9 : Address Inputs
I/O1 to I/O4 : Data Inputs/Outputs
RAS : Row Address Strobe
CAS : Column Address Strobe
WE : Write Enable
OE : Output Enable
Vcc : Power Supply
GND : Ground

Block Diagram



★ **Input/Output Pin Functions**

The μPD424400-L has input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A9 and input/output pins I/O1 to I/O4.

Pin Name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address input)		Address bus. Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data input/output)	Input/ Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

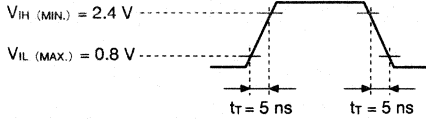
Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		120	mA	1, 2, 3
			$\text{trac} = 70 \text{ ns}$		100		
			$\text{trac} = 80 \text{ ns}$		90		
			$\text{trac} = 100 \text{ ns}$		80		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH}(\text{MIN.}), I_o = 0 \text{ mA}$			2	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}, I_o = 0 \text{ mA}$			0.2		
RAS only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.}), I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		120	mA	1,2,3,4
			$\text{trac} = 70 \text{ ns}$		100		
			$\text{trac} = 80 \text{ ns}$		90		
			$\text{trac} = 100 \text{ ns}$		80		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{IL}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.}), I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		90	mA	1, 2, 5
			$\text{trac} = 70 \text{ ns}$		80		
			$\text{trac} = 80 \text{ ns}$		70		
			$\text{trac} = 100 \text{ ns}$		60		
CAS before RAS refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		120	mA	1, 2
			$\text{trac} = 70 \text{ ns}$		100		
			$\text{trac} = 80 \text{ ns}$		90		
			$\text{trac} = 100 \text{ ns}$		80		
CAS before RAS long refresh current (1 024 Cycles / 128 ms)	I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : 1 024 Cycles / 128 ms $\overline{\text{RAS}}, \overline{\text{CAS}}$: $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH}(\text{MAX.})$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ Standby : $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Address : V_{IH} or V_{IL} $\overline{\text{WE}}, \overline{\text{OE}} : V_{IH}$ $I_o = 0 \text{ mA}$	$\text{tr}_{AS} \leq 200 \text{ ns}$		300	μA	1, 2
			$\text{tr}_{AS} \leq 1 \mu\text{s}$		500		
Input leakage current	I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10		+10	μA	
Output leakage current	I _{O(L)}	$V_o = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10		+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4			V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$			0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (trc and tpc).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{IL}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

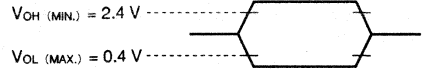
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{RC}	120	—	140	—	160	—	190	—	ns	
RAS Precharge Time	t _{RP}	50	—	60	—	70	—	80	—	ns	
CAS Precharge Time	t _{CPN}	10	—	10	—	10	—	10	—	ns	
RAS Pulse Width	t _{RA}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
CAS Pulse Width	t _{CA}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
RAS Hold Time	t _{RSH}	20	—	20	—	20	—	25	—	ns	
CAS Hold Time	t _{CSH}	60	—	70	—	80	—	100	—	ns	
RAS to CAS Delay Time	t _{RCD}	20	40	20	50	25	60	25	75	ns	1
RAS to Column Address Delay Time	t _{RA}	15	30	15	35	17	40	17	50	ns	1
CAS to RAS Precharge Time	t _{CRP}	10	—	10	—	10	—	10	—	ns	2
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	12	—	12	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	20	—	ns	
OE Lead Time Referenced to RAS	t _{OES}	0	—	0	—	0	—	0	—	ns	
CAS to Data Setup Time	t _{CLZ}	0	—	0	—	0	—	0	—	ns	
OE to Data Setup Time	t _{OLZ}	0	—	0	—	0	—	0	—	ns	
OE to Data Delay Time	t _{OED}	15	—	15	—	20	—	25	—	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
Refresh Time	t _{REF}	—	128	—	128	—	128	—	128	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{RAC} (MAX.)$	$t_{RAC} (MAX.)$
$t_{RAD} > t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{AA} (MAX.)$	$t_{RAD} + t_{AA} (MAX.)$
$t_{RCD} > t_{RCD} (MAX.)$	$t_{CAC} (MAX.)$	$t_{RCD} + t_{CAC} (MAX.)$

$t_{RAD} (MAX.)$ and $t_{RCD} (MAX.)$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD} (MAX.)$ and $t_{RCD} \geq t_{RCD} (MAX.)$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied for $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycle.

Read Cycle

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		$t_{RAC} = 80 \text{ ns}$		$t_{RAC} = 100 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	–	100	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	20	–	20	–	25	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	–	40	–	50	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	20	–	20	–	20	–	25	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	40	–	50	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	3
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	0	25	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi - Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{TRAC} = 60 ns		t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		t _{TRAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	15	–	15	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	15	–	15	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	20	–	20	–	20	–	25	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	15	–	15	–	15	–	20	–	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	–	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	–	0	–	0	–	0	–	ns	
Data-in Setup Time	t _{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in Hold Time	t _{DH}	15	–	15	–	15	–	20	–	ns	3

- Notes**
1. t_{WP(MIN.)} is applied for late write cycles or read modify write cycles. In early write cycles, t_{WCH(MIN.)} should be met.
 2. If t_{WCS} ≥ t_{WCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle.
 3. t_{DS(MIN.)} and t_{DH(MIN.)} are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{TRAC} = 60 ns		t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		t _{TRAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	165	–	185	–	210	–	250	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	80	–	90	–	105	–	130	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	40	–	40	–	45	–	55	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	50	–	55	–	65	–	80	–	ns	1

- Notes**
1. If t_{WCS} ≥ t_{WCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If t_{trwd} ≥ t_{trwd(MIN.)}, t_{tcwd} ≥ t_{tcwd(MIN.)}, t_{tawd} ≥ t_{tawd(MIN.)}, and t_{cpwd} ≥ t_{cpwd(MIN.)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	40	–	45	–	50	–	60	–	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	–	35	–	40	–	45	–	55	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35	–	40	–	45	–	55	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	85	–	90	–	100	–	120	–	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	55	–	60	–	70	–	85	–	ns	1

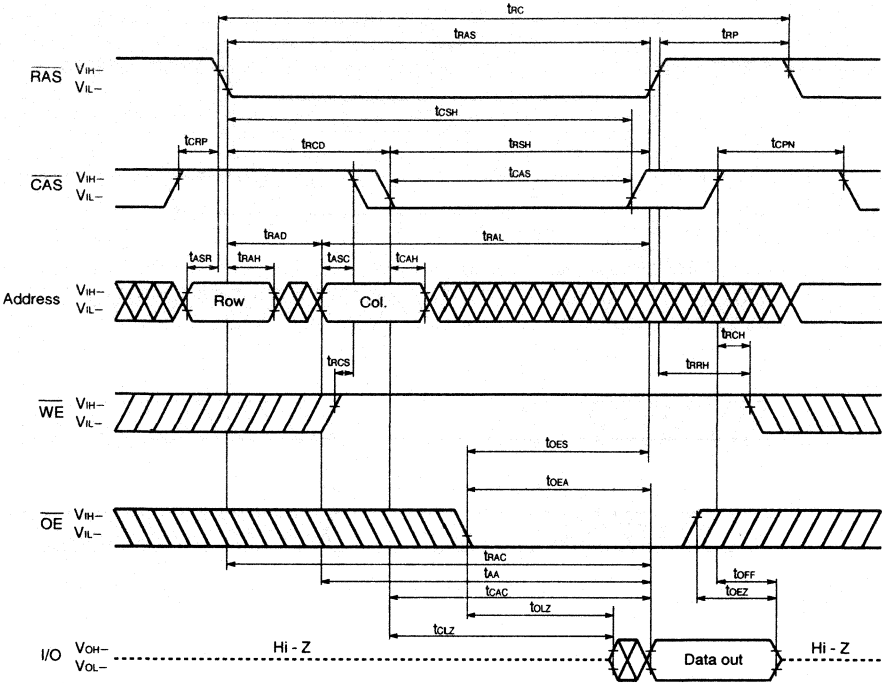
★

Notes 1. If $\text{twcs} \geq \text{twcs}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $\text{trwd} \geq \text{trwd}(\text{MIN.})$, $\text{tcwd} \geq \text{tcwd}(\text{MIN.})$, $\text{tawd} \geq \text{tawd}(\text{MIN.})$, and $\text{tcpwd} \geq \text{tcpwd}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

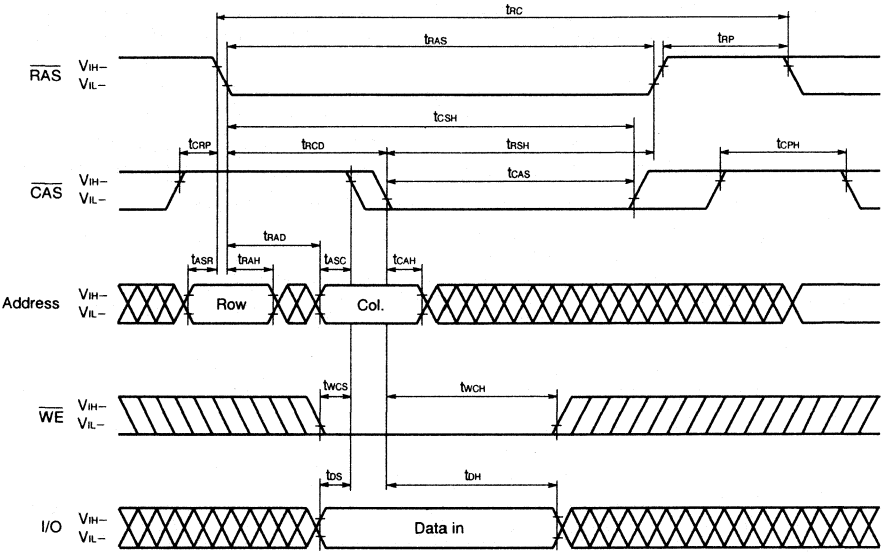
Refresh Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ Setup Time	t _{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	15	–	15	–	15	–	20	–	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15	–	15	–	15	–	20	–	ns	

Read Cycle

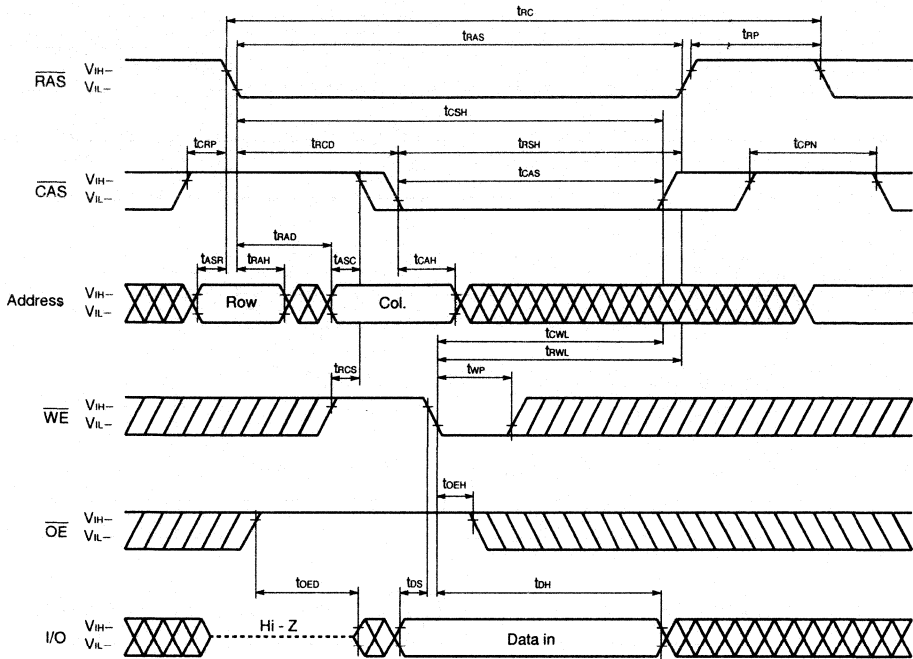


Early Write Cycle

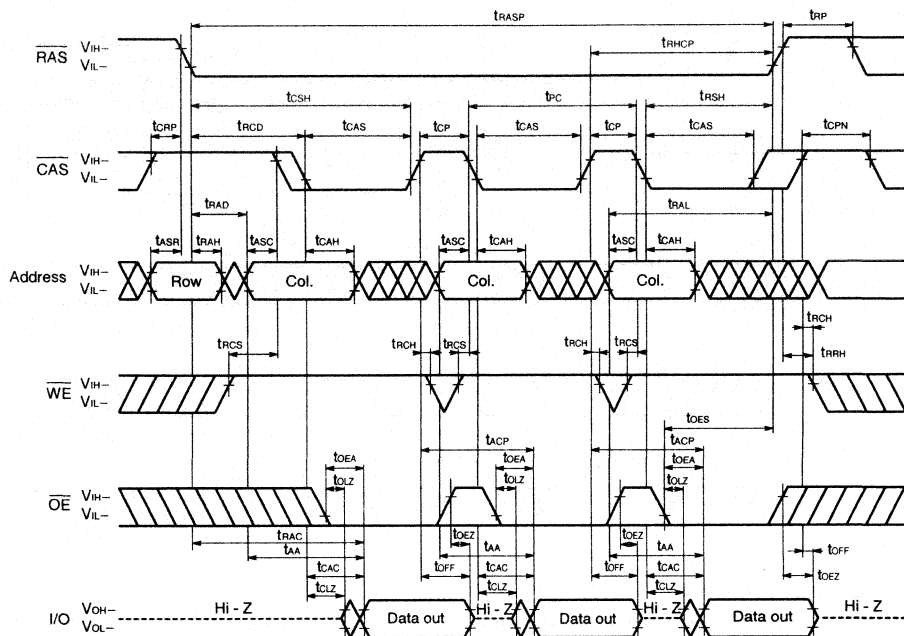


Remark $\overline{\text{OE}}$: Don't care

Late Write Cycle

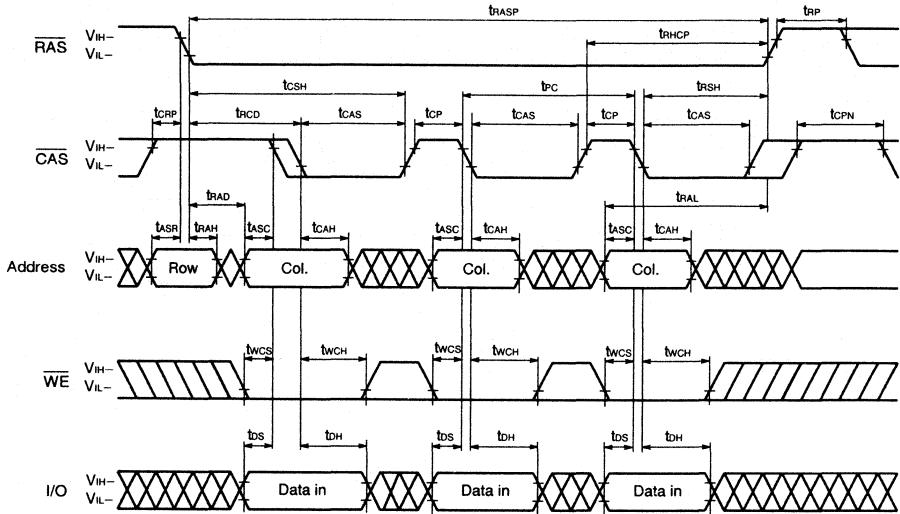


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



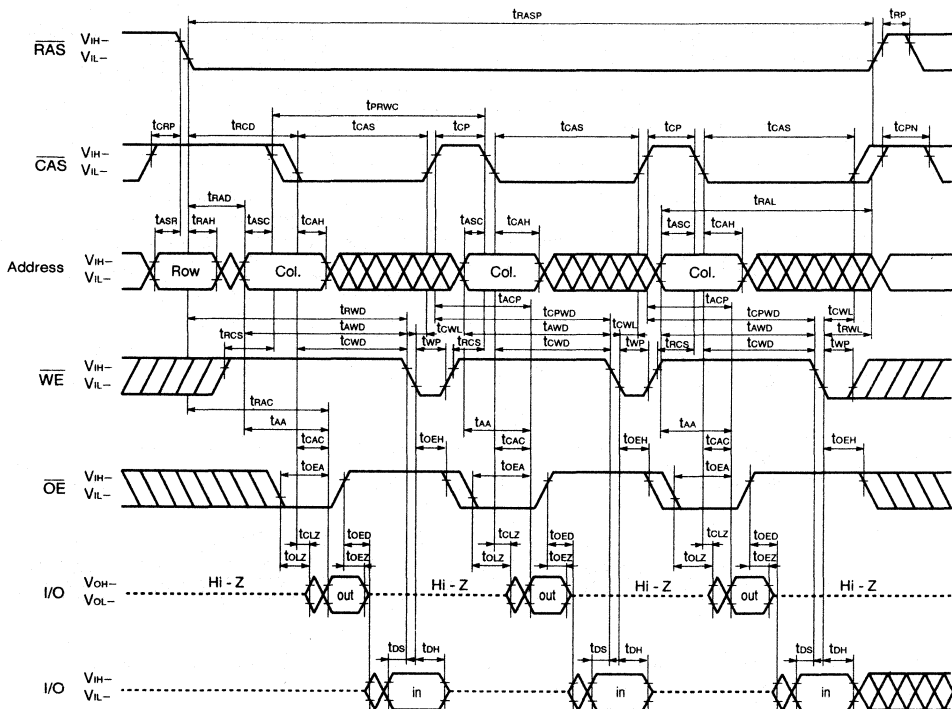
Remark $\overline{OE}$: Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

[illegible]

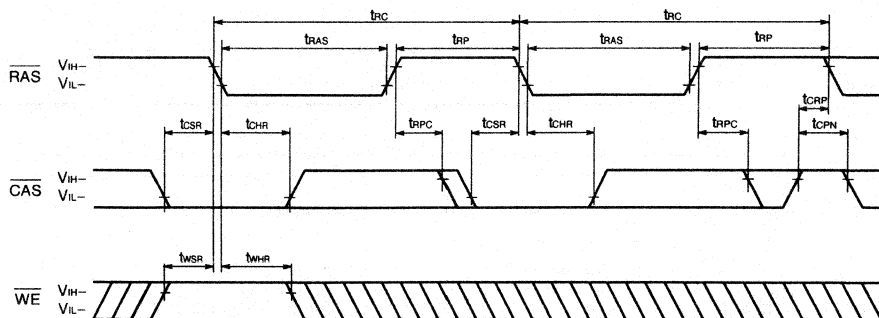
547

★ **Fast Page Mode Read Modify Write Cycle**



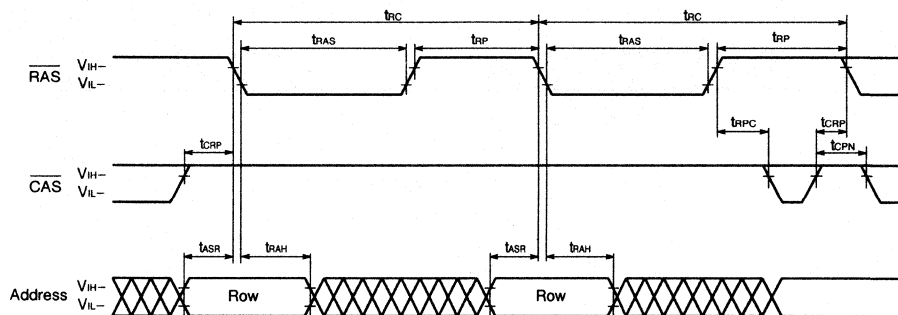
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



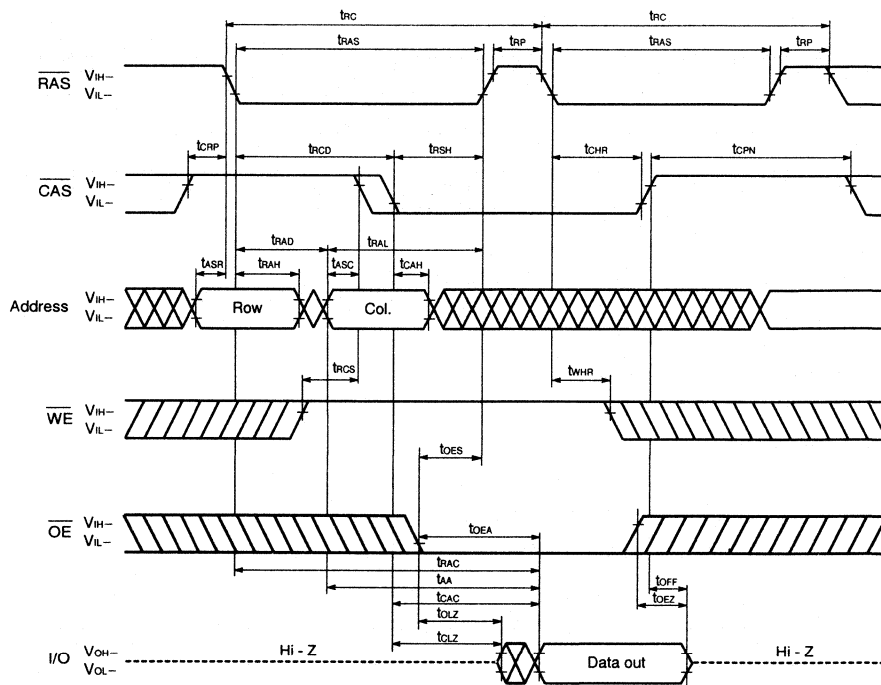
Remark Address, $\overline{OE}$: Don't care I/O : Hi - Z

RAS Only Refresh Cycle

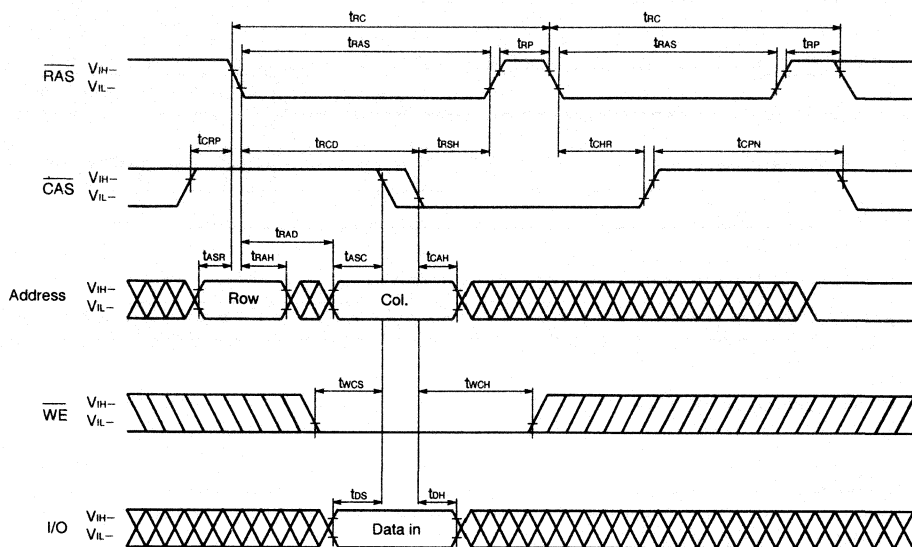


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi - Z

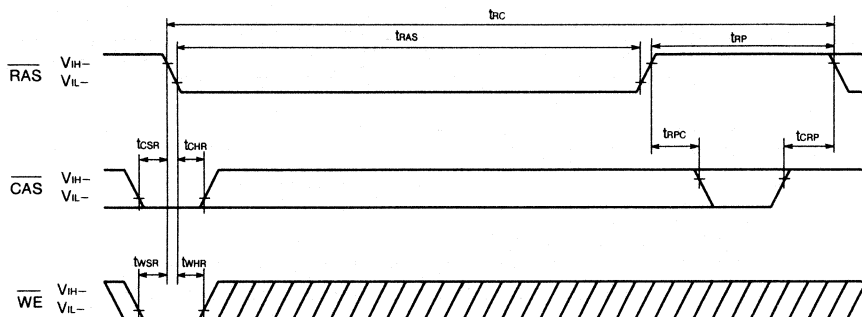
★ Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)

Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 8$ -bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 8 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output="1": Normal write (all memory cells)

Output="0": Abnormal write

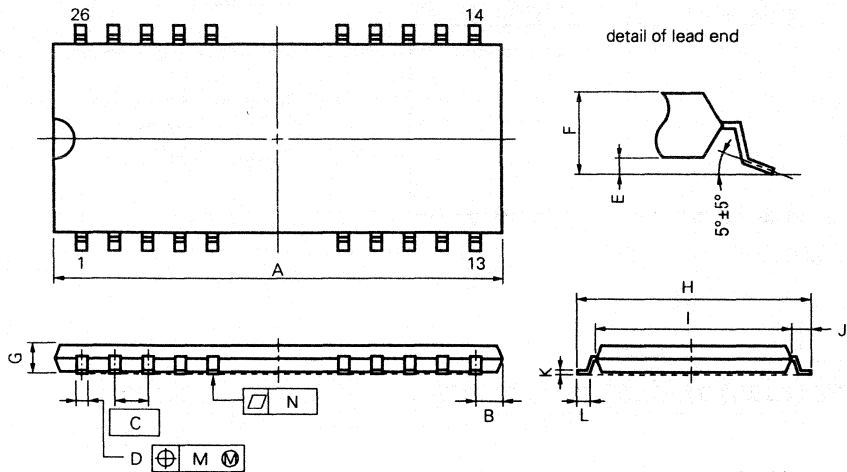
(3) Refresh

Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

Package Drawings
26 PIN PLASTIC TSOP(III) (300 mil)



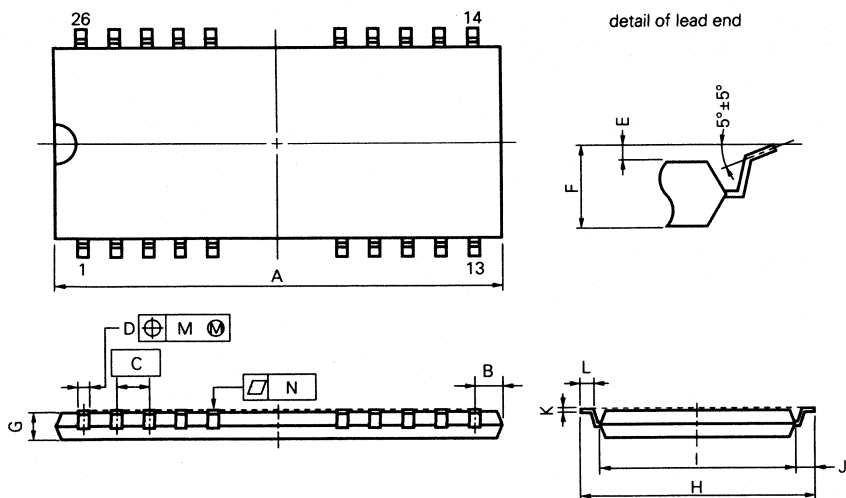
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S26GS-50-9JD-2

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0.691 MAX.
B	1.18 MAX.	0.047 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.13 MAX.	0.045 MAX.
G	1.0	0.039
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

26 PIN PLASTIC TSOP(III) (300 mil)



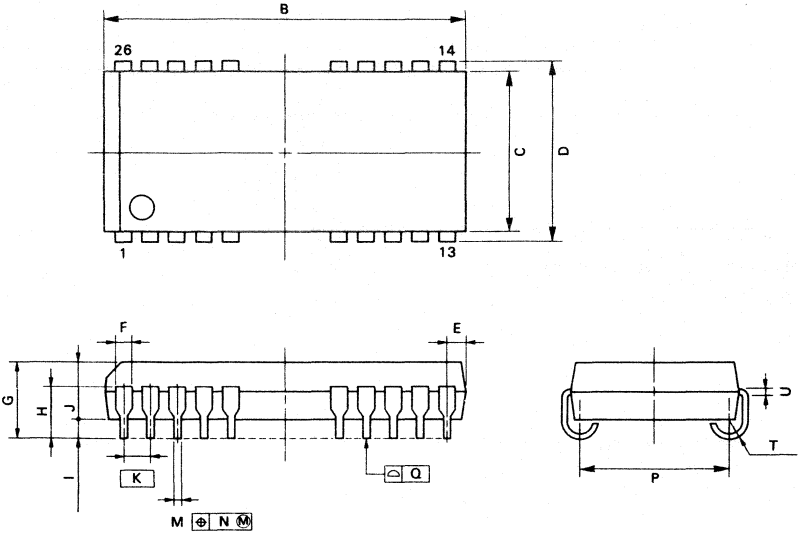
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S26GS-50-9KD-2

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0.691 MAX.
B	1.18 MAX.	0.047 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.13 MAX.	0.045 MAX.
G	1.0	0.039
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

26PIN PLASTIC SOJ (300 mil)

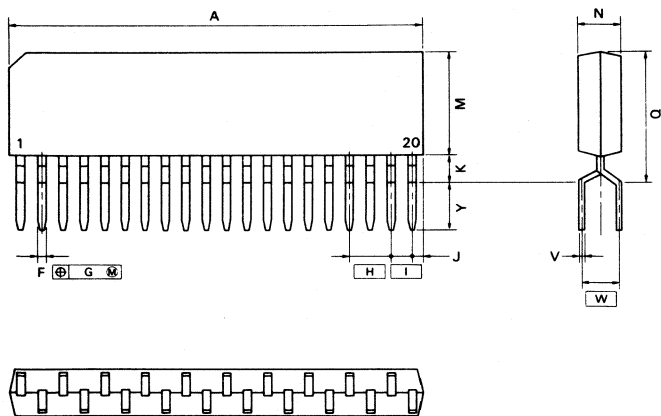


NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LA-50A-1

ITEM	MILLIMETERS	INCHES
B	17.4 ^{+0.2} _{-0.35}	0.685 ^{+0.008} _{-0.013}
C	7.57	0.298
D	8.47 ^{+0.2}	0.333 ^{+0.009} _{-0.008}
E	1.08 ^{+0.15}	0.043 ^{+0.006} _{-0.007}
F	0.6	0.024
G	3.5 ^{+0.2}	0.138 ^{+0.008}
H	2.4 ^{+0.2}	0.094 ^{+0.008} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40 ^{+0.10}	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73 ^{+0.20}	0.265 ^{+0.008}
Q	0.15	0.006
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.08}	0.008 ^{+0.004} _{-0.002}

20PIN PLASTIC ZIP (400 mil)



NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P20V-254-400A-1

ITEM	MILLIMETERS	INCHES
A	26.67 MAX.	1.050 MAX.
F	$0.5^{+0.1}$	$0.020^{+0.004}_{-0.002}$
G	$\phi 0.25$	$\phi 0.010$
H	2.54	0.100
I	1.27	0.050
J	1.27 MAX.	0.050 MAX.
K	1.0 MIN.	0.039 MIN.
M	8.9 MAX.	0.350 MAX.
N	$2.8^{+0.2}$	$0.110^{+0.008}_{-0.004}$
Q	10.16 MAX.	0.400 MAX.
V	$0.25^{+0.10}_{-0.08}$	$0.010^{+0.004}_{-0.003}$
W	2.54	0.100
Y	$3.3^{+0.5}$	$0.130^{+0.020}_{-0.010}$

Recommended Soldering Conditions



The following conditions (see tables below and next page) must be met for soldering conditions of the μPD424400-L. For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD424400GS : 26-pin plastic TSOP(II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD424400LA : 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit^{Note}: 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit^{Note}: 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

Type of Through Hole Mount Device

μPD424400V : 20-pin plastic ZIP (400 mil)

Soldering process	Soldering conditions
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below
Partial heating method	Terminal temperature : 260 °C or below, Time : 10 seconds or below

Caution Do not jet molten solder on the surface of package.

MOS INTEGRATED CIRCUIT

μ PD42S4800, 424800

4 M-BIT DYNAMIC RAM

512 K-WORD BY 8-BIT, FAST PAGE MODE

Description

The μ PD42S4800, 424800 are 524 288 words by 8 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

Besides, the μ PD42S4800 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

These devices are packed in 28-pin plastic TSOP(II), 28-pin plastic SOJ and 28-pin plastic ZIP.

Features

- 524 288 words by 8 bits organization
- Single +5.0 V $\pm$ 10 % power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S4800-70, 424800-70	577.5 mW	70 ns	140 ns	45 ns
μ PD42S4800-80, 424800-80	522.5 mW	80 ns	150 ns	50 ns
μ PD42S4800-10, 424800-10	440.0 mW	100 ns	180 ns	60 ns

- The μ PD42S4800 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S4800	1 024 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	0.825 mW (CMOS level input)
μ PD424800	1 024 cycles/16 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

- Multiplexed address inputs ... Row address : A0 to A9, Column address : A0 to A8

The information in this document is subject to change without notice.

The mark ★ shows revised points.

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD42S4800G5-70-7JD	70 ns	28-pin Plastic TSOP (II) (400 mil)	CAS before RAS self refresh CAS before RAS refresh RAS only refresh Hidden refresh
μ PD42S4800G5-80-7JD	80 ns		
μ PD42S4800G5-10-7JD	100 ns		
μPD42S4800G5-70-7KD	70 ns	28-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD42S4800G5-80-7KD	80 ns		
μPD42S4800G5-10-7KD	100 ns		
μ PD42S4800LE-70	70 ns	28-pin Plastic SOJ (400 mil)	
μ PD42S4800LE-80	80 ns		
μ PD42S4800LE-10	100 ns		
μPD42S4800V-70	70 ns	28-pin Plastic ZIP (400 mil)	
μPD42S4800V-80	80 ns		
μPD42S4800V-10	100 ns		
μ PD424800G5-70-7JD	70 ns	28-pin Plastic TSOP (II) (400 mil)	CAS before RAS refresh RAS only refresh Hidden refresh
μ PD424800G5-80-7JD	80 ns		
μ PD424800G5-10-7JD	100 ns		
μPD424800G5-70-7KD	70 ns	28-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD424800G5-80-7KD	80 ns		
μPD424800G5-10-7KD	100 ns		
μ PD424800LE-70	70 ns	28-pin Plastic SOJ (400 mil)	
μ PD424800LE-80	80 ns		
μ PD424800LE-10	100 ns		
μPD424800V-70	70 ns	28-pin Plastic ZIP (400 mil)	
μPD424800V-80	80 ns		
μPD424800V-10	100 ns		

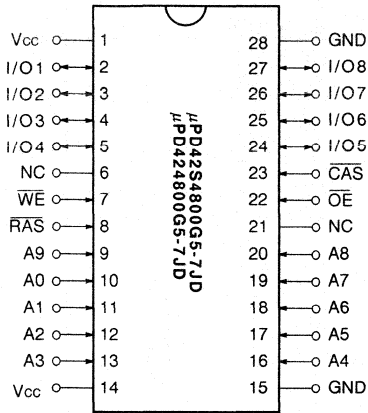
Quality Grade

Standard

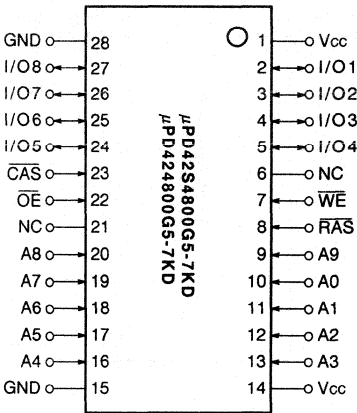
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number I EI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking side)

28-pin Plastic TSOP(II)
(400 mil)

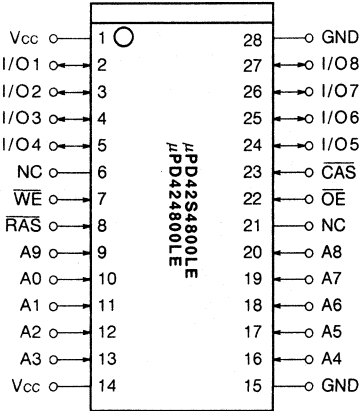


Reverse bent



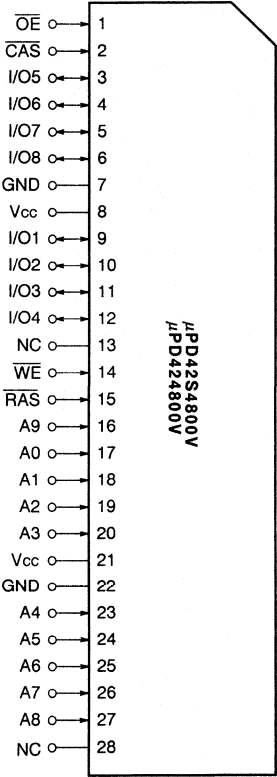
- A0 to A9 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

28-pin Plastic SOJ
(400 mil)

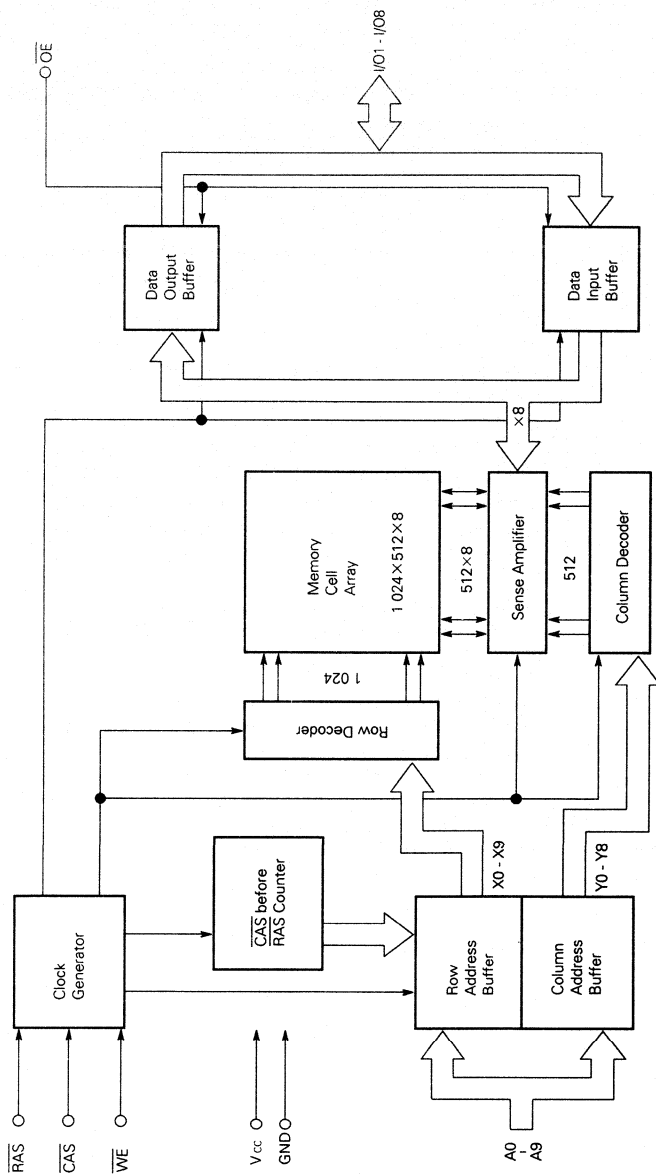


- A0 to A9 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

28-pin Plastic ZIP
(400 mil)



Block Diagram



Input/Output Pin Functions

The μPD42S4800, 424800 have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A9 and input/output pins I/O1 to I/O8.

Pin Name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address inputs)		Address bus. Input total 19-bit of address signal, upper 10-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 524 288-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/ Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

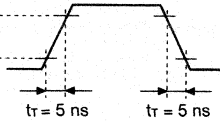
DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	RAS, CAS Cycling			105	mA	1, 2, 3
			trc = trc(MIN.)			95		
			Io = 0 mA			80		
Standby current	μPD42S4800	I _{CC2}	RAS, CAS ≥ V _{IH} (MIN.), Io = 0 mA			2	mA	
			RAS, CAS ≥ V _{CC} - 0.2 V, Io = 0 mA			0.15		
	μPD424800		RAS, CAS ≥ V _{IH} (MIN.), Io = 0 mA			2		
			RAS, CAS ≥ V _{CC} - 0.2 V, Io = 0 mA			1		
RAS only refresh current		I _{CC3}	RAS Cycling, CAS ≥ V _{IH} (MIN.)			105	mA	1,2,3,4
			trc = trc(MIN.), Io = 0 mA			95		
						80		
Operating current (Fast page mode)		I _{CC4}	RAS ≤ V _{IL} (MAX.), CAS Cycling			80	mA	1, 2, 5
			tpc = tpc(MIN.), Io = 0 mA			70		
						60		
CAS before RAS refresh current		I _{CC5}	RAS Cycling			105	mA	1, 2
			trc = trc(MIN.)			95		
			Io = 0 mA			80		
CAS before RAS long refresh current (1 024 Cycles / 128 ms, only for the μPD42S4800)		I _{CC6}	CAS before RAS refresh : 1 024 Cycles / 128 ms			200	μA	1, 2
			RAS, CAS : V _{CC} -0.2 V ≤ V _{IH} ≤ V _{IH} (MAX.) 0 V ≤ V _{IL} ≤ 0.2 V					
			Standby : RAS, CAS ≥ V _{CC} -0.2 V Address : V _{IH} or V _{IL} WE, OE : V _{IH} Io = 0 mA			300		
Self refresh current (CAS before RAS self refresh, only for the μPD42S4800)		I _{CC7}	RAS, CAS : V _{CC} -0.2 V ≤ V _{IH} ≤ V _{IH} (MAX.) 0 V ≤ V _{IL} ≤ 0.2 V Io = 0 mA			150	μA	2
Input leakage current		I _{I(L)}	Vi = 0 to 5.5 V All other pins not under test = 0 V	-10		+10	μA	
Output leakage current		I _{O(L)}	Vo = 0 to 5.5 V Output is disabled (Hi-Z)	-10		+10	μA	
High level output voltage		VOH	Io = -5.0 mA	2.4			V	
Low level output voltage		VOL	Io = +4.2 mA			0.4	V	

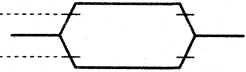
- Notes**
- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (trc and tpc).
 - Specified values are obtained with outputs unloaded.
 - I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during RAS ≤ V_{IL}(MAX.) and CAS ≥ V_{IH}(MIN.).
 - I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 - I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)**AC Characteristics Test Conditions**

(1) Input timing specification

 $V_{IH} \text{ (MIN.)} = 2.4 \text{ V}$ $V_{IL} \text{ (MAX.)} = 0.8 \text{ V}$ 

(2) Output timing specification

 $V_{OH} \text{ (MIN.)} = 2.4 \text{ V}$ $V_{OL} \text{ (MAX.)} = 0.4 \text{ V}$ 

(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 70 ns		tRAC = 80 ns		tRAC = 100 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		tRC	140	–	150	–	180	–	ns	
RAS Precharge Time		tRP	60	–	60	–	70	–	ns	
CAS Precharge Time		tCPN	10	–	10	–	10	–	ns	
RAS Pulse Width		tRAS	70	10 000	80	10 000	100	10 000	ns	
CAS Pulse Width		tCAS	20	10 000	20	10 000	25	10 000	ns	
RAS Hold Time		tRSH	20	–	20	–	25	–	ns	
CAS Hold Time		tCSH	70	–	80	–	100	–	ns	
RAS to $\overline{\text{CAS}}$ Delay Time		tRCD	20	50	25	60	25	75	ns	1
RAS to Column Address Delay Time		tRAD	15	35	17	40	17	50	ns	1
CAS to $\overline{\text{RAS}}$ Precharge Time		tCRP	5	–	5	–	5	–	ns	2
Row Address Setup Time		tASR	0	–	0	–	0	–	ns	
Row Address Hold Time		tRAH	10	–	12	–	12	–	ns	
Column Address Setup Time		tASC	0	–	0	–	0	–	ns	
Column Address Hold Time		tCAH	15	–	15	–	20	–	ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$		tOES	0	–	0	–	0	–	ns	
CAS to Data Setup Time		tCLZ	0	–	0	–	0	–	ns	
$\overline{\text{OE}}$ to Data Setup Time		tOLZ	0	–	0	–	0	–	ns	
$\overline{\text{OE}}$ to Data Delay Time		tOED	15	–	15	–	20	–	ns	
Transition Time (Rise and Fall)		tT	3	50	3	50	3	50	ns	
Refresh Time	$\mu\text{PD42S4800}$	tREF	–	128	–	128	–	128	ms	3
	$\mu\text{PD424800}$		–	16	–	16	–	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD} \text{ (MAX.)}$ and $t_{RCD} \leq t_{RCD} \text{ (MAX.)}$	$t_{RAC} \text{ (MAX.)}$	$t_{RAC} \text{ (MAX.)}$
$t_{RAD} > t_{RAD} \text{ (MAX.)}$ and $t_{RCD} \leq t_{RCD} \text{ (MAX.)}$	$t_{AA} \text{ (MAX.)}$	$t_{RAD} + t_{AA} \text{ (MAX.)}$
$t_{RCD} > t_{RCD} \text{ (MAX.)}$	$t_{CAC} \text{ (MAX.)}$	$t_{RCD} + t_{CAC} \text{ (MAX.)}$

$t_{RAD} \text{ (MAX.)}$ and $t_{RCD} \text{ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD} \text{ (MAX.)}$ and $t_{RCD} \geq t_{RCD} \text{ (MAX.)}$ will not cause any operation problems.

- 2. $t_{CRP(MIN.)}$ requirement is applied for $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycle.
- 3. This specification is applied only for the μPD42S4800.

Read Cycle

Parameter	Symbol	$t_{RAC} = 70\text{ ns}$		$t_{RAC} = 80\text{ ns}$		$t_{RAC} = 100\text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	70	–	80	–	100	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	20	–	20	–	25	ns	1
Access Time from Column Address	t_{AA}	–	35	–	40	–	50	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	20	–	20	–	25	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	35	–	40	–	50	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	3
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$ will not cause any operation problems.

- 2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
- 3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi - Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		t _{TRAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twCH	10	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Pulse Width	tWP	10	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trWL	20	–	20	–	25	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcWL	15	–	15	–	20	–	ns	
$\overline{\text{WE}}$ Setup Time	twCS	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toEH	0	–	0	–	0	–	ns	
Data-in Setup Time	tDS	0	–	0	–	0	–	ns	3
Data-in Hold Time	tDH	15	–	15	–	20	–	ns	3

- Notes**
1. tWP(MIN.) is applied for late write cycles or read modify write cycles. In early write cycles, twCH(MIN.) should be met.
 2. If twCS $\geq$ twCS(MIN.), the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle.
 3. tDS(MIN.) and tDH(MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		t _{TRAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trWC	185	–	200	–	240	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trWD	90	–	105	–	130	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcWD	40	–	45	–	55	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tAWD	55	–	65	–	80	–	ns	1

- Note**
1. If twCS $\geq$ twCS(MIN.), the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If trWD $\geq$ trWD(MIN.), tcWD $\geq$ tcWD(MIN.), tAWD $\geq$ tAWD(MIN.), and tCPWD $\geq$ tCPWD(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.



Fast Page Mode

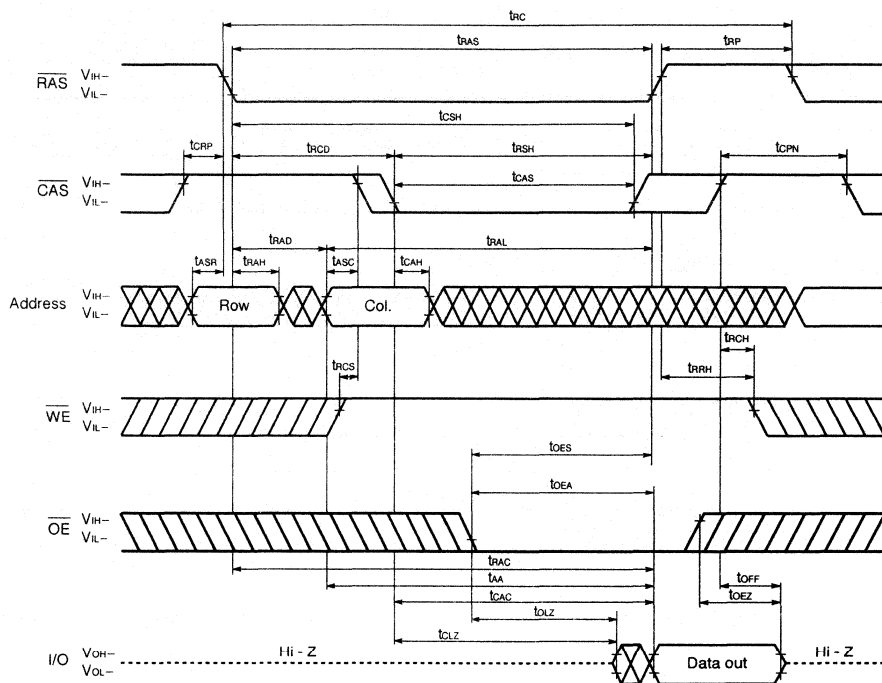
Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	45	–	50	–	60	–	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	–	40	–	45	–	55	ns	
RAS Pulse Width	t _{RASP}	70	125 000	80	125 000	100	125 000	ns	
CAS Precharge Time	t _{CP}	10	–	10	–	10	–	ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40	–	45	–	55	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	90	–	100	–	120	–	ns	
CAS Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	60	–	70	–	85	–	ns	1

Note 1. If $\text{twCS} \geq \text{twCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $\text{trWD} \geq \text{trWD(MIN.)}$, $\text{tcWD} \geq \text{tcWD(MIN.)}$, $\text{tawD} \geq \text{tawD(MIN.)}$, and $\text{tcpWD} \geq \text{tcpWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

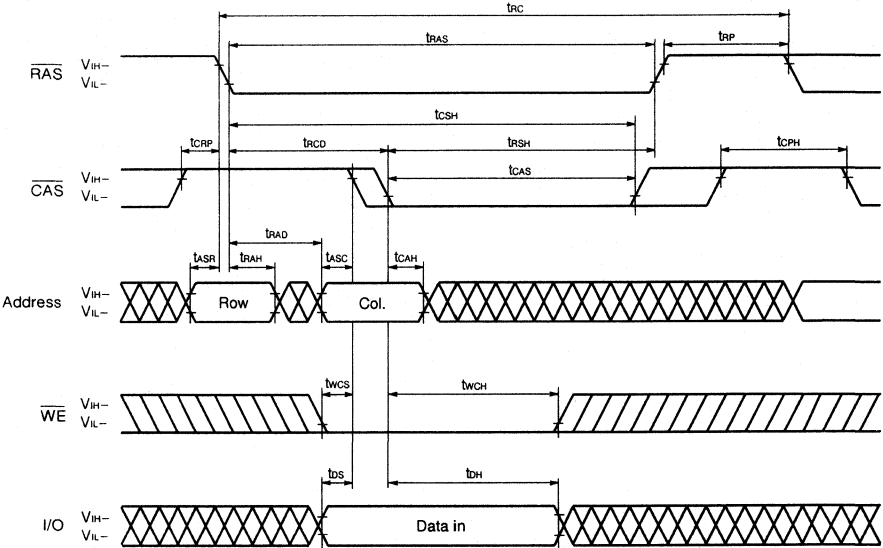
Refresh Cycle

Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ Setup Time	t _{CSR}	5	–	5	–	5	–	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RASS}	100	–	100	–	100	–	μs	1
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{RPS}	130	–	150	–	180	–	ns	1
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15	–	15	–	20	–	ns	

Note 1. This specification is applied only for the μPD42S4800.

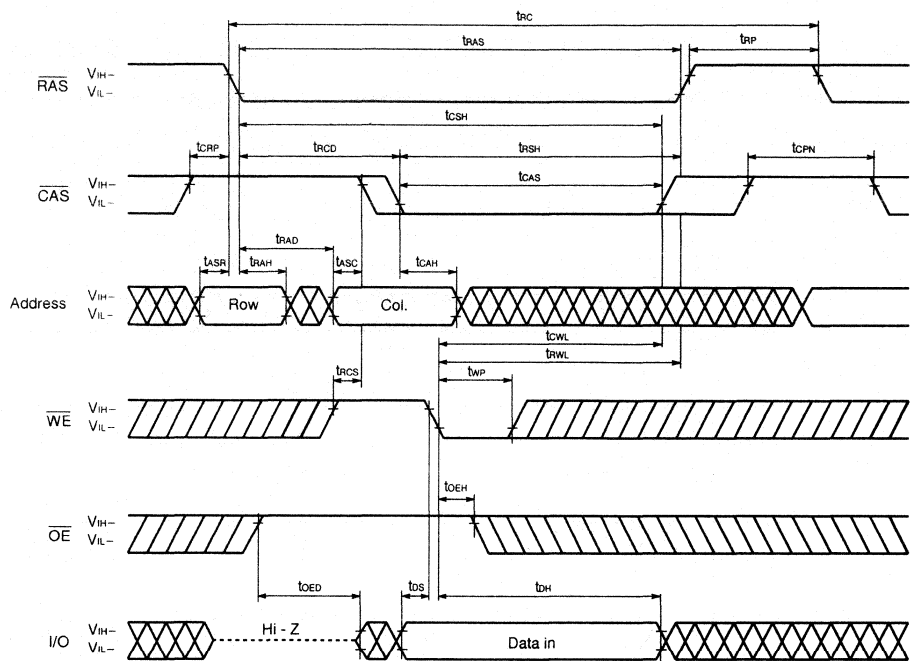


Early Write Cycle

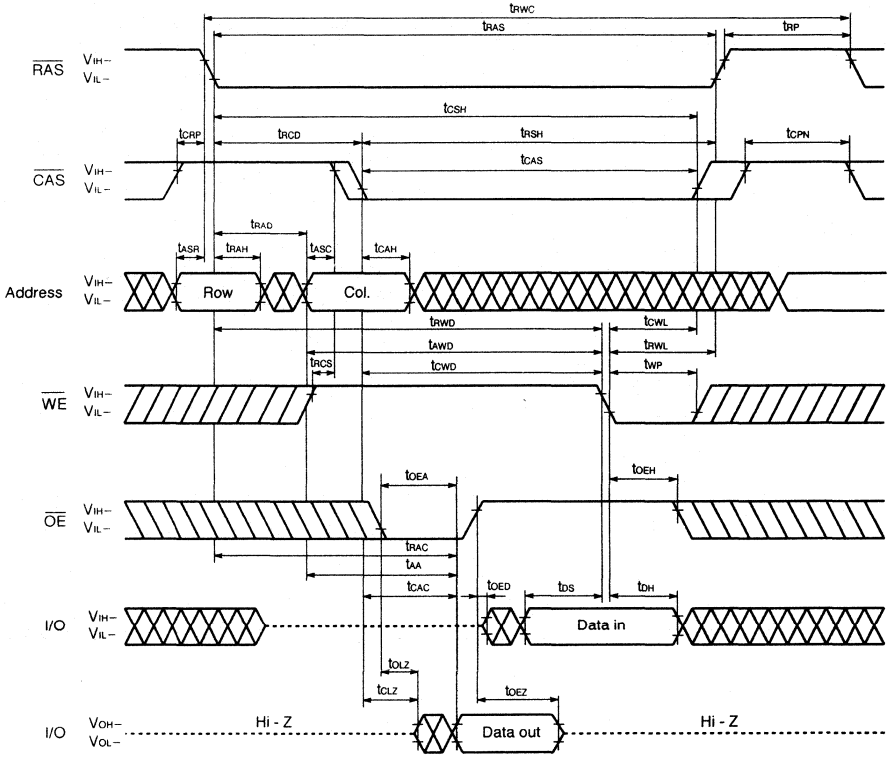


Remark $\overline{\text{OE}}$: Don't care

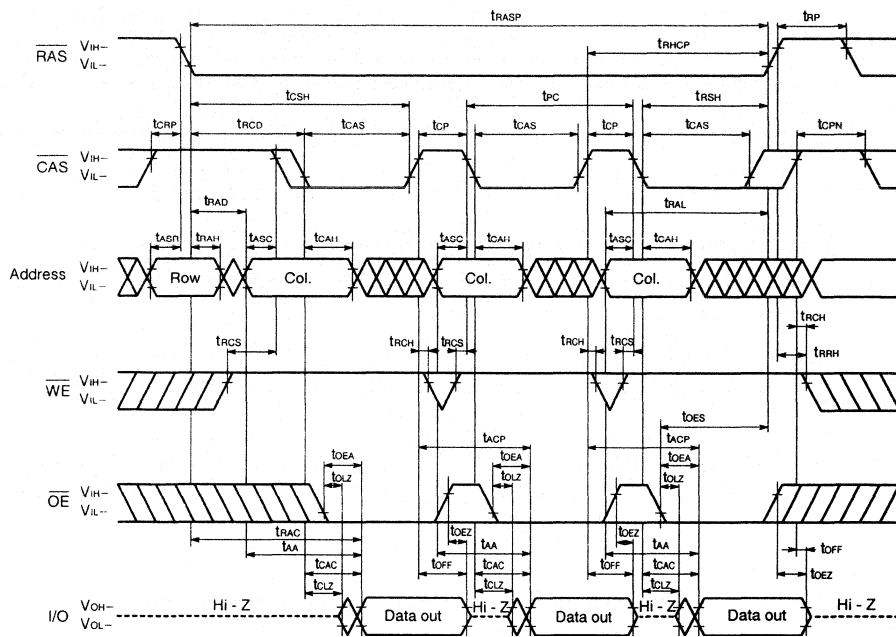
Late Write Cycle



★ Read Modify Write Cycle

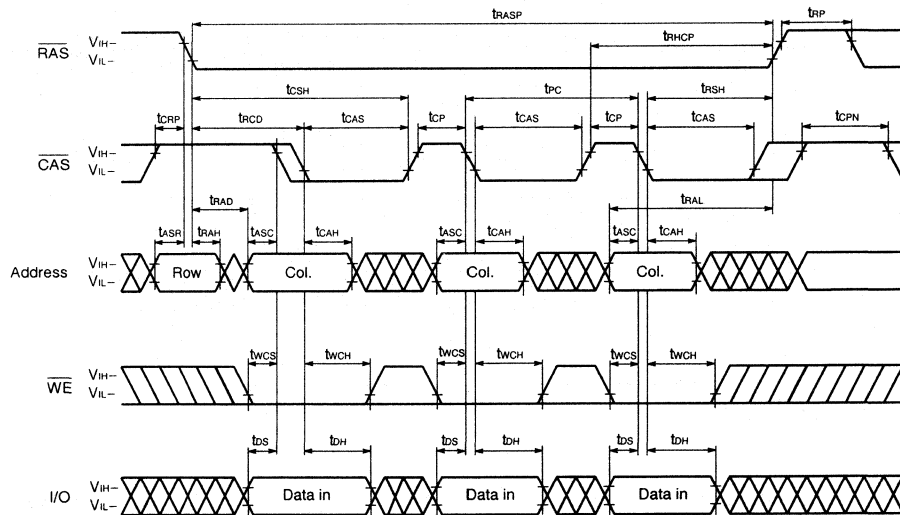


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

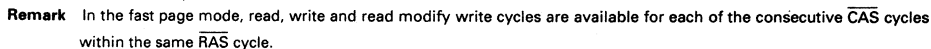
Fast Page Mode Early Write Cycle



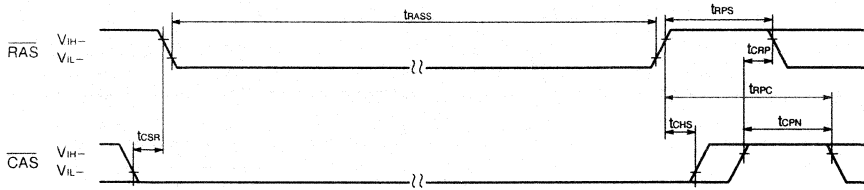
Remark $\overline{OE}$: Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

★



CAS Before RAS Self Refresh Cycle (Only for the μPD42S4800)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh



CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

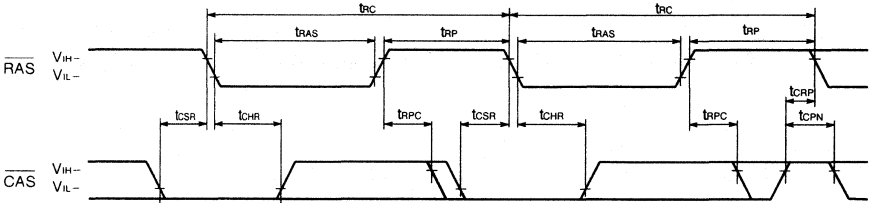
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 1 024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh 1 024 times within an interval of 16 ms or less just before and after setting CAS before RAS self refresh.

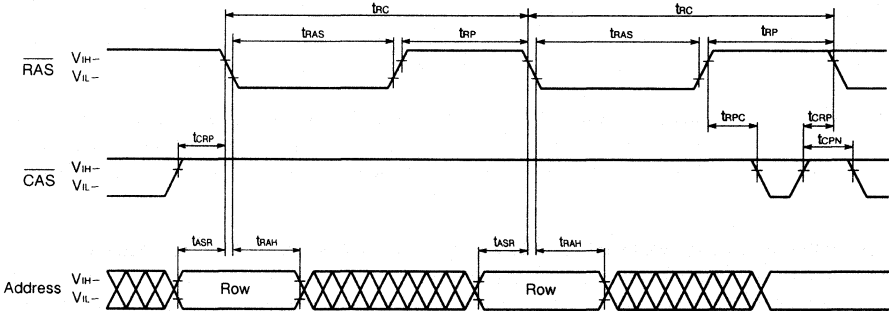
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



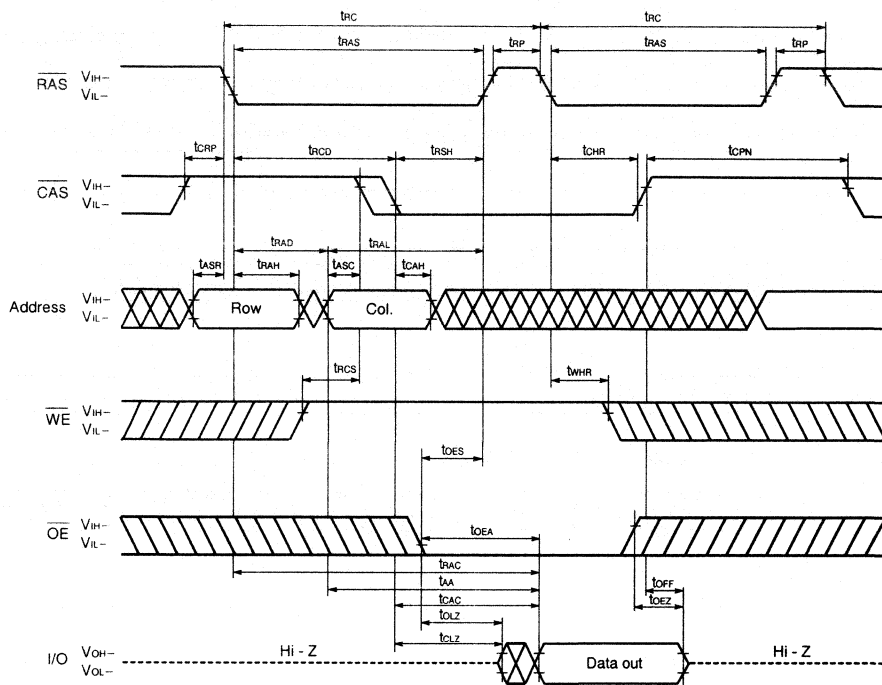
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi - Z

RAS Only Refresh Cycle

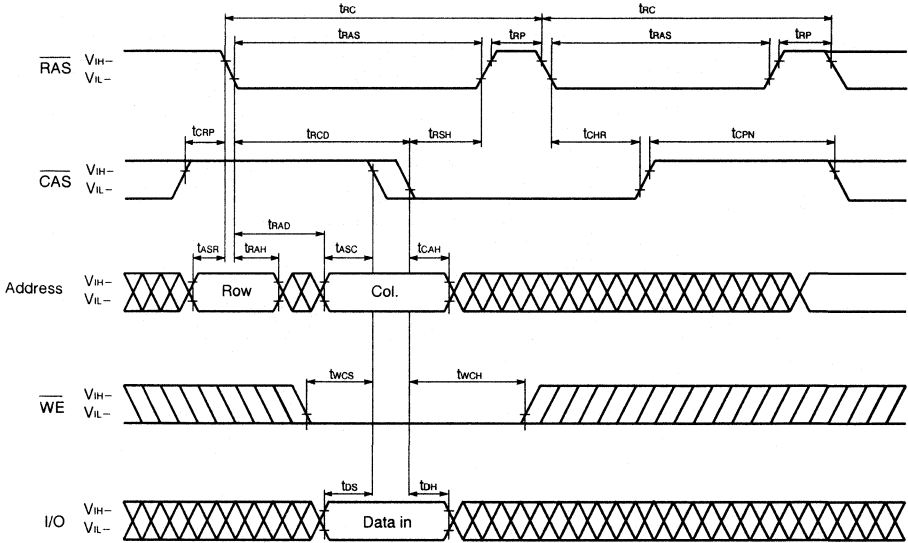


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi - Z

★



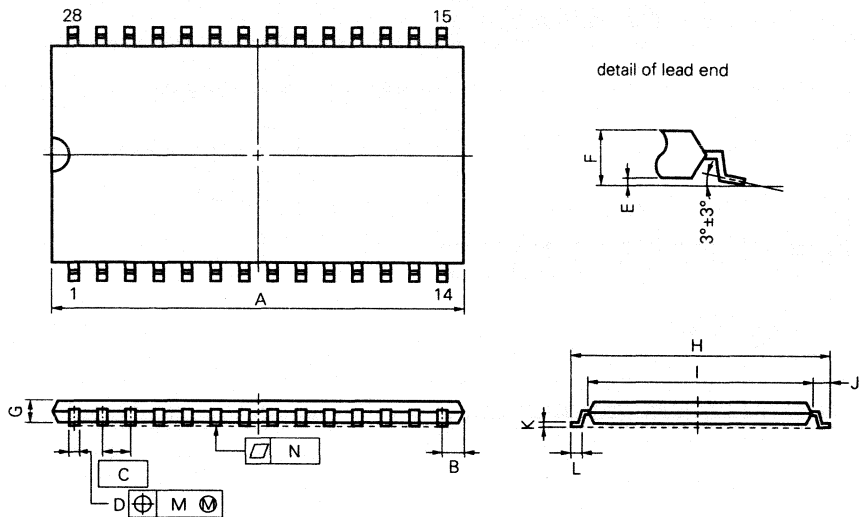
★ Hidden Refresh Cycle (Write)



Remark OE : Don't care

Package Drawings

28 PIN PLASTIC TSOP(III) (400 mil)



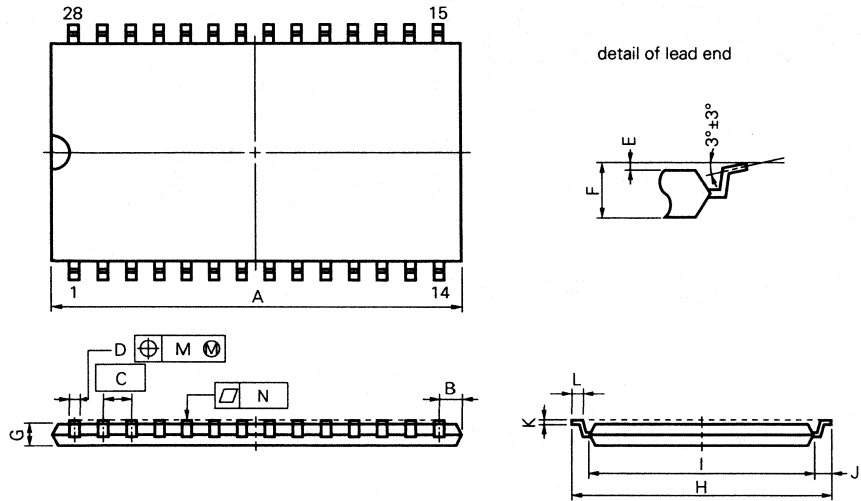
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD-2

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP(III) (400 mil)



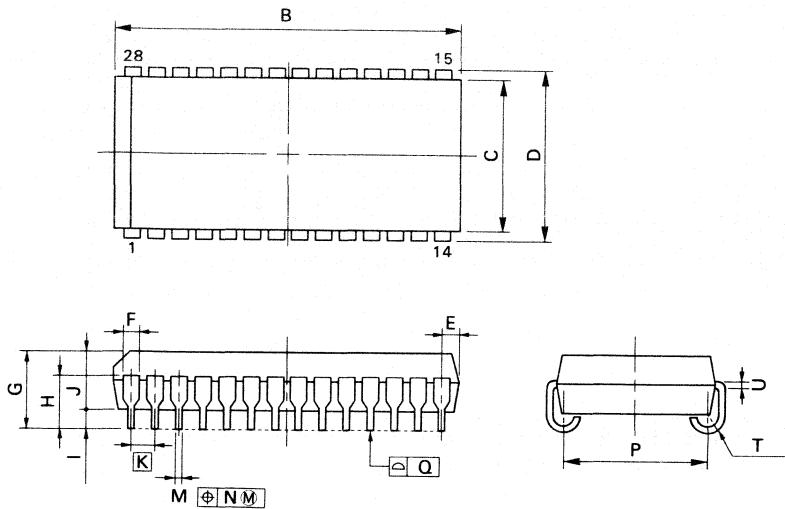
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7KD-2

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28PIN PLASTIC SOJ (400 mil)

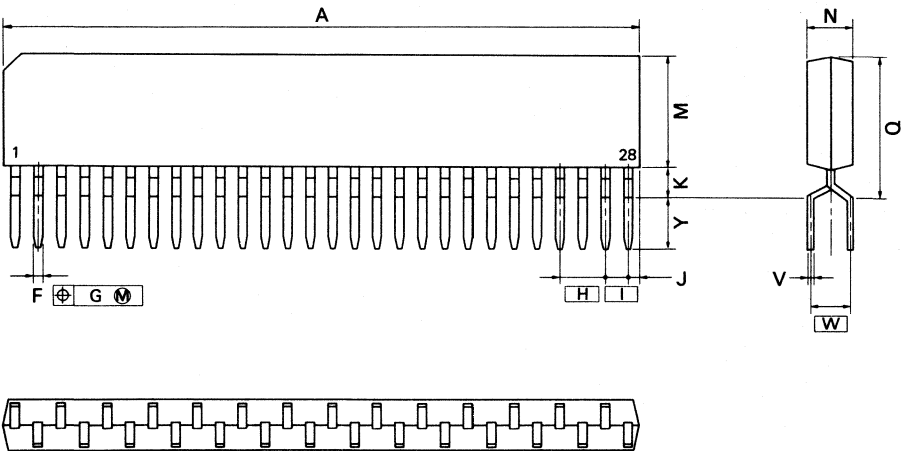


NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LA-400A-1

ITEM	MILLIMETERS	INCHES
B	18.67 ^{+0.2} _{-0.35}	0.735 ^{+0.008} _{-0.013}
C	10.16	0.400
D	11.18 ^{+0.2}	0.440 ^{+0.008} _{-0.009}
E	1.08 ^{+0.15}	0.043 ^{+0.006} _{-0.009}
F	0.6	0.024
G	3.5 ^{+0.2}	0.138 ^{+0.008} _{-0.009}
H	2.4 ^{+0.2}	0.094 ^{+0.008} _{-0.009}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40 ^{+0.10}	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.40 ^{+0.20}	0.370 ^{+0.008} _{-0.009}
Q	0.15	0.006
T	R0.85	R0.033
U	0.20 ^{+0.10} _{-0.08}	0.008 ^{+0.004} _{-0.005}

28PIN PLASTIC ZIP (400mil)



P28V-254-400A

NOTE
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	36.83 MAX.	1.450 MAX.
F	0.5 ^{±0.1}	0.020 ^{+0.004} _{-0.008}
G	φ0.25	φ0.010
H	2.54	0.100
I	1.27	0.050
J	1.27 MAX.	0.050 MAX.
K	1.0 MIN.	0.039 MIN.
M	8.9 MAX.	0.350 MAX.
N	2.8 ^{±0.2}	0.110 ^{+0.008} _{-0.008}
Q	10.16 MAX.	0.400 MAX.
V	0.25 ^{+0.10} _{-0.08}	0.010 ^{+0.004} _{-0.003}
W	2.54	0.100
Y	3.3 ^{±0.5}	0.130 ^{±0.02}

Recommended Soldering Conditions



The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S4800, 424800.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S4800G5, 424800G5 : 28-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S4800LE, 424800LE : 28-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit^{Note)}: 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit^{Note)}: 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

Type of Through Hole Mount Device

μPD42S4800V, 424800V : 28-pin plastic ZIP (400 mil)

Soldering process	Soldering conditions
Wave soldering	Solder temperature : 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Terminal temperature : 260 °C or below, Time : 10 seconds or below

Caution Do not jet molten solder on the surface of package.

MOS INTEGRATED CIRCUIT

μ PD42S4805A, 424805A

4 M-BIT DYNAMIC RAM

512 K-WORD BY 8-BIT, HYPER PAGE MODE

Description

The μ PD42S4805A, 424805A are 524 288 words by 8 bits dynamic CMOS RAMs with optional hyper page mode.

Hyper page mode is a kind of page mode and is useful for the read operation.

The μ PD42S4805A, 424805A are packed in 28-pin plastic TSOP(II) and 28-pin plastic SOJ.

Features

- Hyper page mode
- 524 288 words by 8 bits organization
- Single +5.0 V $\pm$ 10 % power supply

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μ PD42S4805A-50, 424805A-50	50 ns	84 ns	20 ns
μ PD42S4805A-60, 424805A-60	60 ns	104 ns	25 ns
μ PD42S4805A-70, 424805A-70	70 ns	124 ns	30 ns

- μ PD42S4805A can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh
μ PD42S4805A	1 024 cycles / 128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD424805A	1 024 cycles / 16 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh

The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD42S4805AG5-50-7JD	50 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S4805AG5-60-7JD	60 ns		
μ PD42S4805AG5-70-7JD	70 ns		
μPD42S4805AG5-50-7KD	50 ns	28-pin Plastic TSOP (II) (400 mil)	
μPD42S4805AG5-60-7KD	60 ns	Reverse bent	
μPD42S4805AG5-70-7KD	70 ns	Reverse bent	
μ PD42S4805ALE-50	50 ns	28-pin Plastic SOJ (400 mil)	
μ PD42S4805ALE-60	60 ns		
μ PD42S4805ALE-70	70 ns		
μ PD424805AG5-50-7JD	50 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD424805AG5-60-7JD	60 ns		
μ PD424805AG5-70-7JD	70 ns		
μPD424805AG5-50-7KD	50 ns	28-pin Plastic TSOP (II) (400 mil)	
μPD424805AG5-60-7KD	60 ns	Reverse bent	
μPD424805AG5-70-7KD	70 ns	Reverse bent	
μ PD424805ALE-50	50 ns	28-pin Plastic SOJ (400 mil)	
μ PD424805ALE-60	60 ns		
μ PD424805ALE-70	70 ns		

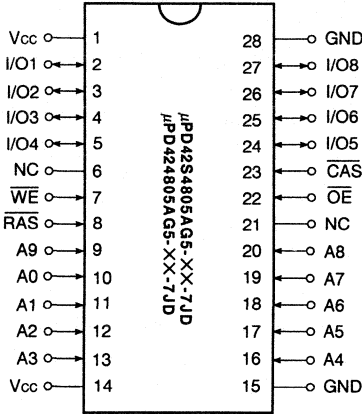
Quality Grade

Standard

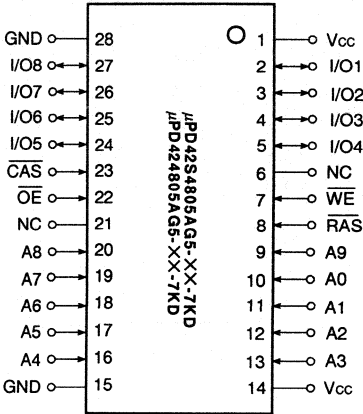
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking Side)

28-pin Plastic TSOP(III)
(400 mil)

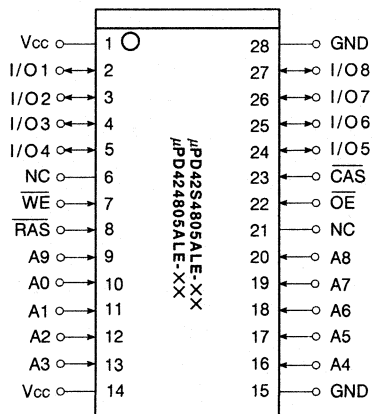


Reverse bent



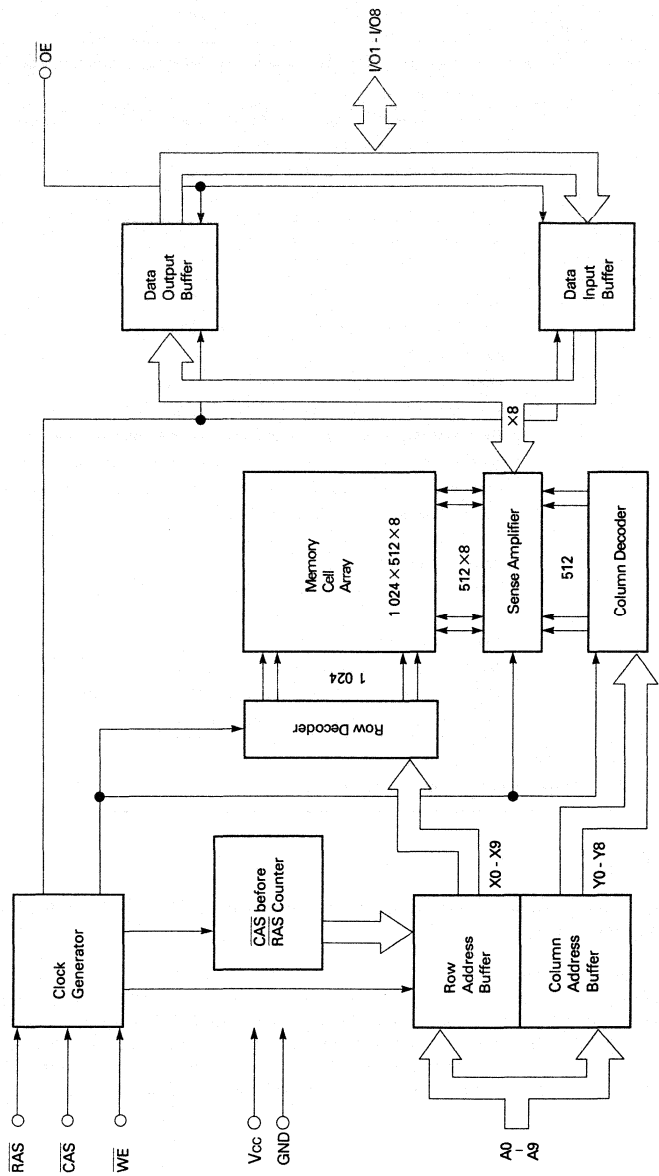
- A0 to A9 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

28-pin Plastic SOJ
(400 mil)



- A0 to A9 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Input/Output Pin Functions

The μ PD42S4805A, 424805A have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A9 and input/output pins I/O1 to I/O8.

Pin Name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address inputs)		Address bus. Input total 19-bit of address signal, upper 10-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 524 288-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input/ Output	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)		8-bit data bus. I/O1 to I/O8 are used to input/output data.

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

In the hyper page mode, the output data is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the CAS cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

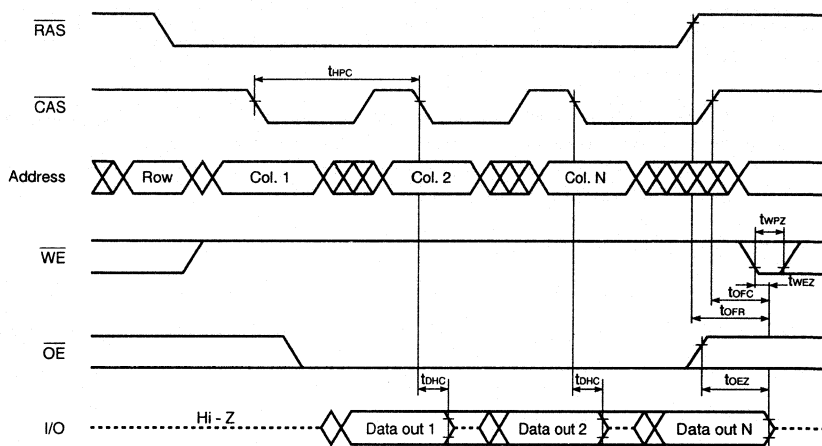
2. The $\overline{\text{CAS}}$ cycle time in the hyper page mode is shorter than that in the fast page mode.

In the hyper page mode, due to the data extend function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{\text{CAS}}$ cycle time in the hyper page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{\text{RAS}}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

Hyper Page Mode Read Cycle



To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.

- (1) $\overline{\text{RAS}}$, $\overline{\text{CAS}}$: inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

- (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$: active, $\overline{\text{OE}}$: active ... t_{WEZ} , t_{WPZ} are effective.

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: inactive ... t_{OEZ} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

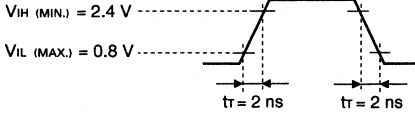
Parameter		Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling			80	mA	1, 2, 3
			trc = trc (MIN.)			70		
			lo = 0 mA			60		
Standby current	μ PD42S4805A	I _{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, lo = 0 mA			2	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2 V$, lo = 0 mA			0.15		
	μ PD424805A		$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, lo = 0 mA			2		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2 V$, lo = 0 mA			1		
$\overline{RAS}$ only refresh current		I _{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH(MIN.)}$	trac = 50 ns		80	mA	1, 2, 3, 4
			trc = trc (MIN.), lo = 0 mA	trac = 60 ns		70		
				trac = 70 ns		60		
Operating current (Hyper page mode)		I _{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling	thpc = 50 ns		80	mA	1, 2, 5
			thpc = thpc (MIN.), lo = 0 mA	trac = 60 ns		70		
				trac = 70 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I _{CC5}	$\overline{RAS}$ Cycling	trac = 50 ns		80	mA	1, 2
			trc = trc (MIN.)	trac = 60 ns		70		
			lo = 0 mA	trac = 70 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (1 024 Cycles / 128 ms, only for the μ PD42S4805A)		I _{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : 1 024 Cycles / 128 ms $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2 V \leq V_{IH} \leq V_{IH(MAX.)}$ $0 V \leq V_{IL} \leq 0.2 V$	trac $\leq$ 200 ns		200	μA	1, 2
			Standby : $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2 V$ Address : V_{IH} or V_{IL} WE, OE : V_{IH} lo = 0 mA	trac $\leq$ 1 μs		300		
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for the μ PD42S4805A)		I _{CC7}	$\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2 V \leq V_{IH} \leq V_{IH(MAX.)}$ $0 V \leq V_{IL} \leq 0.2 V$ lo = 0 mA			150	μA	2
Input leakage current		I _{I (L)}	$V_I = 0$ to 5.5 V All other pins not under test = 0 V	-10		+10	μA	
Output leakage current		I _{O (L)}	$V_O = 0$ to 5.5 V Output is disabled (Hi-Z)	-10		+10	μA	
High level output voltage		V _{OH}	lo = -5.0 mA	2.4			V	
Low level output voltage		V _{OL}	lo = +4.2 mA			0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (trc and thpc).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

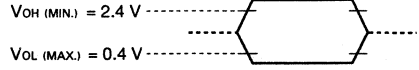
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	trac = 50 ns		trac = 60 ns		trac = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		trc	84	–	104	–	124	–	ns	
RAS Precharge Time		trp	30	–	40	–	50	–	ns	
CAS Precharge Time		tcpn	7	–	10	–	10	–	ns	
RAS Pulse Width		tras	50	10 000	60	10 000	70	10 000	ns	
CAS Pulse Width		tcas	7	10 000	10	10 000	12	10 000	ns	
RAS Hold Time		trsh	7	–	10	–	12	–	ns	
CAS Hold Time		tcsH	35	–	40	–	50	–	ns	
RAS to CAS Delay Time		trcd	11	37	14	45	14	52	ns	1
RAS to Column Address Delay Time		trad	9	25	12	30	12	35	ns	1
CAS to RAS Precharge Time		tcpR	5	–	5	–	5	–	ns	2
Row Address Setup Time		tasR	0	–	0	–	0	–	ns	
Row Address Hold Time		trah	7	–	10	–	10	–	ns	
Column Address Setup Time		tasc	0	–	0	–	0	–	ns	
Column Address Hold Time		tcaH	7	–	10	–	12	–	ns	
OE Lead Time Referenced to RAS		toes	0	–	0	–	0	–	ns	
CAS to Data Setup Time		tclZ	0	–	0	–	0	–	ns	
OE to Data Setup Time		tolZ	0	–	0	–	0	–	ns	
OE to Data Delay Time		toed	10	–	13	–	15	–	ns	
Transition Time (Rise and Fall)		tt	1	50	1	50	1	50	ns	
Refresh Time	μPD42S4805A	tref	–	128	–	128	–	128	ms	3
	μPD424805A		–	16	–	16	–	16	ms	

Notes 1. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD (MAX.) and trCD (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

2. tCRP (MIN.) requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
3. This specification is applied only to the μPD42S4805A.

Read Cycle

Parameter	Symbol	$\text{trAC} = 50 \text{ ns}$		$\text{trAC} = 60 \text{ ns}$		$\text{trAC} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	trAC	-	50	-	60	-	70	ns	1
Access Time from $\overline{\text{CAS}}$	tCAC	-	13	-	15	-	18	ns	1
Access Time from Column Address	tAA	-	25	-	30	-	35	ns	1
Access Time from $\overline{\text{OE}}$	tOEA	-	13	-	15	-	18	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	trAL	25	-	30	-	35	-	ns	
Read Command Setup Time	trCS	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	trRH	0	-	0	-	0	-	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	trCH	0	-	0	-	0	-	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	tOEZ	0	10	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD (MAX.) and trCD (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

2. Either trCH(MIN.) or trRH (MIN.) should be met in read cycles.
3. tOEZ (MAX.) defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	7	–	10	–	10	–	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	7	–	10	–	10	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	7	–	10	–	12	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	7	–	10	–	12	–	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	–	0	–	0	–	ns	
Data-in Setup Time	tds	0	–	0	–	0	–	ns	3
Data-in Hold Time	tdh	7	–	10	–	10	–	ns	3

- Notes**
1. twp(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch(MIN.) should be met.
 2. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. tds(MIN.) and tdh(MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	107	–	133	–	157	–	ns	
RAS to $\overline{\text{WE}}$ Delay Time	trwd	64	–	77	–	89	–	ns	1
CAS to $\overline{\text{WE}}$ Delay Time	tcwd	27	–	32	–	37	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	39	–	47	–	54	–	ns	1

- Note**
1. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwd ≥ trwd(MIN.), tcwd ≥ tcwd(MIN.), tawd ≥ tawd(MIN.), and tcpwd ≥ tcpwd(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	trAC = 50 ns		trAC = 60 ns		trAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tHPC	20	–	25	–	30	–	ns	
RAS Pulse Width	tRASP	50	125 000	60	125 000	70	125 000	ns	
CAS Pulse Width	tHCAS	7	10 000	10	10 000	12	10 000	ns	
CAS Precharge Time	tCP	7	–	10	–	10	–	ns	
Access Time from CAS Precharge	tACP	–	27	–	35	–	40	ns	
CAS Precharge to WE Delay Time	tCPWD	41	–	52	–	59	–	ns	1
RAS Hold Time from CAS Precharge	tRHCP	27	–	35	–	40	–	ns	
Read Modify Write Cycle Time	tHPRWC	52	–	66	–	75	–	ns	
Data Output Hold Time	tDHC	5	–	5	–	5	–	ns	
Output Buffer Turn-off Delay from WE	tWEZ	0	10	0	13	0	15	ns	2,3
WE Pulse Width	tWPZ	7	–	10	–	10	–	ns	3
Output Buffer Turn-off Delay from RAS	tOFR	0	10	0	13	0	15	ns	2,3
Output Buffer Turn-off Delay from CAS	tOFC	0	10	0	13	0	15	ns	2,3

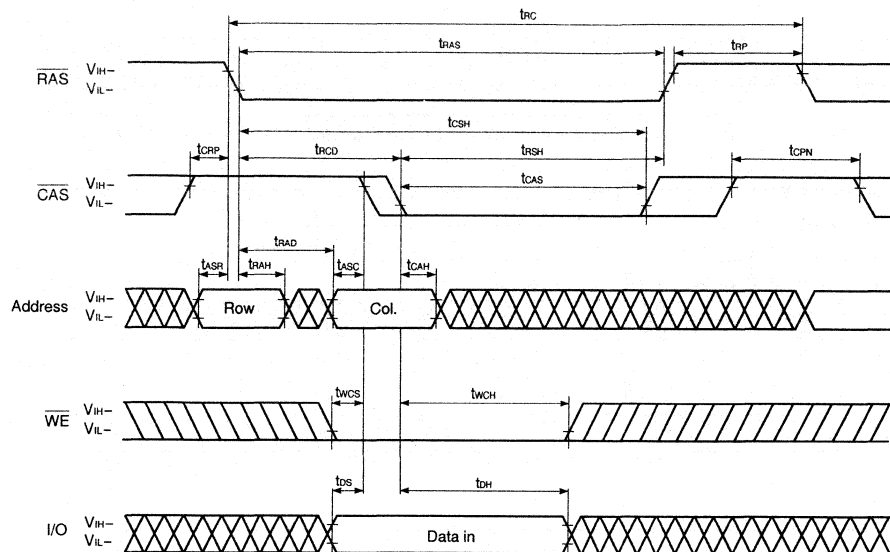
- Notes**
- If $tWCS \geq tWCS(MIN.)$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $tRWD \geq tRWD(MIN.)$, $tCWD \geq tCWD(MIN.)$, $tAWD \geq tAWD(MIN.)$, and $tCPWD \geq tCPWD(MIN.)$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
 - $tOFC(MAX.)$, $tOFR(MAX.)$ and $tWEZ(MAX.)$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .
 - To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.
 - $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)
 $\overline{WE}$: inactive, $\overline{OE}$: active
 $tOFC$ is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
 $tOFR$ is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
 - Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
 $\overline{WE}$: active, $\overline{OE}$: active ... $tWEZ$, $tWPZ$ are effective.
 $\overline{WE}$: inactive, $\overline{OE}$: inactive ... tOZ is effective.

Refresh Cycle

Parameter	Symbol	trAC = 50 ns		trAC = 60 ns		trAC = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	tCSR	5	–	5	–	5	–	ns	
CAS Hold Time (CAS before RAS Refresh)	tCHR	10	–	10	–	10	–	ns	
RAS Precharge CAS Hold Time	tRPC	5	–	5	–	5	–	ns	
RAS Pulse Width (CAS before RAS Self Refresh)	tRASS	100	–	100	–	100	–	μ s	1
RAS Precharge Time (CAS before RAS Self Refresh)	tRPS	90	–	110	–	130	–	ns	1
CAS Hold Time (CAS before RAS Self Refresh)	tCHS	–50	–	–50	–	–50	–	ns	1
WE Hold Time (Hidden Refresh Cycle)	tWHR	15	–	15	–	15	–	ns	

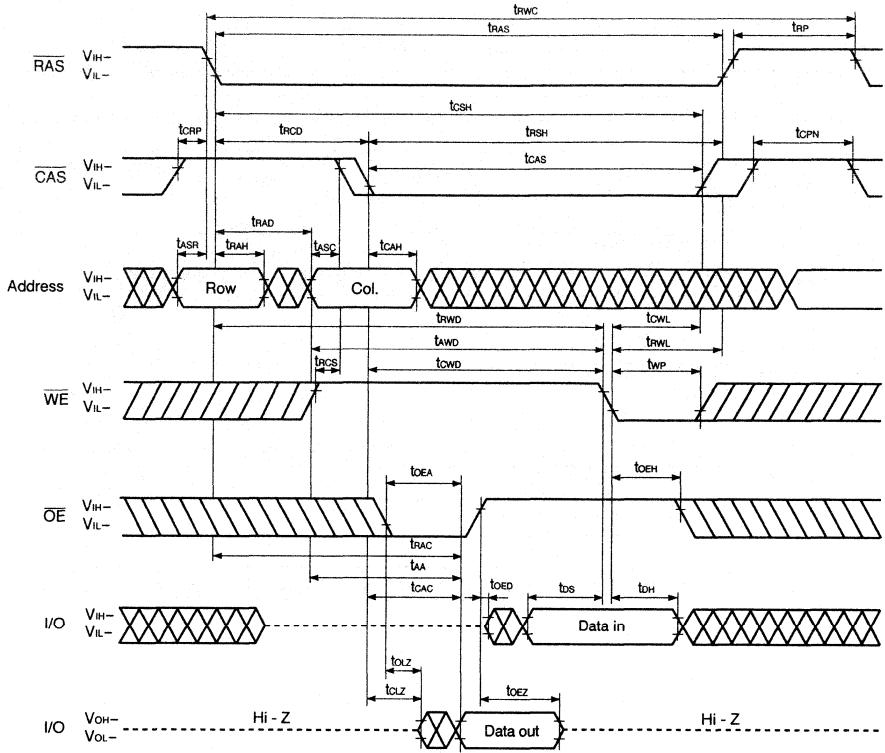
- Note** 1. This specification is applied only to the μ PD42S4805A.

Early Write Cycle



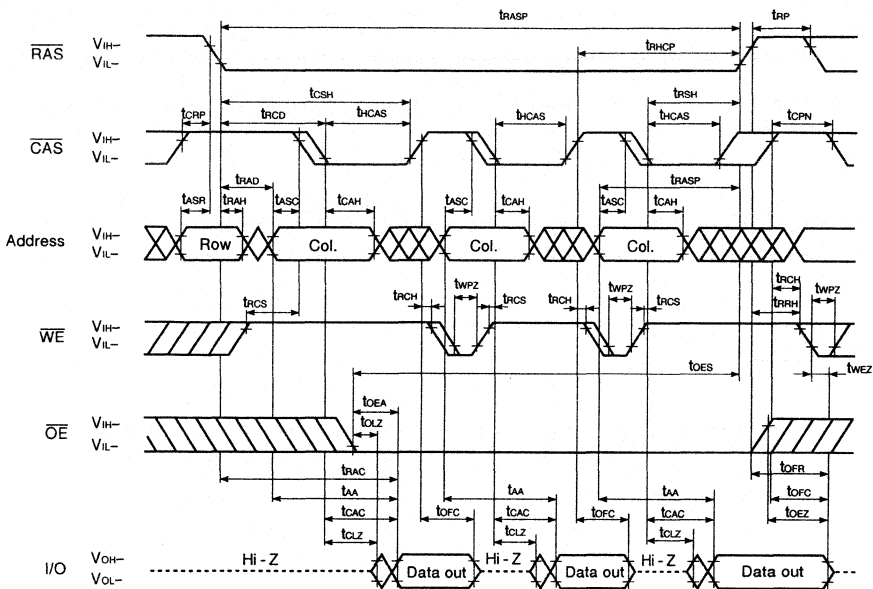
Remark $\overline{OE}$: Don't care

Read Modify Write Cycle

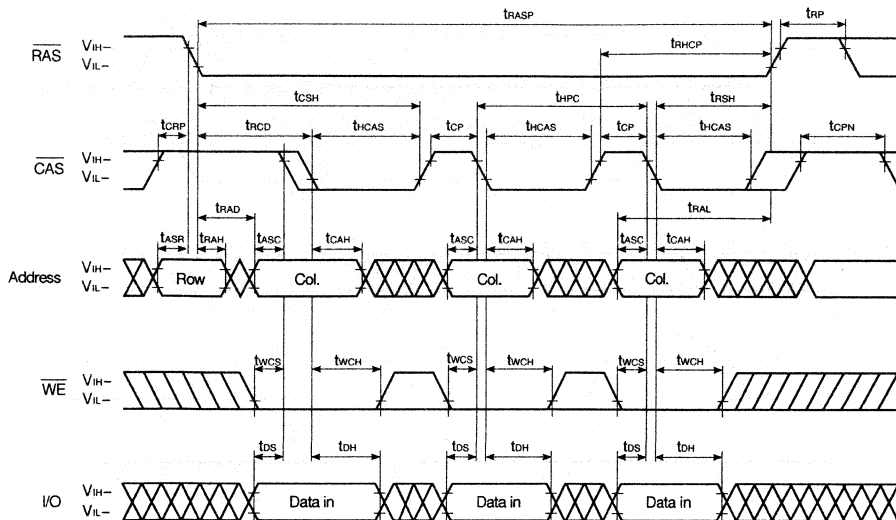


[illegible]

Hyper Page Mode Read Cycle ($\overline{\text{WE}}$ Control)

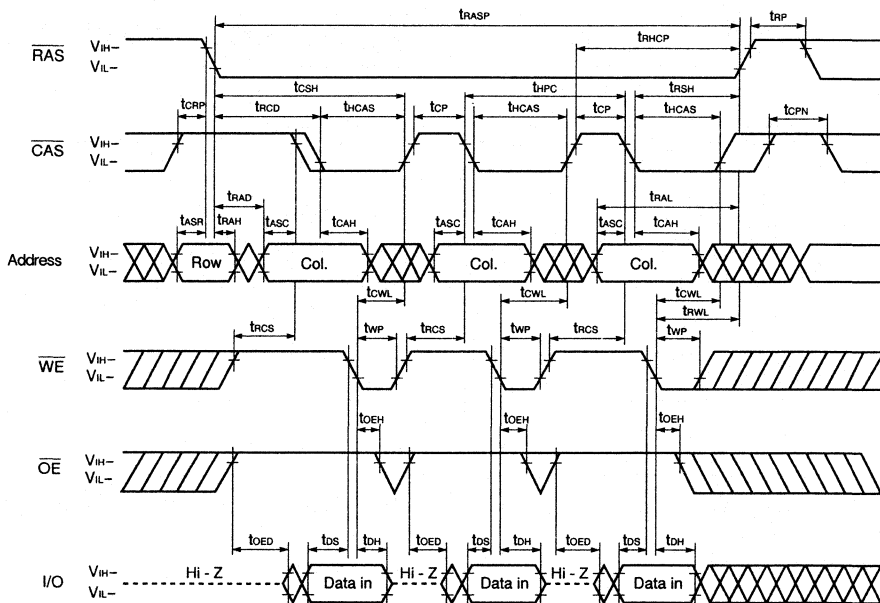


Hyper Page Mode Early Write Cycle

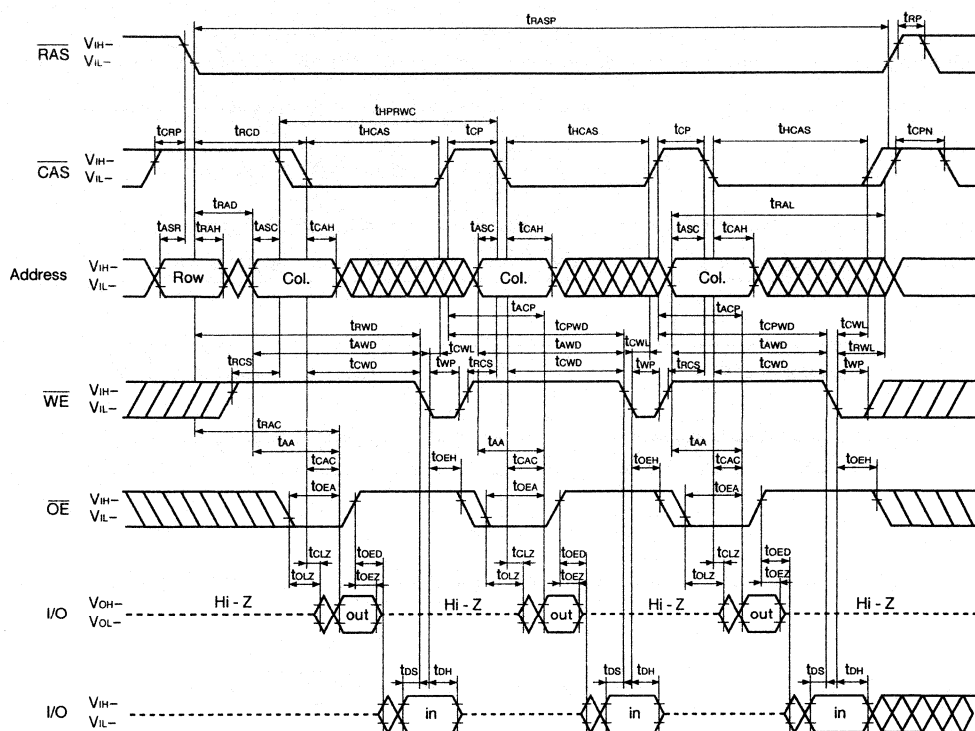


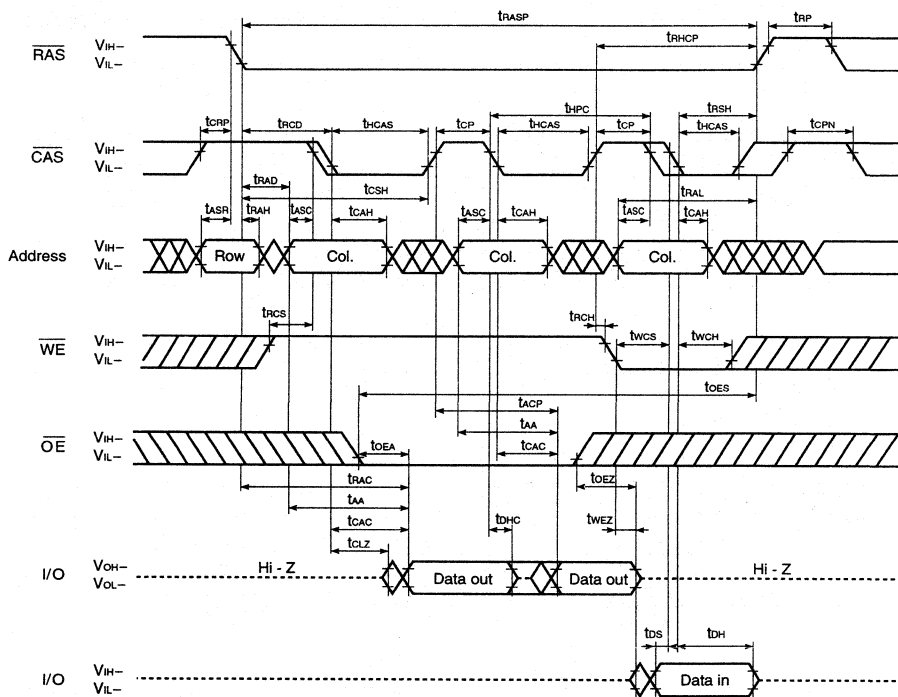
Remark $\overline{OE}$: Don't care

Hyper Page Mode Late Write Cycle

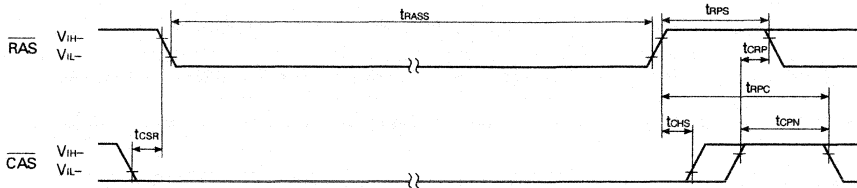


Hyper Page Mode Read Modify Write Cycle





CAS Before RAS Self Refresh Cycle (Only for the μPD42S4805A)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi - Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh ; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

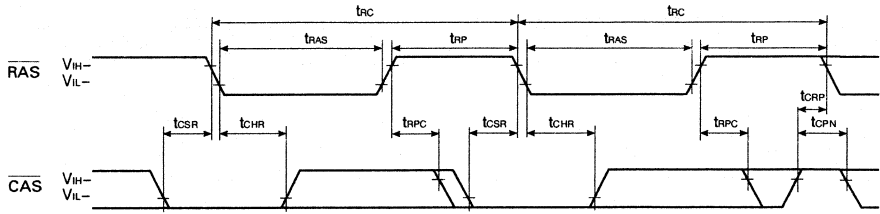
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 1 024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh 1 024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

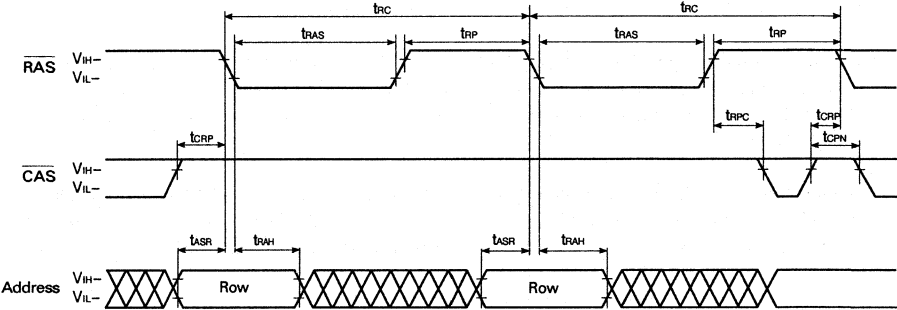
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



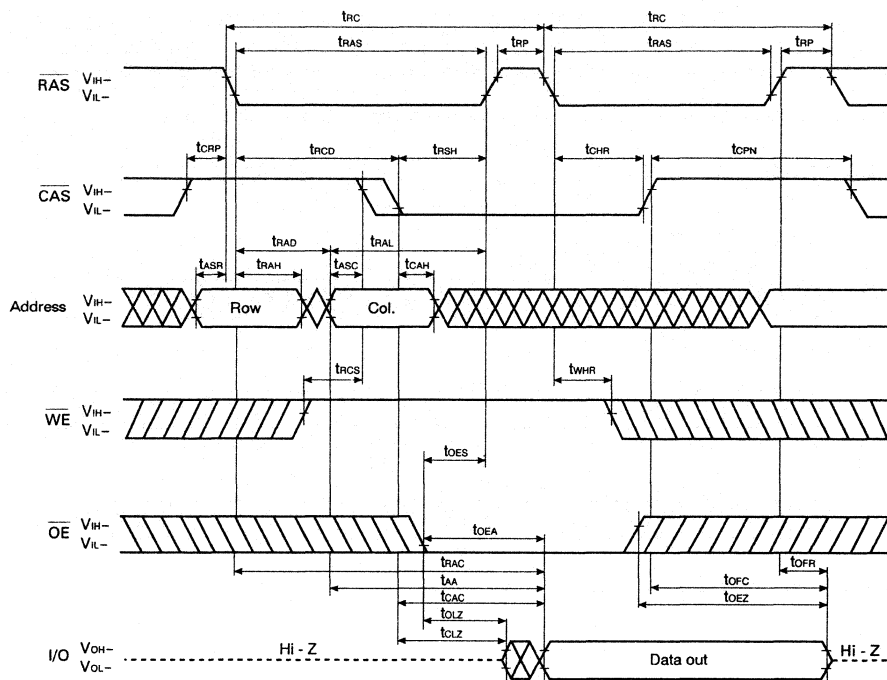
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi-Z

RAS Only Refresh Cycle

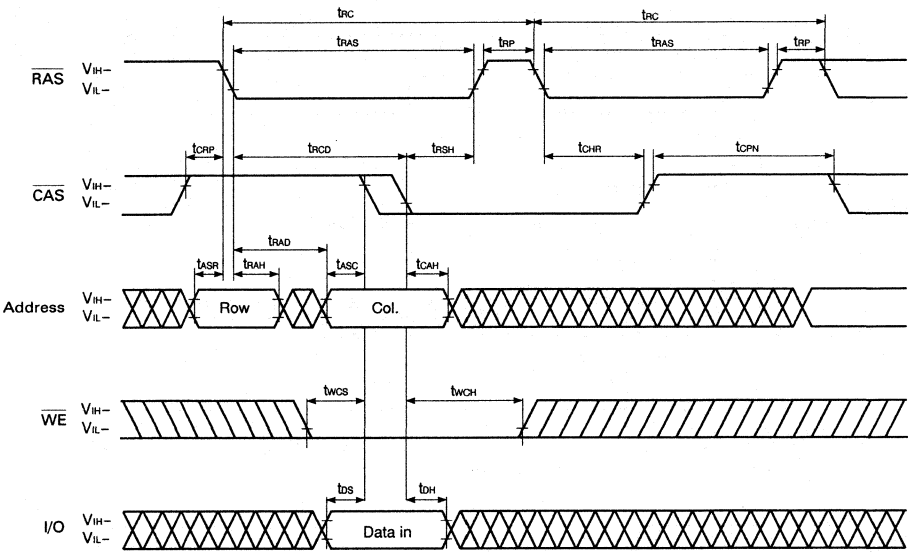


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi-Z

Hidden Refresh Cycle (Read)



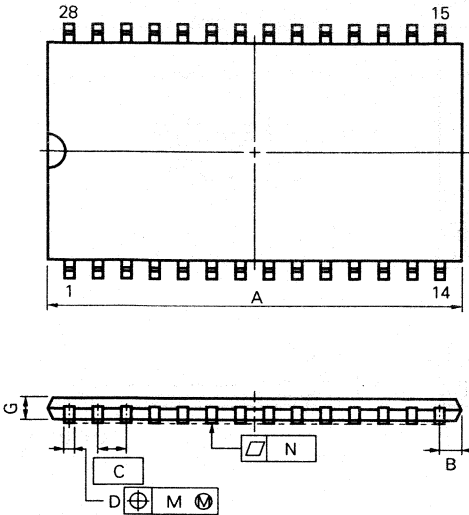
Hidden Refresh Cycle (Write)



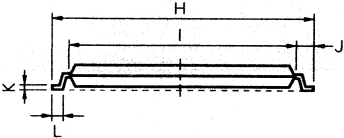
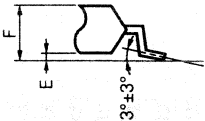
Remark $\overline{OE}$: Don't care

Package Drawings

28 PIN PLASTIC TSOP(III) (400 mil)



detail of lead end



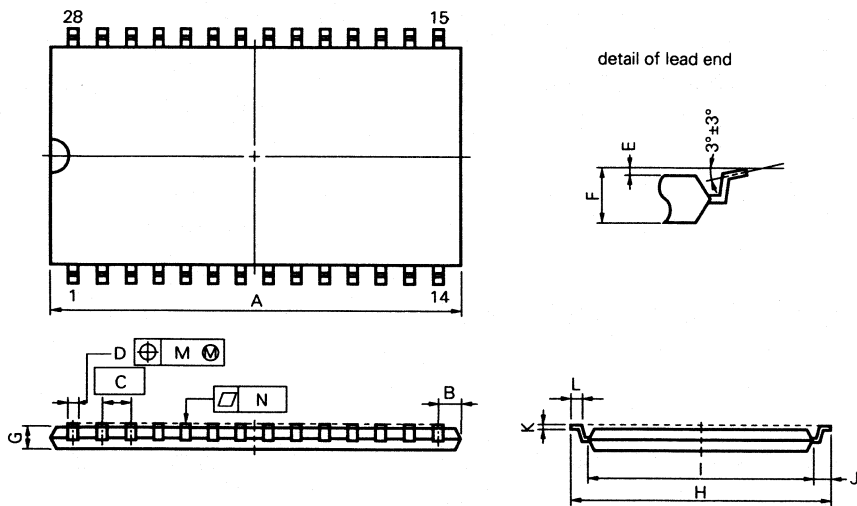
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD-2

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.005}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP(II) (400 mil)



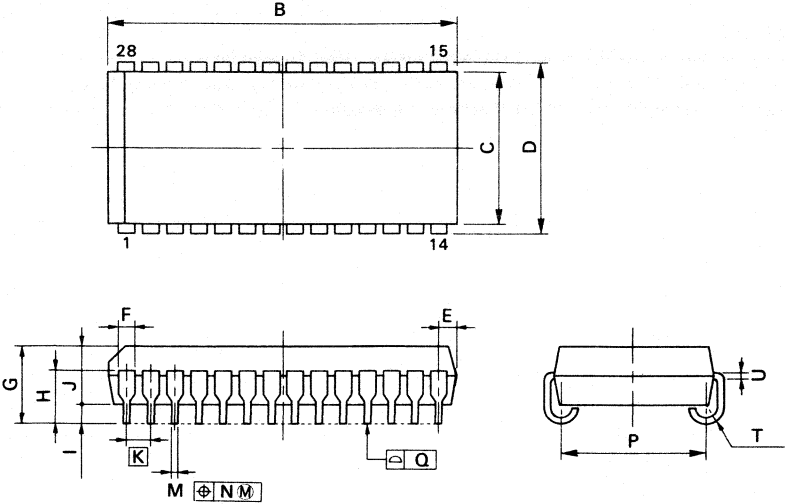
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7KD-2

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28PIN PLASTIC SOJ (400 mil)



P28LA-400A-1

NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	18.67 ^{+0.35} _{-0.35}	0.735 ^{+0.008} _{-0.008}
C	10.16	0.400
D	11.18 ^{+0.2}	0.440 ^{+0.008} _{-0.008}
E	1.08 ^{+0.15}	0.043 ^{+0.006} _{-0.006}
F	0.6	0.024
G	3.5 ^{+0.2}	0.138 ^{+0.008} _{-0.008}
H	2.4 ^{+0.2}	0.094 ^{+0.008} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40 ^{+0.10}	0.016 ^{+0.004} _{-0.004}
N	0.12	0.005
P	9.40 ^{+0.20}	0.370 ^{+0.008} _{-0.008}
Q	0.15	0.006
T	R0.85	R0.033
U	0.20 ^{+0.05} _{-0.05}	0.008 ^{+0.002} _{-0.002}

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD42S4805A, 424805A.

Types of Surface Mount Device

μ PD42S4805AG5-XX-7JD, 424805AG5-XX-7JD : 28-pin Plastic TSOP (II) (400 mil)

μ PD42S4805AG5-XX-7KD, 424805AG5-XX-7KD : 28-pin Plastic TSOP (II) (400 mil) Reverse bent

μ PD42S4805ALE-XX, 424805ALE-XX : 28-pin Plastic SOJ (400 mil)

MOS INTEGRATED CIRCUIT

μ PD42S4260, 424260

4 M-BIT DYNAMIC RAM

256 K-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

Description

The μ PD42S4260, 424260 are 262,144 words by 16 bits dynamic CMOS RAMs. The fast page mode and byte read/write mode capability realize high speed access and low power consumption.

Besides, the μ PD42S4260 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

These are packaged in 44-pin plastic TSOP (III) and 40-pin plastic SOJ.

★

Features

- 262,144 words by 16 bits organization
- Single +5.0 V ± 10 % power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S4260-70, 424260-70	880.0 mW	70 ns	130 ns	45 ns
μ PD42S4260-80, 424260-80	797.5 mW	80 ns	150 ns	50 ns

- The μ PD42S4260 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S4260	512 cycles / 128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	0.825 mW (CMOS level input)
μ PD424260	512 cycles / 8 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

- Multiplexed address inputs ... Row address: A0 to A8, Column address: A0 to A8

The information in this document is subject to change without notice.

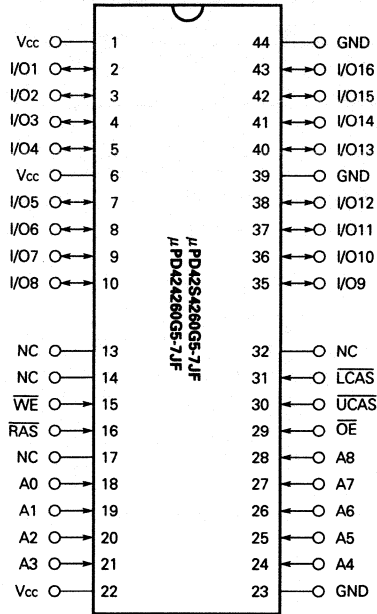
★ Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD42S4260G5-70-7JF	70 ns	44-pin Plastic TSOP (II) (400 mil)	CAS before RAS self refresh
μPD42S4260G5-80-7JF	80 ns		CAS before RAS refresh
μPD42S4260LE-70	70 ns	40-pin Plastic SOJ (400 mil)	RAS only refresh
μPD42S4260LE-80	80 ns		Hidden refresh
μPD424260G5-70-7JF	70 ns	44-pin Plastic TSOP (II) (400 mil)	CAS before RAS refresh
μPD424260G5-80-7JF	80 ns		RAS only refresh
μPD424260LE-70	70 ns	40-pin Plastic SOJ (400 mil)	Hidden refresh
μPD424260LE-80	80 ns		

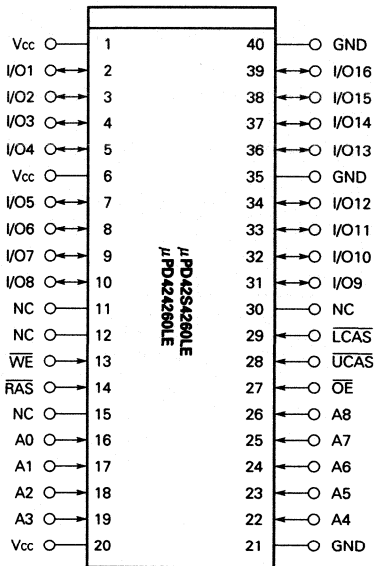
Pin Configurations (Marking Side)



44-pin Plastic TSOP (II)
(400 mil)

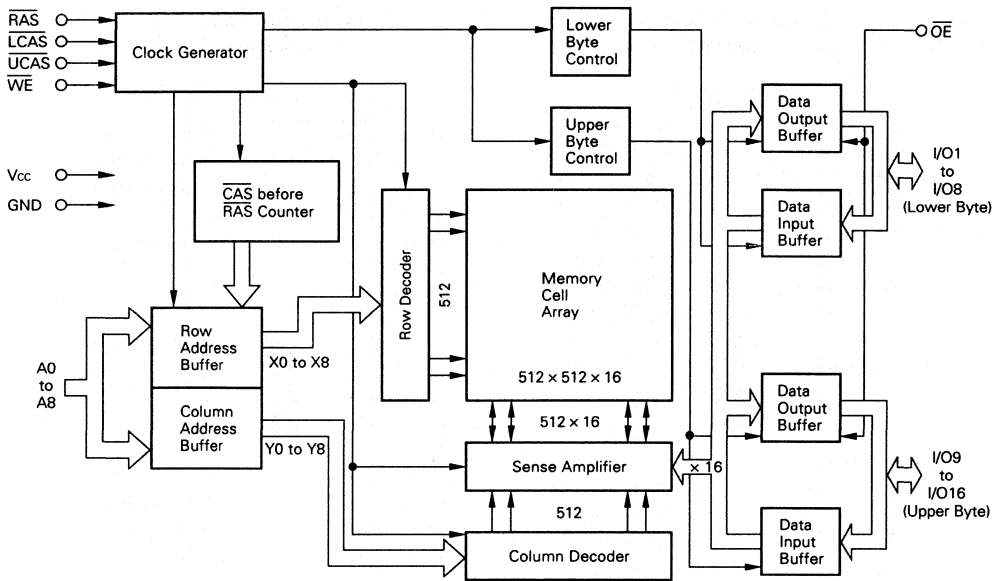


40-pin Plastic SOJ
(400 mil)



- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
- LCAS : Column Address Strobe (lower)
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Input/Output Pin Functions

The μ PD42S4260, 424260 have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ^{Note}, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A8 and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address (A0 to A8) and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address (A0 to A8). It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)	Input	$\overline{\text{CAS}}$ activates data input/output circuit by latching column address (A0 to A8) and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address input)	Input	9-bit address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word (16-bit) is selected from 262,144-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data input/ output)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^{\circ}\text{C}$

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	$^{\circ}\text{C}$

Capacitance ($T_A = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	RAS, $\overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$, $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$		160	mA	1, 2, 3
				$t_{\text{RAC}} = 80 \text{ ns}$		145		
Standby current	μ PD42S4260	I _{CC2}	RAS, $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$, $I_O = 0 \text{ mA}$			2	mA	
			RAS, $\overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$, $I_O = 0 \text{ mA}$			0.15		
	μ PD424260		RAS, $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$, $I_O = 0 \text{ mA}$			2		
			RAS, $\overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$, $I_O = 0 \text{ mA}$			1		
RAS only refresh current		I _{CC3}	RAS Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$, $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$		160	mA	1, 2, 3, 4
				$t_{\text{RAC}} = 80 \text{ ns}$		145		
Operating current (Fast page mode)		I _{CC4}	RAS $\leq V_{\text{IL}}(\text{MAX.})$, $\overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.})$, $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$		140	mA	1, 2, 5
				$t_{\text{RAC}} = 80 \text{ ns}$		130		
CAS before RAS refresh current		I _{CC5}	RAS Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$, $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$		160	mA	1, 2
				$t_{\text{RAC}} = 80 \text{ ns}$		145		
CAS before RAS long refresh current (512 Cycles / 128 ms, only for the μ PD42S4260)		I _{CC6}	CAS before RAS refresh: $t_{\text{RC}} = 250.0 \mu\text{s}$ RAS, $\overline{\text{CAS}}$: $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}(\text{MAX.})}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$	$t_{\text{RAS}} \leq 200 \text{ ns}$		200	μA	1, 2 ★
			Standby: RAS, $\overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address: V_{IH} or V_{IL} $\overline{\text{WE}}$, $\overline{\text{OE}}$: V_{IH} $I_O = 0 \text{ mA}$	$t_{\text{RAS}} \leq 1 \mu\text{s}$		300	μA	1, 2 ★
Self refresh current (CAS before RAS self refresh, only for the μ PD42S4260)		I _{CC7}	RAS, $\overline{\text{CAS}}$: $t_{\text{RAS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}(\text{MAX.})}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_O = 0 \text{ mA}$			150	μA	2 ★
Input leakage current		I _{IL(L)}	$V_I = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10		+10	μA	
Output leakage current		I _{OL(L)}	$V_O = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10		+10	μA	
High level output voltage		V _{OH}	$I_O = -2.5 \text{ mA}$	2.4			V	
Low level output voltage		V _{OL}	$I_O = +2.1 \text{ mA}$			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

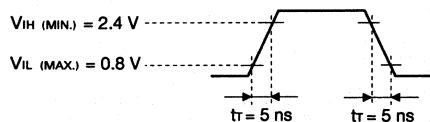
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$.

4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

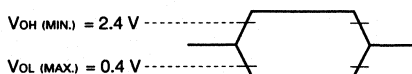
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)**AC Characteristics Test Conditions**

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	tRC	130	–	150	–	ns	
RAS Precharge Time	tRP	50	–	60	–	ns	
CAS Precharge Time	tCPN	10	–	10	–	ns	
RAS Pulse Width	tRAS	70	10,000	80	10,000	ns	
CAS Pulse Width	tCAS	20	10,000	20	10,000	ns	
RAS Hold Time	tRSH	20	–	20	–	ns	
CAS Hold Time	tCSH	70	–	80	–	ns	
RAS to CAS Delay Time	tRCD	20	50	20	60	ns	1
RAS to Column Address Delay Time	tRAD	15	35	15	40	ns	1
CAS to RAS Precharge Time	tCRP	10	–	10	–	ns	2
Row Address Setup Time	tASR	0	–	0	–	ns	
Row Address Hold Time	tRAH	10	–	10	–	ns	
Column Address Setup Time	tASC	0	–	0	–	ns	
Column Address Hold Time	tCAH	15	–	15	–	ns	
OE Lead Time Referenced to RAS	tOES	0	–	0	–	ns	
CAS to Data Setup Time	tCLZ	0	–	0	–	ns	
OE to Data Setup Time	tOLZ	0	–	0	–	ns	
OE to Data Delay Time	tOED	15	–	20	–	ns	
Masked Byte Write Hold Time Referenced to RAS	tMRH	0	–	0	–	ns	
Transition Time (Rise and Fall)		tT	3	50	3	50	ns
Refresh Time	μPD42S4260	tREF	–	128	–	128	ms
	μPD424260		–	8	–	8	ms

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{t}_{\text{RAD}} \leq \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \leq \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{RAC}}(\text{MAX.})$	$\text{t}_{\text{RAC}}(\text{MAX.})$
$\text{t}_{\text{RAD}} > \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \leq \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{AA}}(\text{MAX.})$	$\text{t}_{\text{RAD}} + \text{t}_{\text{AA}}(\text{MAX.})$
$\text{t}_{\text{RCD}} > \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{CAC}}(\text{MAX.})$	$\text{t}_{\text{RCD}} + \text{t}_{\text{CAC}}(\text{MAX.})$

$\text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{t}_{\text{RAD}} \geq \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \geq \text{t}_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

- $\text{t}_{\text{CRP}}(\text{MIN.})$ requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles preceded by any cycle.
- This specification is applied only to the μ PD42S4260.

Read Cycle

Parameter	Symbol	$\text{t}_{\text{RAC}} = 70 \text{ ns}$		$\text{t}_{\text{RAC}} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	–	70	–	80	ns	1
Access Time from $\overline{\text{CAS}}$	t_{CAC}	–	20	–	20	ns	1
Access Time from Column Address	t_{AA}	–	35	–	40	ns	1
Access Time from $\overline{\text{OE}}$	t_{OEA}	–	20	–	20	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t_{RAL}	35	–	40	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{RCH}	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t_{OEZ}	0	15	0	20	ns	3
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t_{OFF}	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{t}_{\text{RAD}} \leq \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \leq \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{RAC}}(\text{MAX.})$	$\text{t}_{\text{RAC}}(\text{MAX.})$
$\text{t}_{\text{RAD}} > \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \leq \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{AA}}(\text{MAX.})$	$\text{t}_{\text{RAD}} + \text{t}_{\text{AA}}(\text{MAX.})$
$\text{t}_{\text{RCD}} > \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{CAC}}(\text{MAX.})$	$\text{t}_{\text{RCD}} + \text{t}_{\text{CAC}}(\text{MAX.})$

$\text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{t}_{\text{RAD}} \geq \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \geq \text{t}_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

- Either $\text{t}_{\text{RCH}}(\text{MIN.})$ or $\text{t}_{\text{RRH}}(\text{MIN.})$ should be met in read cycles.
- $\text{t}_{\text{OFF}}(\text{MAX.})$ and $\text{t}_{\text{OEZ}}(\text{MAX.})$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	15	–	15	–	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	15	–	15	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	20	–	20	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	15	–	20	–	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	–	0	–	ns	2
OE Hold Time	toeh	0	–	0	–	ns	
Data-in Setup Time	t _{ds}	0	–	0	–	ns	3
Data-in Hold Time	t _{dh}	15	–	20	–	ns	3

Notes 1. t_{wp} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{wch} (MIN.) should be met.

2. If t_{wcs} ≥ t_{wcs} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. t_{ds} (MIN.) and t_{dh} (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	175	–	200	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	90	–	105	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	40	–	45	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	55	–	65	–	ns	1

Note 1. If t_{wcs} ≥ t_{wcs} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwd ≥ trwd (MIN.), tcwd ≥ tcwd (MIN.), tawd ≥ tawd (MIN.) and tcpwd ≥ tcpwd (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	trac = 70 ns		trac = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	45	–	50	–	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	–	40	–	45	ns	
RAS Pulse Width	t _{RASP}	70	125,000	80	125,000	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	–	10	–	ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40	–	45	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	90	–	105	–	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	60	–	70	–	ns	1

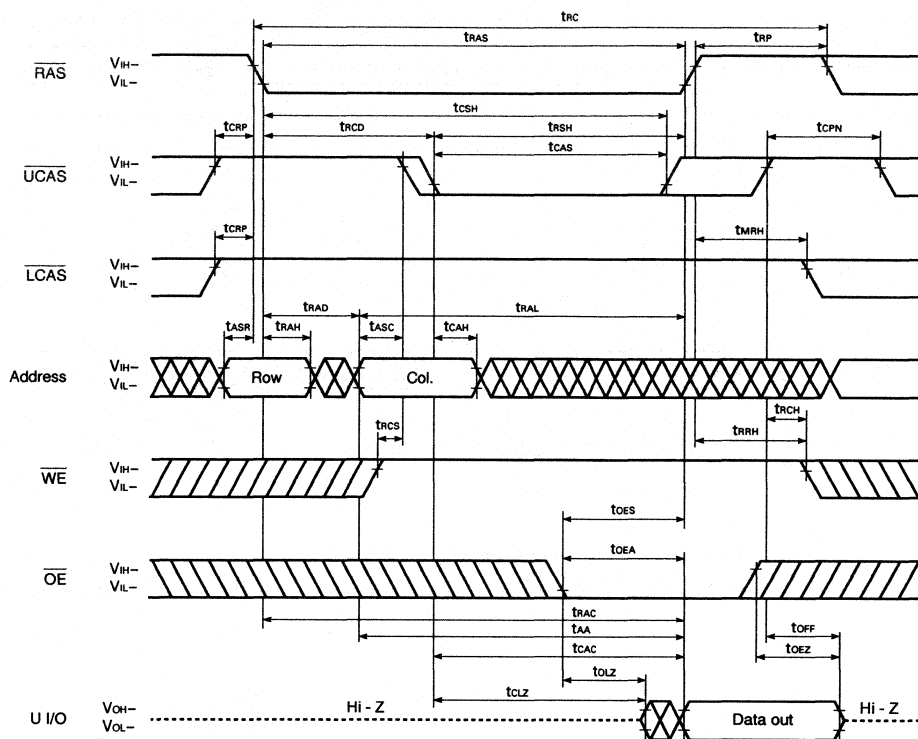
Note 1. If $\text{twcs} \geq \text{twcs (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{trwd} \geq \text{trwd (MIN.)}$, $\text{tcwd} \geq \text{tcwd (MIN.)}$, $\text{tawd} \geq \text{tawd (MIN.)}$ and $\text{tcpwd} \geq \text{tcpwd (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

Parameter	Symbol	trac = 70 ns		trac = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ Setup Time	t _{CSR}	10	–	10	–	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before RAS Refresh)	t _{CHR}	15	–	15	–	ns	
RAS Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10	–	10	–	ns	
RAS Pulse Width ($\overline{\text{CAS}}$ before RAS Self Refresh Cycle)	t _{RASS}	100	–	100	–	μ s	1
RAS Precharge Time ($\overline{\text{CAS}}$ before RAS Self Refresh Cycle)	t _{RPS}	130	–	150	–	ns	1
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before RAS Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ Hold Time (Hidden Refresh Cycle)	t _{WHR}	15	–	15	–	ns	

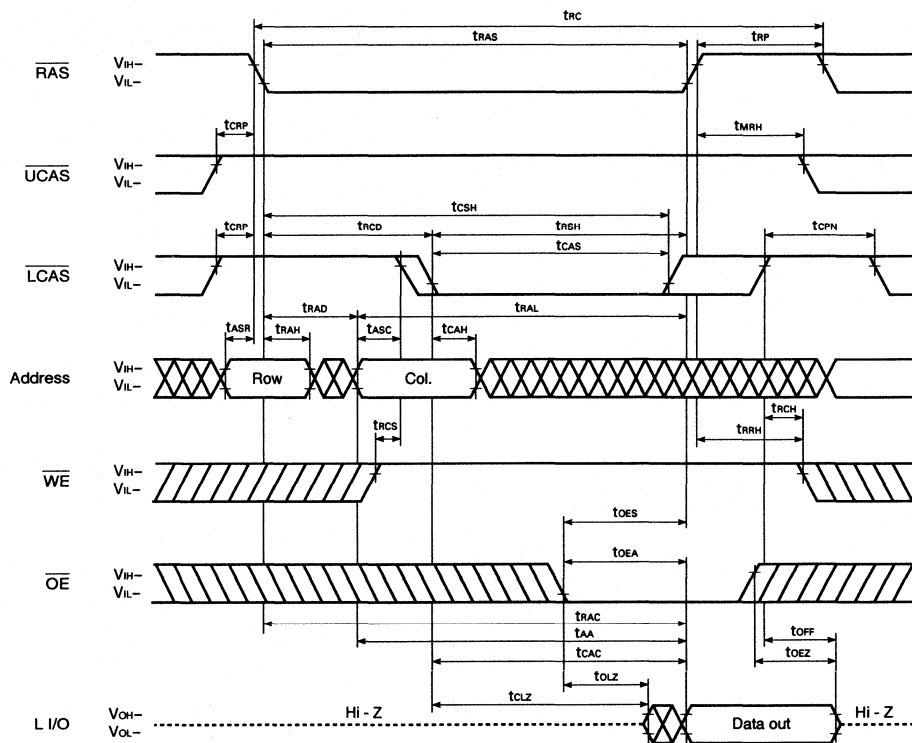
Note 1. This specification is applied only to the μ PD42S4260.

Upper Byte Read Cycle



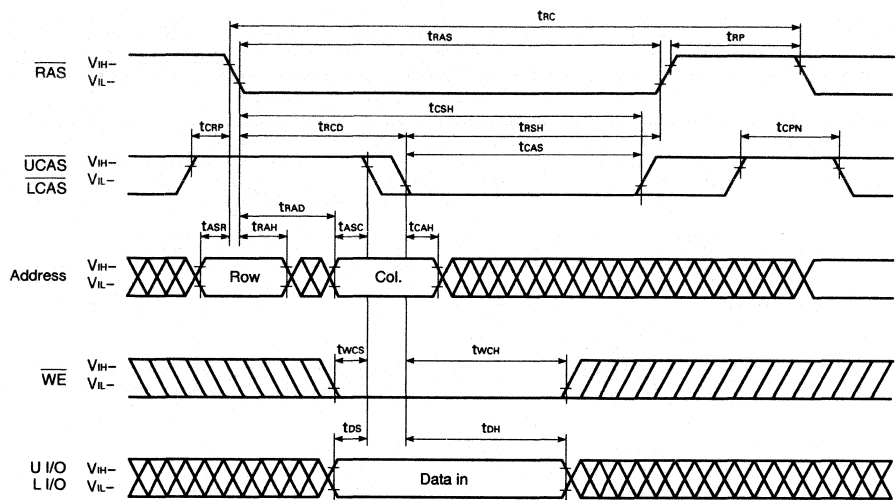
Remark L I/O: Hi-Z

Lower Byte Read Cycle



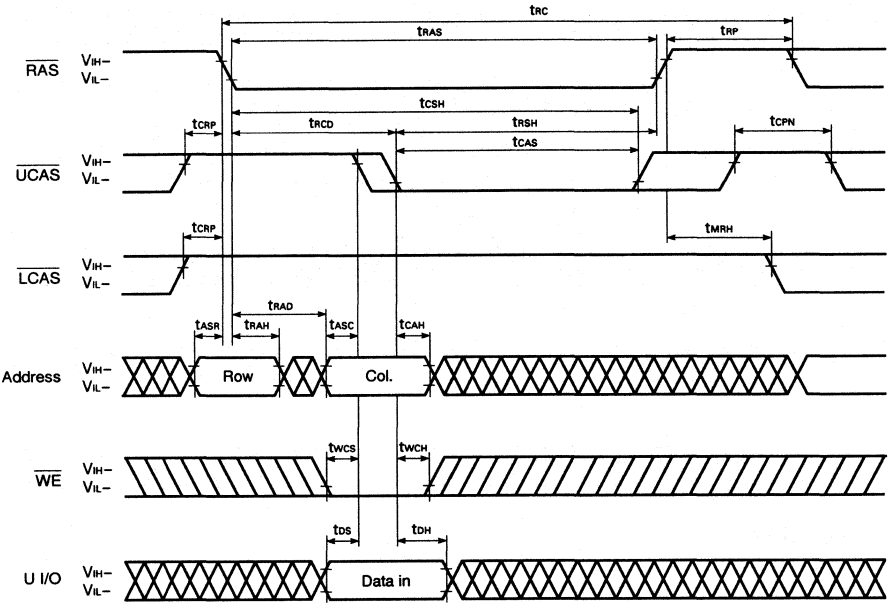
Remark U I/O: Hi-Z

Early Write Cycle



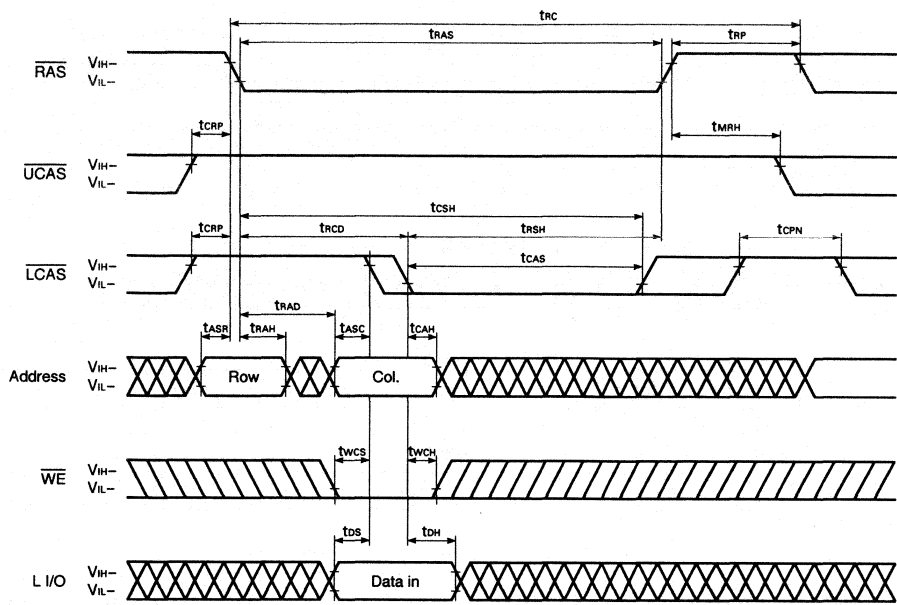
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



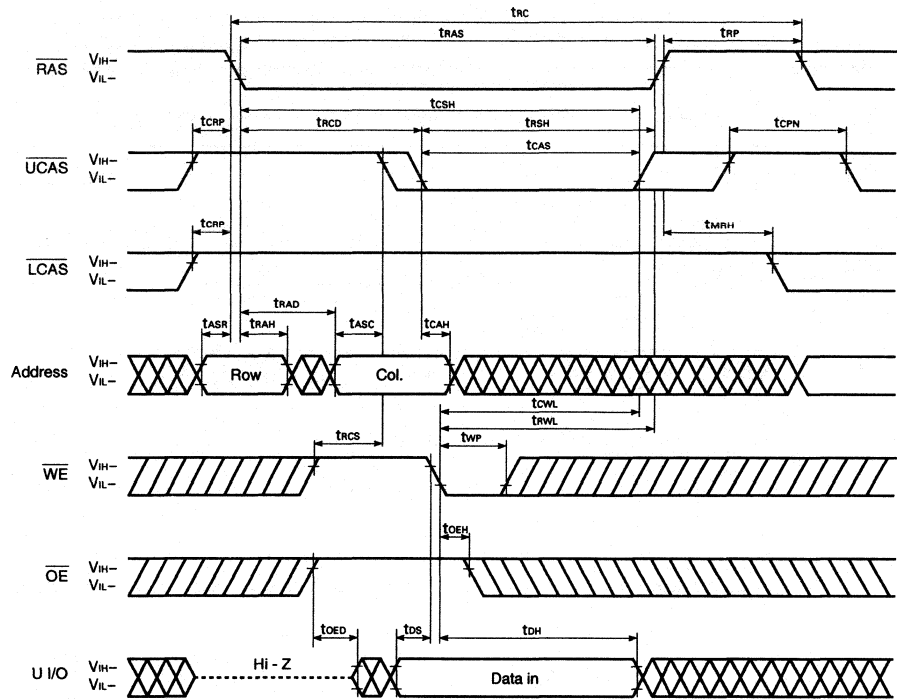
Remark $\overline{\text{OE}}$, L I/O: Don't care

Lower Byte Early Write Cycle



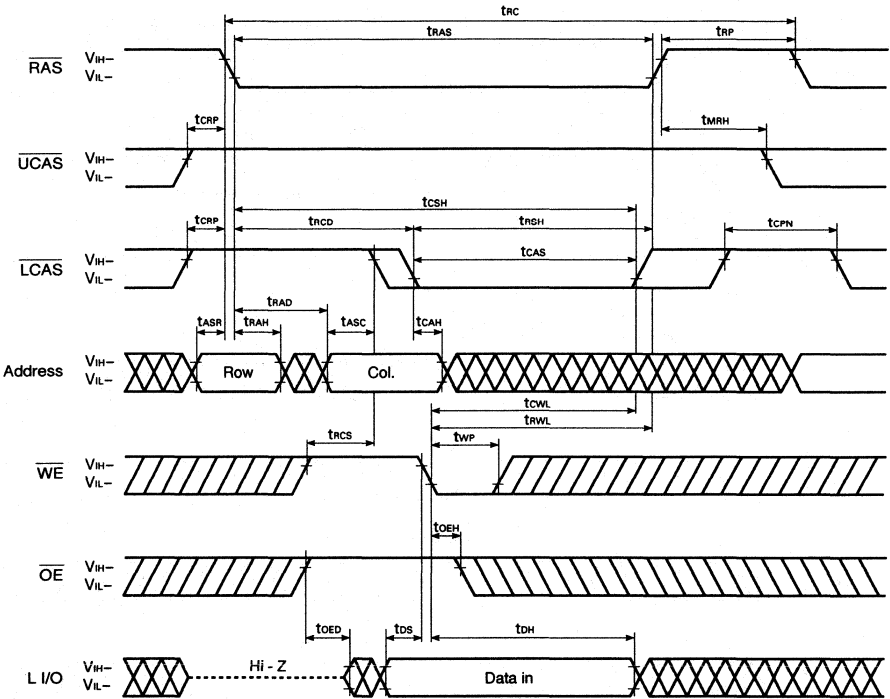
Remark $\overline{\text{OE}}$, U I/O: Don't care

Upper Byte Late Write Cycle



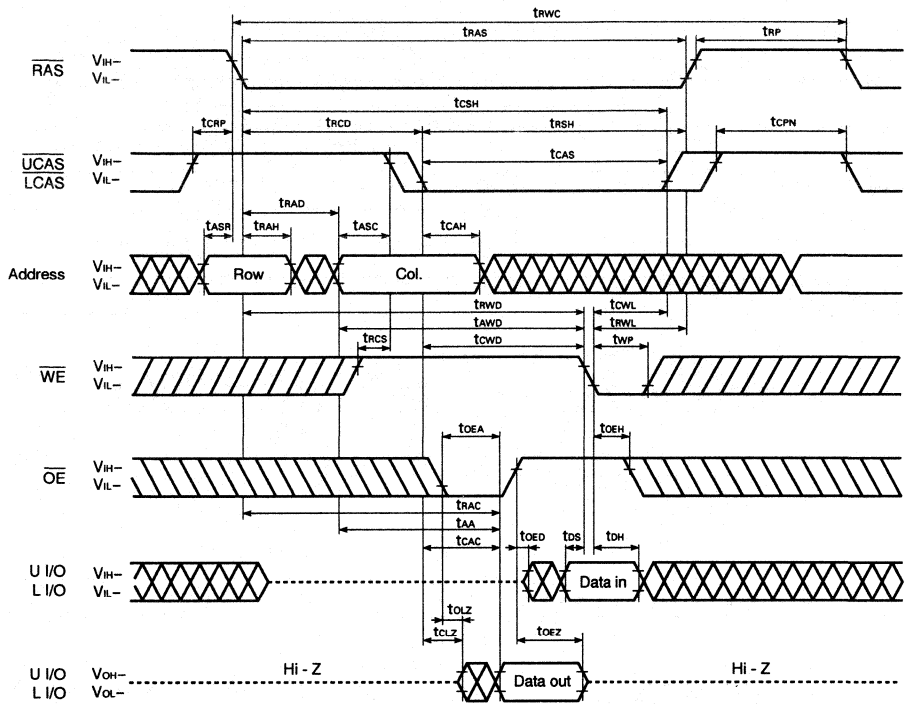
Remark L I/O: Don't care

Lower Byte Late Write Cycle

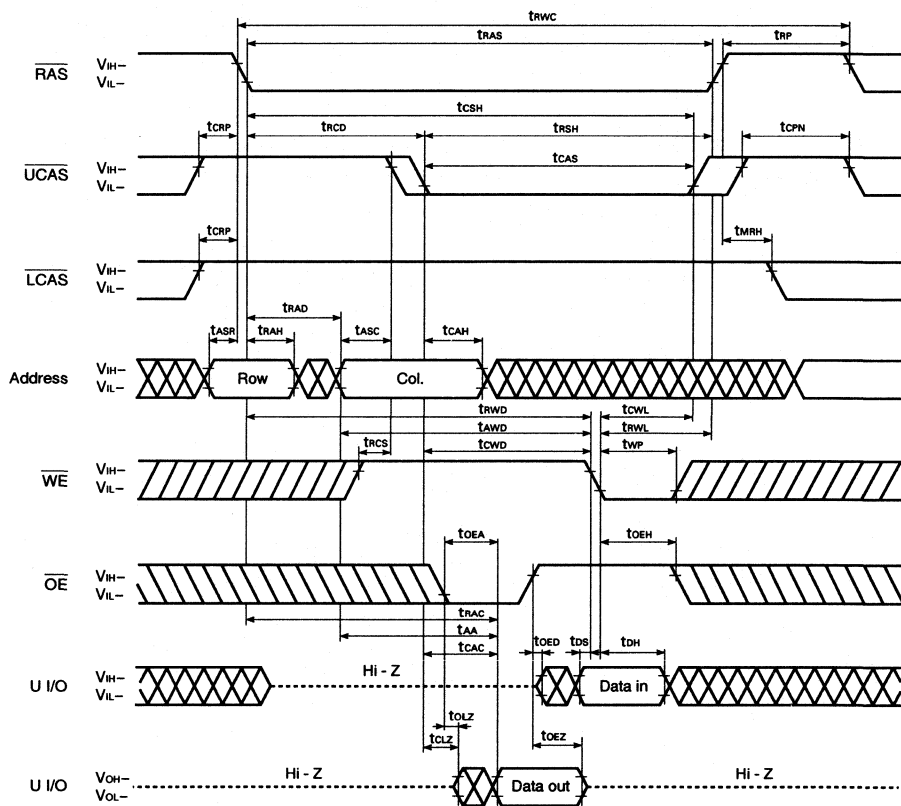


Remark U I/O: Don't care

Read Modify Write Cycle



Upper Byte Read Modify Write Cycle



Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

The timing diagram illustrates the relationship between various control and data signals for the 64K1602 LCD module. The signals shown are:

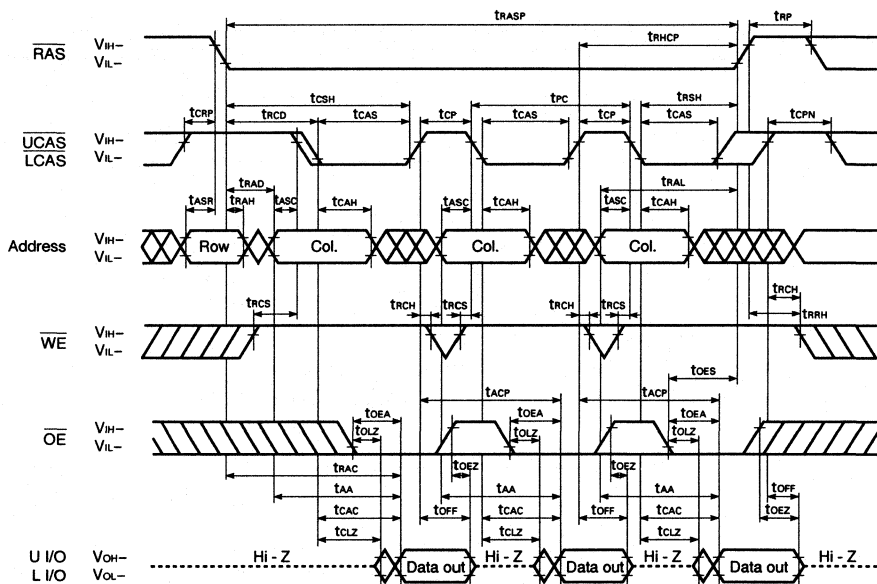
- RAS**: Row Address Strobe, active low.
- UCAS**: Upper Column Address Strobe, active low.
- LCAS**: Lower Column Address Strobe, active low.
- Address**: Data bus for Row and Column addresses.
- WE**: Write Enable, active low.
- OE**: Output Enable, active low.
- L I/O**: Low-level Input/Output data bus.
- Hi-Z**: High-impedance state for the data bus.

Key timing parameters are indicated by arrows and labels:

- trwc**: Row Address Setup Time before RAS.
- trp**: Row Address Pulse Width.
- tcrp**: Row Address Setup Time before UCAS.
- ttrh**: Row Address Setup Time before LCAS.
- trcd**: Row Address Setup Time before UCAS.
- ttrsh**: Row Address Setup Time before LCAS.
- tcsh**: Row Address Setup Time before LCAS.
- tcas**: Row Address Setup Time before LCAS.
- tcpsn**: Row Address Setup Time before LCAS.
- trsr**: Row Address Setup Time before UCAS.
- trah**: Row Address Setup Time before LCAS.
- tasc**: Row Address Setup Time before LCAS.
- tcah**: Row Address Setup Time before LCAS.
- trwd**: Row Address Setup Time before UCAS.
- tawl**: Row Address Setup Time before LCAS.
- trwl**: Row Address Setup Time before LCAS.
- twp**: Row Address Setup Time before LCAS.
- trcs**: Row Address Setup Time before UCAS.
- toea**: Row Address Setup Time before UCAS.
- toeh**: Row Address Setup Time before LCAS.
- trac**: Row Address Setup Time before UCAS.
- taa**: Row Address Setup Time before LCAS.
- tcac**: Row Address Setup Time before LCAS.
- toed**: Row Address Setup Time before UCAS.
- tps**: Row Address Setup Time before LCAS.
- tdi**: Row Address Setup Time before LCAS.
- toez**: Row Address Setup Time before UCAS.
- tolz**: Row Address Setup Time before LCAS.
- tclz**: Row Address Setup Time before LCAS.

Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

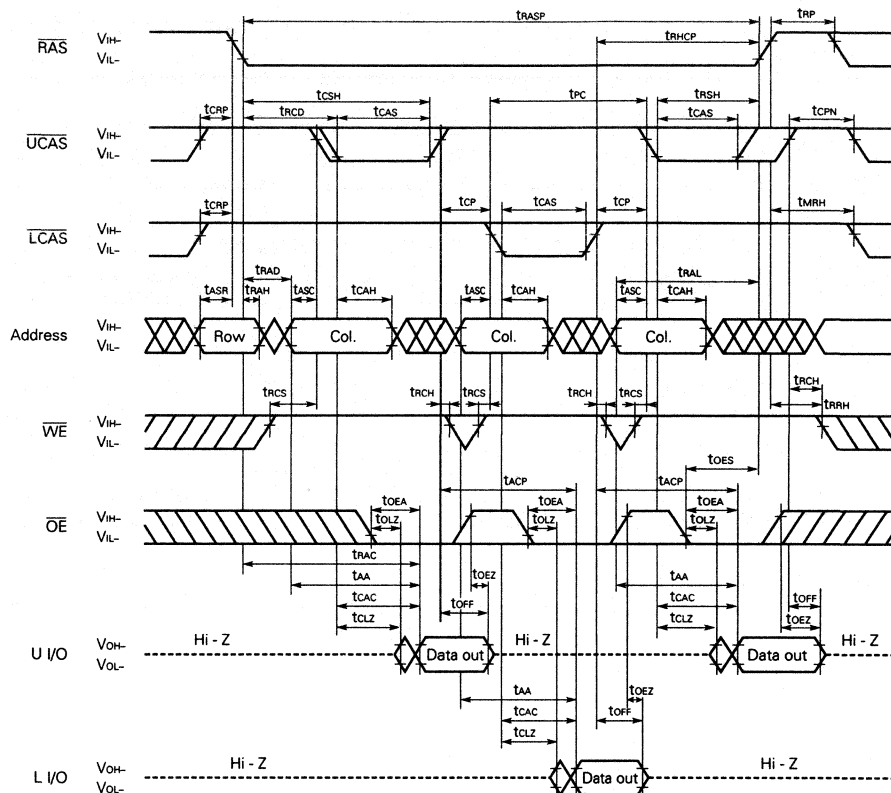
Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Byte Read Cycle

★



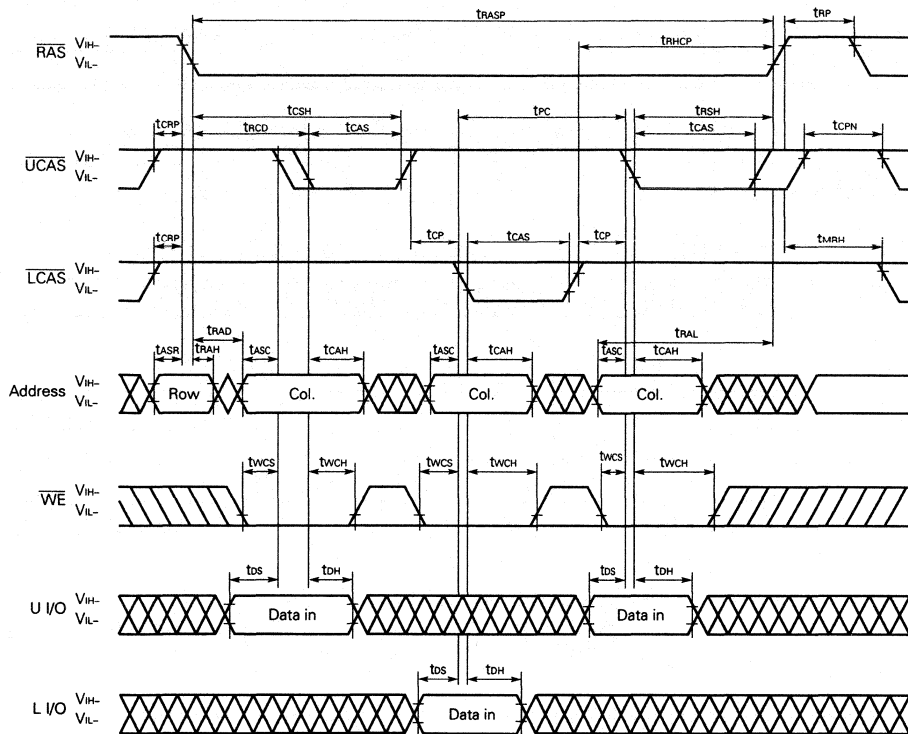
Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

[illegible]

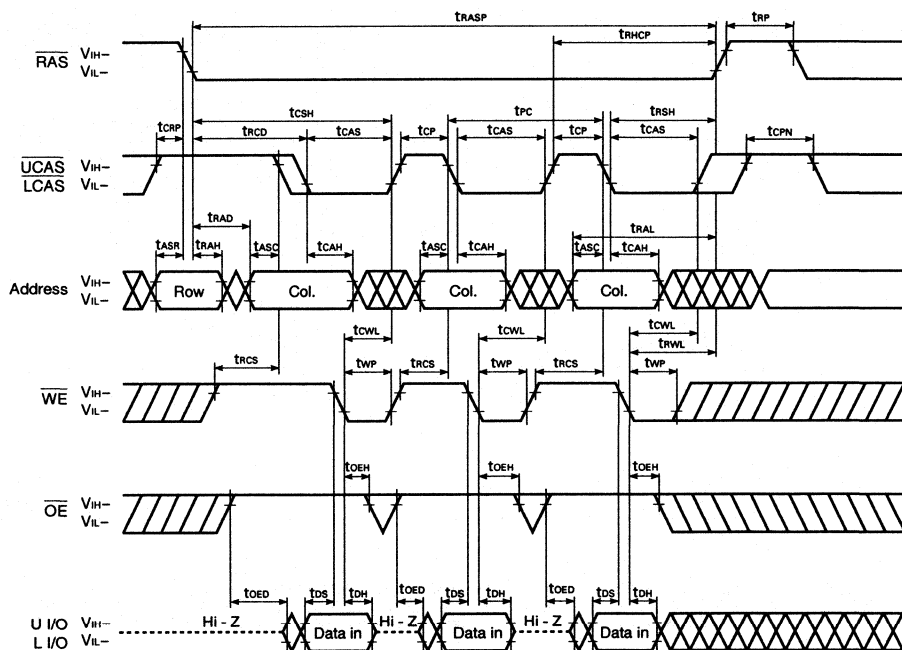
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Byte Early Write Cycle

**Remarks** 1. $\overline{OE}$: Don't care

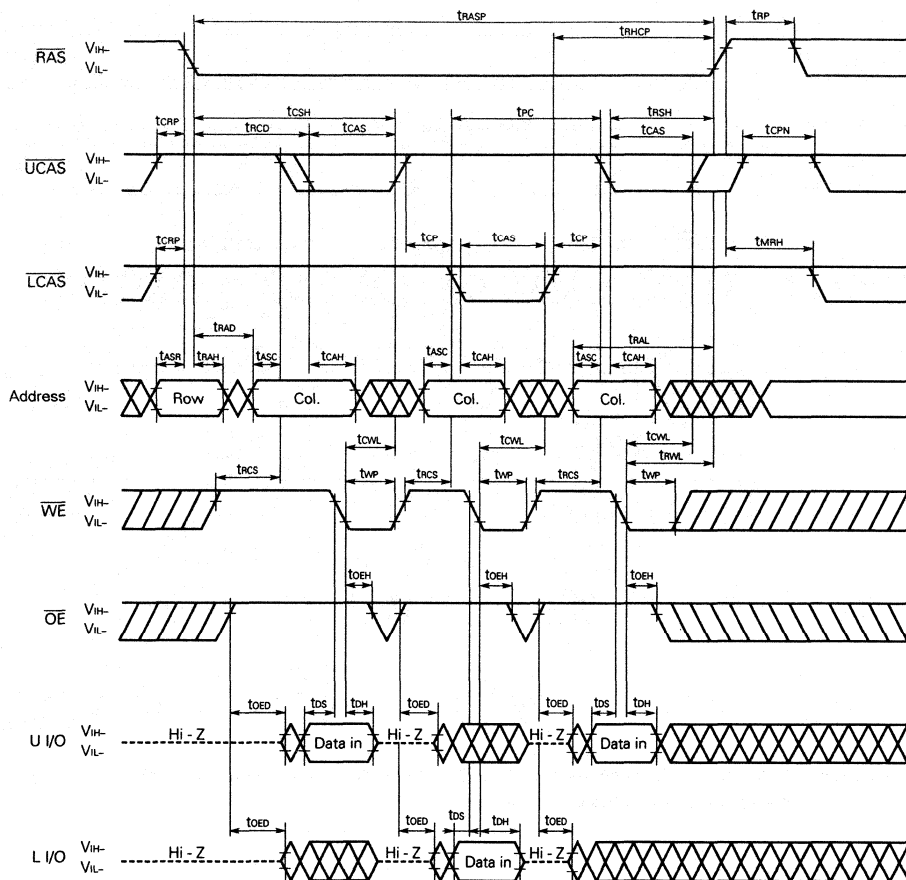
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

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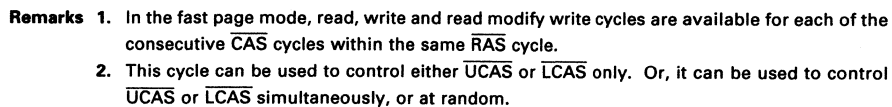
Remarks

1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.
2. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

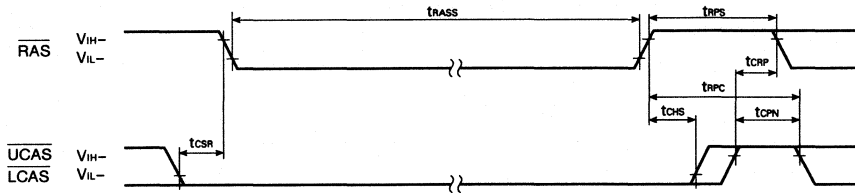
[illegible]

650

★



$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh Cycle (Only for the μ PD42S4260)



Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

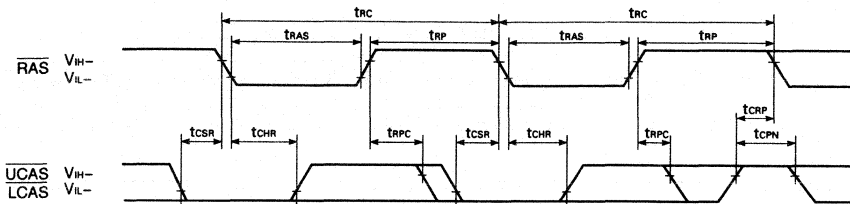
Cautions on Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh can be used independently when used in combination with distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh; However, when used in combination with burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh or with long $\overline{\text{RAS}}$ only refresh (both distributed and burst), the following cautions must be observed.

- (1) **Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Burst $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Long Refresh**
When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh are used in combination, please perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh 512 times within an 8 ms interval just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.
- (2) **Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Long $\overline{\text{RAS}}$ Only Refresh**
When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and $\overline{\text{RAS}}$ only refresh are used in combination, please perform $\overline{\text{RAS}}$ only refresh 512 times within an 8 ms interval just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

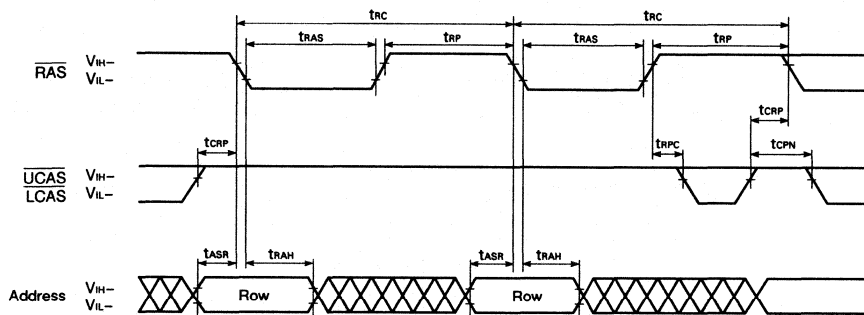
For details, please refer to **How to use DRAM User's Manual**.

CAS Before RAS Refresh Cycle



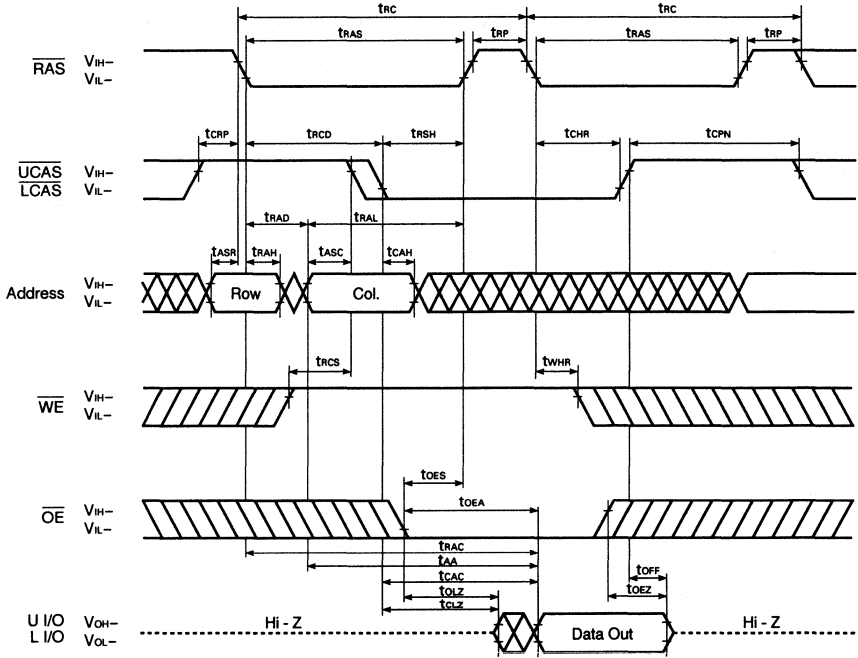
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

RAS Only Refresh Cycle

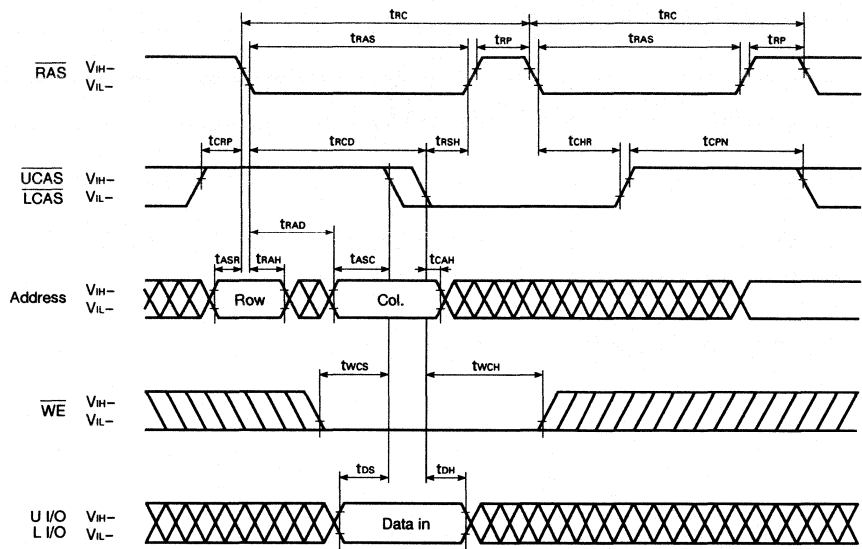


Remark $\overline{WE}, \overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



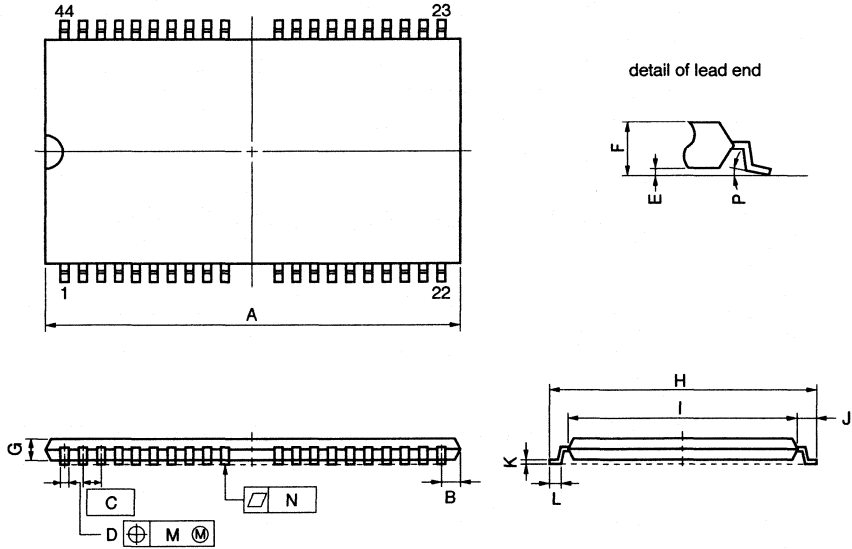
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

★ Package Drawings

44 PIN PLASTIC TSOP(II) (400 mil)

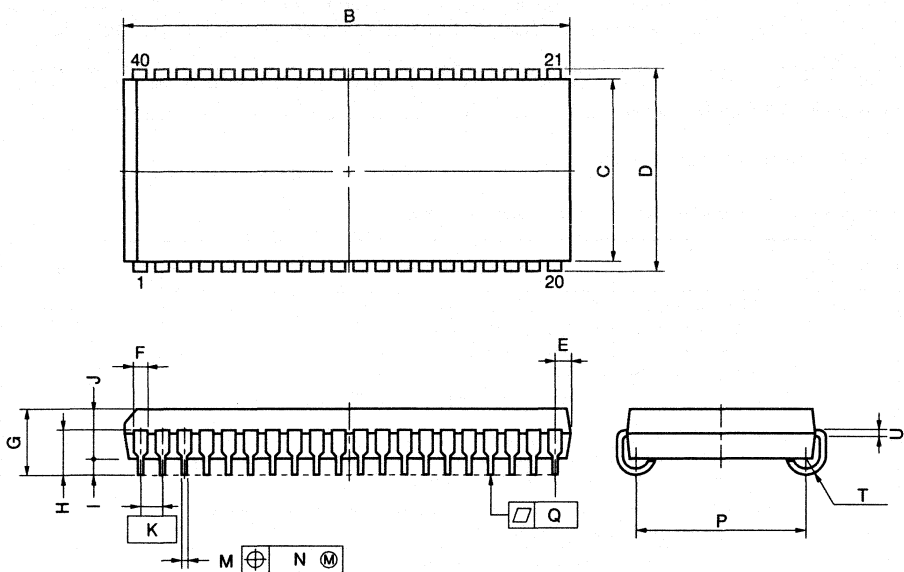


NOTE
 Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 ^{+0.09} _{-0.07}	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004
P	3°+7° -3°	3°+7° -3°

S44G5-80-7JF4

40 PIN PLASTIC SOJ (400 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	26.29 ^{+0.2} _{-0.35}	1.035 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.7	0.028
G	3.5±0.2	0.138±0.008
H	2.4±0.2	0.094 ^{+0.009} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.40±0.20	0.370±0.008
Q	0.15	0.006
T	R0.85	R0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

P40LE-400A-2

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met when soldering μPD42S4260, 424260.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S4260G5, 424260G5: 44-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S4260LE, 424260LE: 40-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days^{Note} (20 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days^{Note} (20 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

MOS INTEGRATED CIRCUIT

μ PD42S4210A, 424210A

4 M-BIT DYNAMIC RAM

256 K-WORD BY 16-BIT, HYPER PAGE MODE, BYTE READ/WRITE MODE

Description

The μ PD42S4210A, 424210A are 262 144 words by 16 bits dynamic CMOS RAMs with optional hyper page mode.

Hyper page mode is a kind of the page mode and is useful for the read operation.

The μ PD42S4210A, 424210A are packed in 44-pin plastic TSOP(II) and 40-pin plastic SOJ.

Features

- Hyper page mode
- 262 144 words by 16 bits organization
- Single +5.0 V $\pm$ 10 % power supply

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μ PD42S4210A-50, 424210A-50	50 ns	84 ns	20 ns
μ PD42S4210A-60, 424210A-60	60 ns	104 ns	25 ns
μ PD42S4210A-70, 424210A-70	70 ns	124 ns	30 ns

- The μ PD42S4210A can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh
μ PD42S4210A	512 cycles / 128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD424210A	512 cycles / 8 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh

The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD42S4210AG5-50-7JF	50 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S4210AG5-60-7JF	60 ns		
μPD42S4210AG5-70-7JF	70 ns		
μPD42S4210AG5-50-7KF	50 ns	44-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD42S4210AG5-60-7KF	60 ns		
μPD42S4210AG5-70-7KF	70 ns		
μPD42S4210ALE-50	50 ns	40-pin Plastic SOJ (400 mil)	
μPD42S4210ALE-60	60 ns		
μPD42S4210ALE-70	70 ns		
μPD424210AG5-50-7JF	50 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD424210AG5-60-7JF	60 ns		
μPD424210AG5-70-7JF	70 ns		
μPD424210AG5-50-7KF	50 ns	44-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD424210AG5-60-7KF	60 ns		
μPD424210AG5-70-7KF	70 ns		
μPD424210ALE-50	50 ns	40-pin Plastic SOJ (400 mil)	
μPD424210ALE-60	60 ns		
μPD424210ALE-70	70 ns		

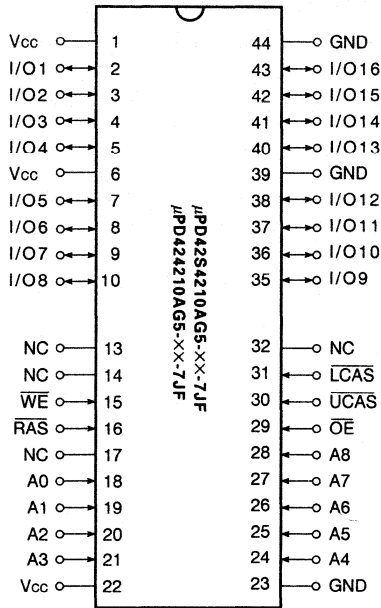
Quality Grade

Standard

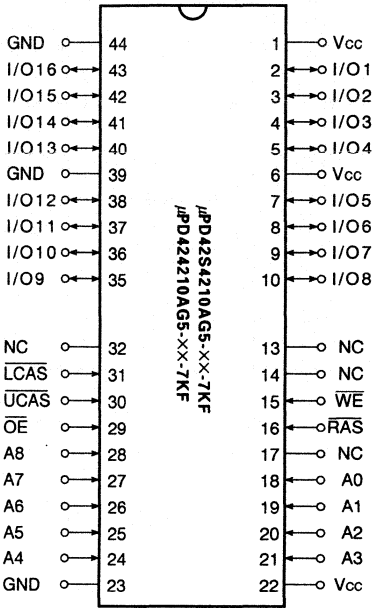
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking Side)

44-pin Plastic TSOP (II)
(400 mil)

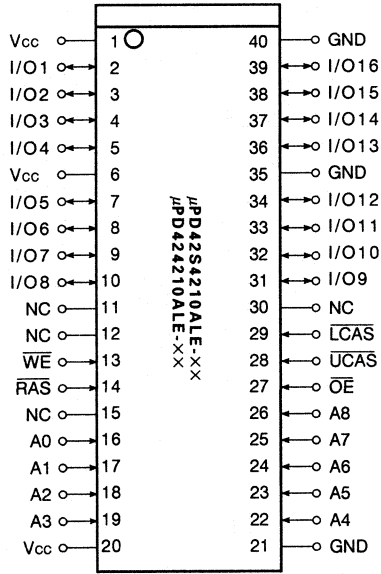


Reverse bent



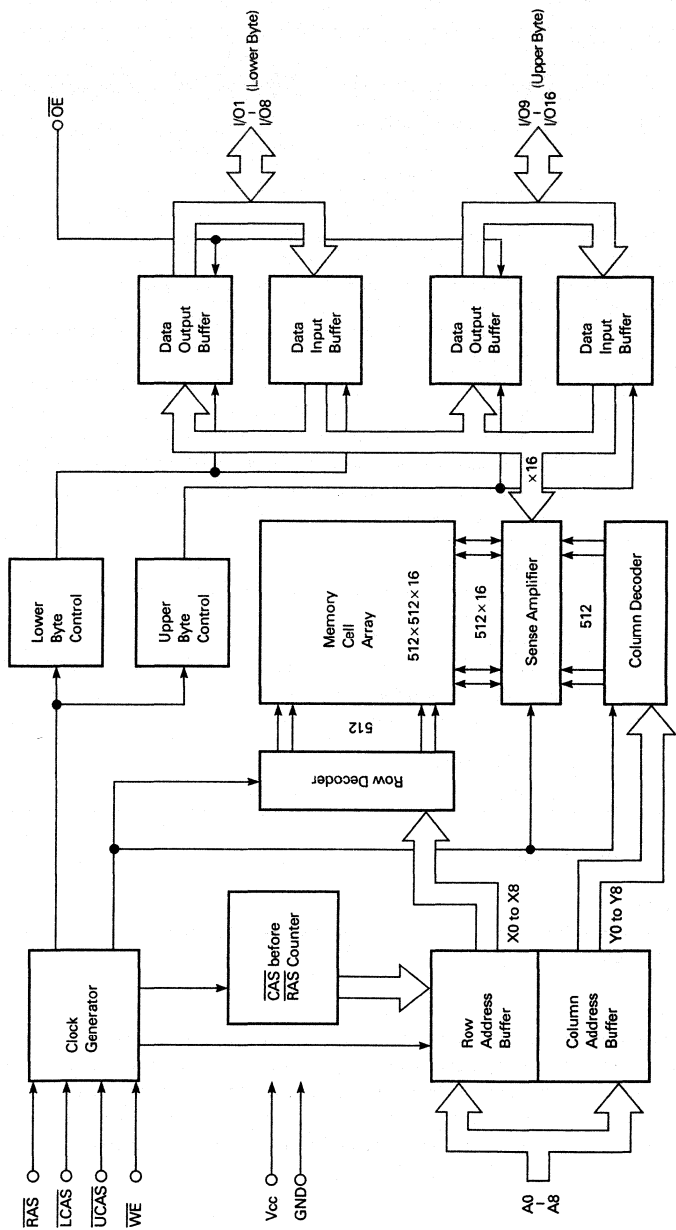
- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{UCAS}}$: Column Address Strobe (upper)
- $\overline{\text{LCAS}}$: Column Address Strobe (lower)
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

40-pin Plastic SOJ
(400 mil)



- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
- LCAS : Column Address Strobe (lower)
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S4210A, 424210A have input pins $\overline{RAS}$, $\overline{CAS}$ ^{Note}, $\overline{WE}$, $\overline{OE}$, A0 to A8 and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address inputs)	Input	9-bit address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 262 144-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t _{ASR} , t _{ASC}) and hold time (t _{RAH} , t _{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

In the hyper page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

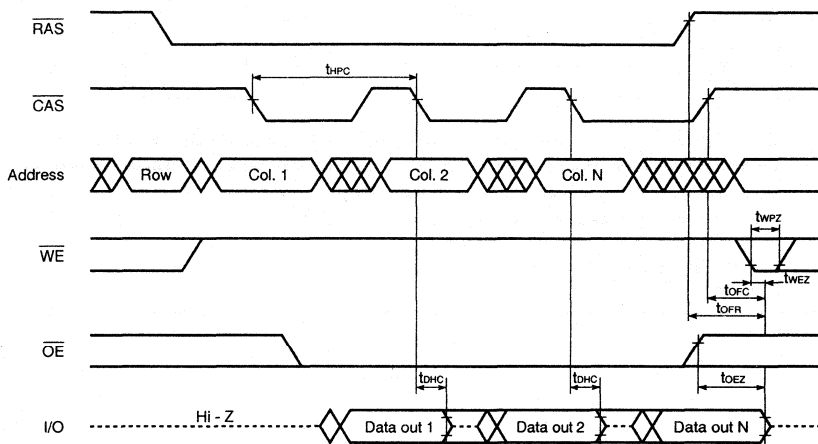
2. The $\overline{\text{CAS}}$ cycle time in the hyper page mode is shorter than that in the fast page mode.

In the hyper page mode, due to the data extend function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{\text{CAS}}$ cycle time in the hyper page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{\text{RAS}}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

Hyper Page Mode Read Cycle



To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.

- (1) $\overline{\text{RAS}}$, $\overline{\text{CAS}}$: inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

- (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$: active, $\overline{\text{OE}}$: active... t_{WEZ} , t_{WPZ} are effective.

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: inactive... t_{OEZ} is effective.

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

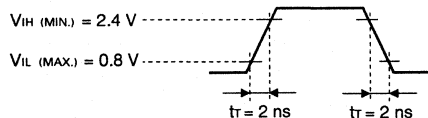
Parameter		Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		90	mA	1, 2, 3
				$\text{trac} = 60 \text{ ns}$		80		
				$\text{trac} = 70 \text{ ns}$		70		
Standby current	μ PD42S4210A	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), \text{I}_\text{O} = 0 \text{ mA}$			2	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, \text{I}_\text{O} = 0 \text{ mA}$			0.15		
	μ PD424210A		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), \text{I}_\text{O} = 0 \text{ mA}$			2		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, \text{I}_\text{O} = 0 \text{ mA}$			1		
RAS only refresh current		I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.}), \text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		90	mA	1, 2, 3, 4
				$\text{trac} = 60 \text{ ns}$		80		
				$\text{trac} = 70 \text{ ns}$		70		
Operating current (Hyper page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $\text{thpc} = \text{thpc}(\text{MIN.}), \text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		90	mA	1, 2, 5
				$\text{trac} = 60 \text{ ns}$		80		
				$\text{trac} = 70 \text{ ns}$		70		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		90	mA	1, 2
				$\text{trac} = 60 \text{ ns}$		80		
				$\text{trac} = 70 \text{ ns}$		70		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (512 Cycles / 128 ms, only for the μ PD42S4210A)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : 512 Cycles / 128 ms $\overline{\text{RAS}}, \overline{\text{CAS}}$: $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby : $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : V_{IH} or V_{IL} $\overline{\text{WE}}, \overline{\text{OE}} : V_{\text{IH}}$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{tras} \leq 200 \text{ ns}$		200	μA	1, 2
				$\text{tras} \leq 1 \mu\text{s}$		300		
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for the μ PD42S4210A)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}$: $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $\text{I}_\text{O} = 0 \text{ mA}$			150	μA	2
Input leakage current		I _{I(L)}	$V_{\text{I}} = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10		+10	μA	
Output leakage current		I _{O(L)}	$V_{\text{O}} = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10		+10	μA	
High level output voltage		V _{OH}	$\text{I}_\text{O} = -2.5 \text{ mA}$	2.4			V	
Low level output voltage		V _{OL}	$\text{I}_\text{O} = +2.1 \text{ mA}$			0.4	V	

- Notes**
- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (trc and thpc).
 - Specified values are obtained with outputs unloaded.
 - I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$.
 - I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 - I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

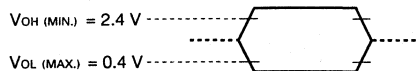
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	trAC = 50 ns		trAC = 60 ns		trAC = 70 ns		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Read / Write Cycle Time	trC	84	–	104	–	124	–	ns		
RAS Precharge Time	trP	30	–	40	–	50	–	ns		
CAS Precharge Time	tCPN	7	–	10	–	10	–	ns		
RAS Pulse Width	trAS	50	10 000	60	10 000	70	10 000	ns		
CAS Pulse Width	tCAS	7	10 000	10	10 000	12	10 000	ns		
RAS Hold Time	trSH	7	–	10	–	12	–	ns		
CAS Hold Time	tCSH	35	–	40	–	50	–	ns		
RAS to CAS Delay Time	trCD	11	37	14	45	14	52	ns	1	
RAS to Column Address Delay Time	trAD	9	25	12	30	12	35	ns	1	
CAS to RAS Precharge Time	tCRP	5	–	5	–	5	–	ns	2	
Row Address Setup Time	tASR	0	–	0	–	0	–	ns		
Row Address Hold Time	trAH	7	–	10	–	10	–	ns		
Column Address Setup Time	tASC	0	–	0	–	0	–	ns		
Column Address Hold Time	tCAH	7	–	10	–	12	–	ns		
OE Lead Time Referenced to RAS	toES	0	–	0	–	0	–	ns		
CAS to Data Setup Time	tCLZ	0	–	0	–	0	–	ns		
OE to Data Setup Time	toLZ	0	–	0	–	0	–	ns		
OE to Data Delay Time	toED	10	–	13	–	15	–	ns		
Masked Byte Write Hold Time Referenced to RAS	tMRH	0	–	0	–	0	–	ns		
Transition Time (Rise and Fall)		trT	1	50	1	50	1	50	ns	
Refresh Time	μPD42S4210A	trEF	–	128	–	128	–	128	ms	3
	μPD424210A		–	8	–	8	–	8	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{RAC} (MAX.)$	$t_{RAC} (MAX.)$
$t_{RAD} > t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{AA} (MAX.)$	$t_{RAD} + t_{AA} (MAX.)$
$t_{RCD} > t_{RCD} (MAX.)$	$t_{CAC} (MAX.)$	$t_{RCD} + t_{CAC} (MAX.)$

$t_{RAD}(MAX.)$ and $t_{RCD}(MAX.)$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}(MAX.)$ and $t_{RCD} \geq t_{RCD}(MAX.)$ will not cause any operation problems.

- $t_{CRP}(MIN.)$ requirement is applied to RAS, CAS cycles.
- This specification is applied only to the μPD42S4210A.

Read Cycle

Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from RAS	t_{RAC}	–	50	–	60	–	70	ns	1
Access Time from CAS	t_{CAC}	–	13	–	15	–	18	ns	1
Access Time from Column Address	t_{AA}	–	25	–	30	–	35	ns	1
Access Time from OE	t_{OEA}	–	13	–	15	–	18	ns	
Column Address Lead Time Referenced to RAS	t_{RAL}	25	–	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to RAS	t_{RRH}	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to CAS	t_{RCH}	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from OE	t_{OEZ}	0	10	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{RAC} (MAX.)$	$t_{RAC} (MAX.)$
$t_{RAD} > t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{AA} (MAX.)$	$t_{RAD} + t_{AA} (MAX.)$
$t_{RCD} > t_{RCD} (MAX.)$	$t_{CAC} (MAX.)$	$t_{RCD} + t_{CAC} (MAX.)$

$t_{RAD}(MAX.)$ and $t_{RCD}(MAX.)$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}(MAX.)$ and $t_{RCD} \geq t_{RCD}(MAX.)$ will not cause any operation problems.

- Either $t_{RCH}(MIN.)$ or $t_{RRH}(MIN.)$ should be met in read cycles.
- $t_{OEZ}(MAX.)$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{WAC} = 50 ns		t _{WAC} = 60 ns		t _{WAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	7	–	10	–	10	–	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	7	–	10	–	10	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	7	–	10	–	12	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	7	–	10	–	12	–	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	–	0	–	0	–	ns	
Data-in Setup Time	t _{ds}	0	–	0	–	0	–	ns	3
Data-in Hold Time	t _{dH}	7	–	10	–	10	–	ns	3

- Notes**
1. t_{wp(MIN.)} is applied to late write cycles or read modify write cycles. In early write cycles, t_{twch(MIN.)} should be met.
 2. If t_{twcs} $\geq$ t_{twcs(MIN.)}, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{ds(MIN.)} and t_{dH(MIN.)} are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{WAC} = 50 ns		t _{WAC} = 60 ns		t _{WAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	107	–	133	–	157	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	64	–	77	–	89	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	27	–	32	–	37	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	39	–	47	–	54	–	ns	1

- Note 1.** If t_{twcs} $\geq$ t_{twcs(MIN.)} the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{trwd} $\geq$ t_{trwd(MIN.)}, t_{tcwd} $\geq$ t_{tcwd(MIN.)}, t_{tawd} $\geq$ t_{tawd(MIN.)}, and t_{tcpwd} $\geq$ t_{tcpwd(MIN.)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{HPC}	20	—	25	—	30	—	ns	
RAS Pulse Width	t _{RASP}	50	125 000	60	125 000	70	125 000	ns	
CAS Pulse Width	t _{H_{CAS}}	7	10 000	10	10 000	12	10 000	ns	
CAS Precharge Time	t _{CP}	7	—	10	—	10	—	ns	
Access Time from CAS Precharge	t _{ACP}	—	27	—	35	—	40	ns	
CAS Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	41	—	52	—	59	—	ns	1
RAS Hold Time from CAS Precharge	t _{RHCP}	27	—	35	—	40	—	ns	
Read Modify Write Cycle Time	t _{HPRWC}	52	—	66	—	75	—	ns	
Data Output Hold Time	t _{DHC}	5	—	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{\text{WE}}$	t _{WEZ}	0	10	0	13	0	15	ns	2,3
$\overline{\text{WE}}$ Pulse Width	t _{WPZ}	7	—	10	—	10	—	ns	3
Output Buffer Turn-off Delay from $\overline{\text{RAS}}$	t _{OF_R}	0	10	0	13	0	15	ns	2,3
Output Buffer Turn-off Delay from $\overline{\text{CAS}}$	t _{OF_C}	0	10	0	13	0	15	ns	2,3

- Notes**
1. If $t_{\text{WC}} \geq t_{\text{WC}}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{\text{RW}} \geq t_{\text{RW}}(\text{MIN.})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{MIN.})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{MIN.})$, and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
 2. $t_{\text{OFC}}(\text{MAX.})$, $t_{\text{OFR}}(\text{MAX.})$ and $t_{\text{WEZ}}(\text{MAX.})$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .
 3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on state of each signal.

(1) $\overline{\text{RAS}}$, $\overline{\text{CAS}}$: inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

(2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$: active, $\overline{\text{OE}}$: active ... t_{WEZ} , t_{WPZ} are effective

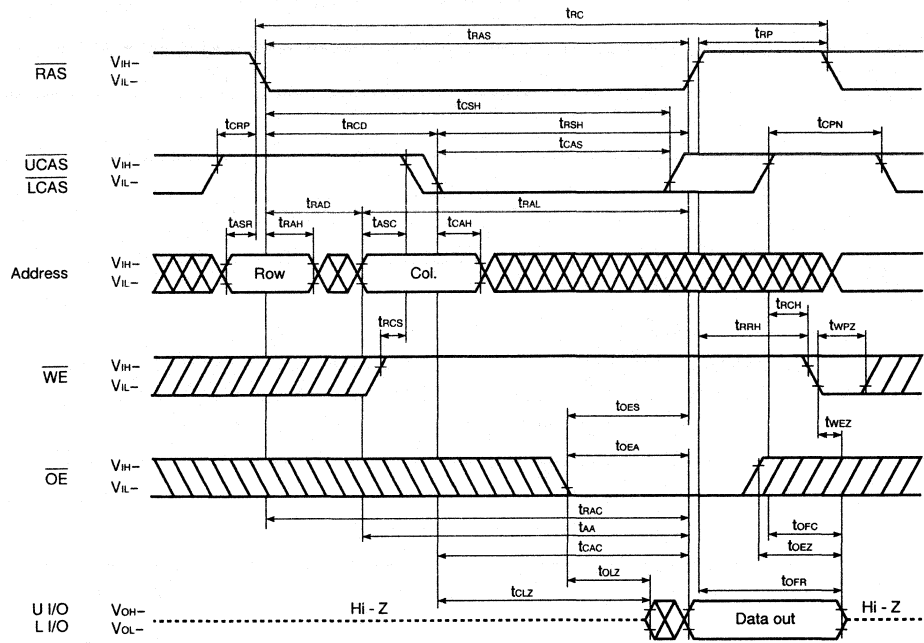
$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: inactive ... t_{OEZ} is effective.

Refresh Cycle

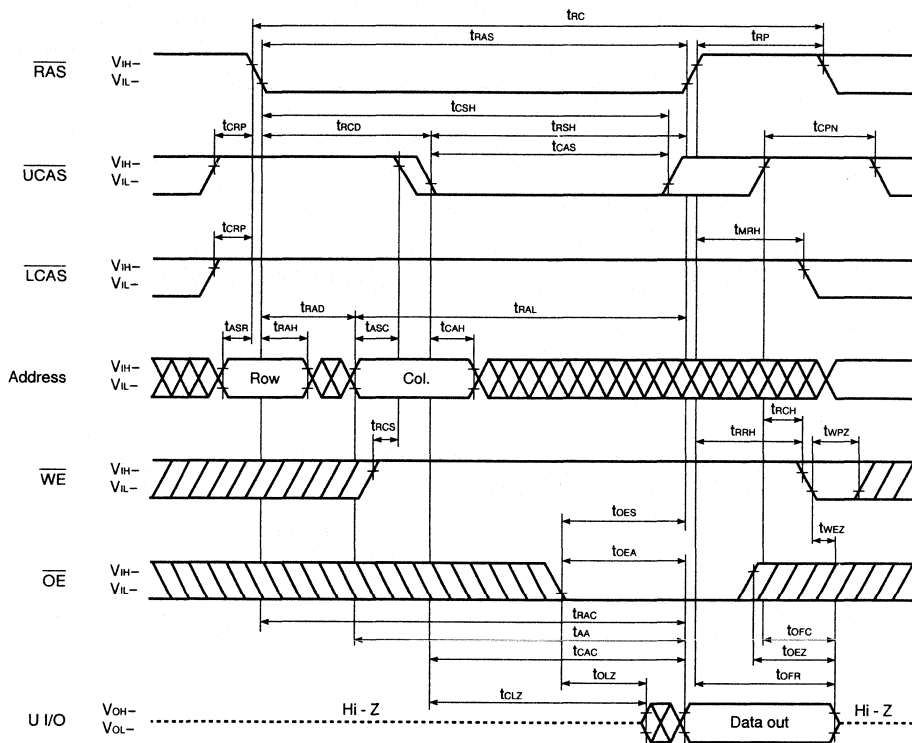
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	–	5	–	5	–	ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10	–	10	–	10	–	ns	
RAS Precharge CAS Hold Time	t _{RPC}	5	–	5	–	5	–	ns	
RAS Pulse Width (CAS before RAS Self Refresh Cycle)	t _{RAS}	100	–	100	–	100	–	μs	1
RAS Precharge Time (CAS before RAS Self Refresh Cycle)	t _{RPS}	90	–	110	–	130	–	ns	1
CAS Hold Time (CAS before RAS Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	–50	–	ns	1
WE Hold Time (Hidden Refresh Cycle)	t _{WHR}	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S4210A.

Read Cycle

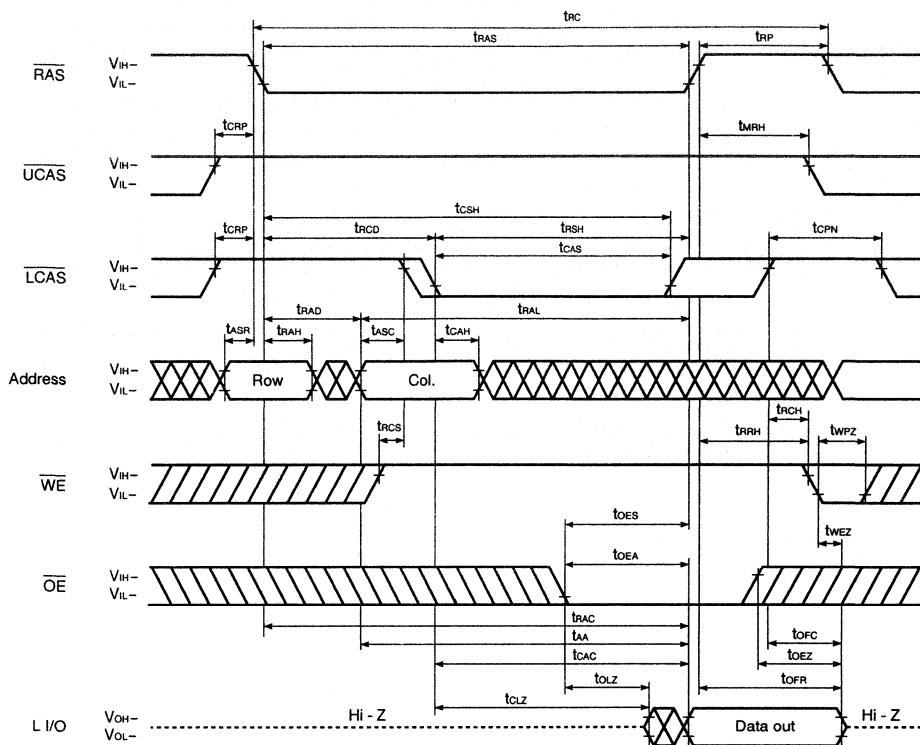


Upper Byte Read Cycle



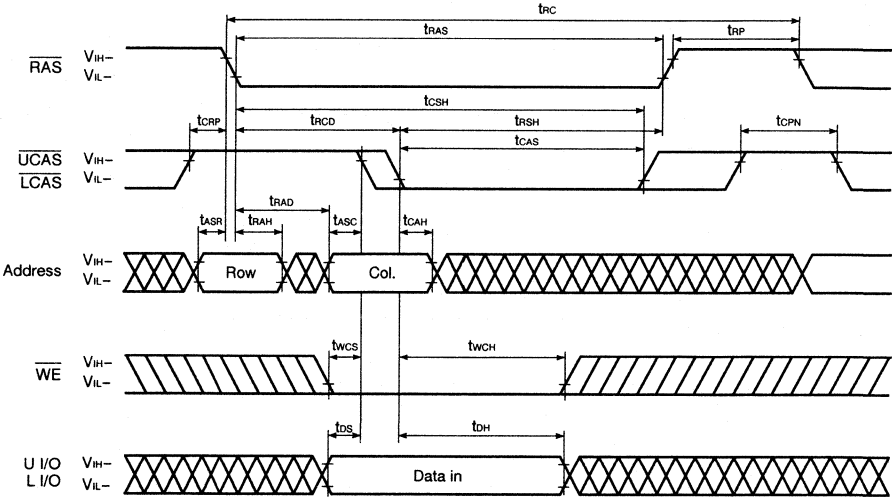
Remark L I/O : Hi-Z

Lower Byte Read Cycle



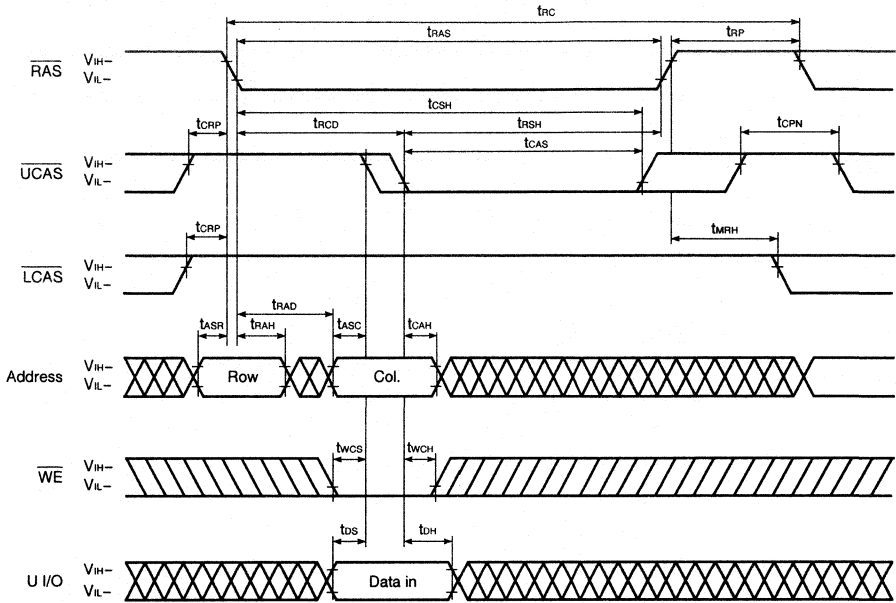
Remark U I/O : Hi-Z

Early Write Cycle



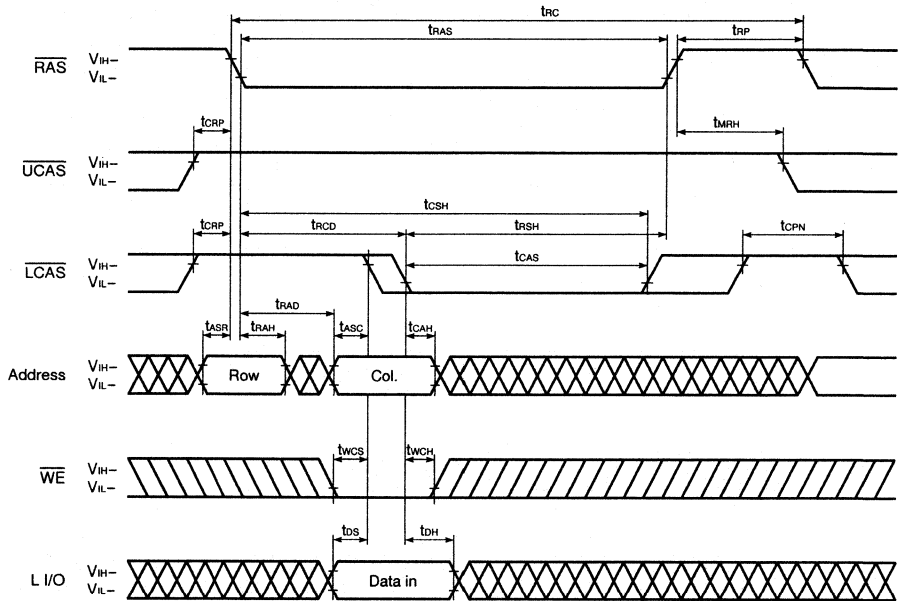
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



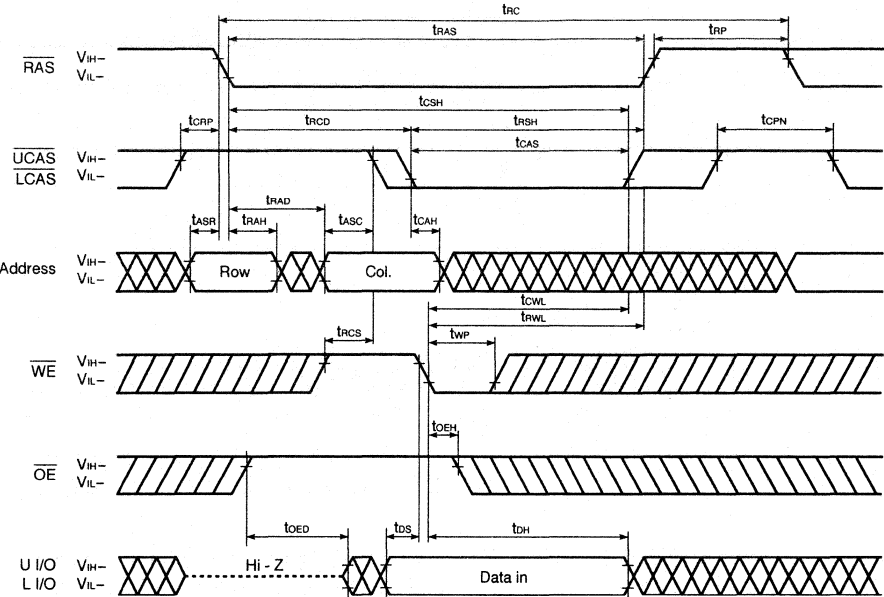
Remark $\overline{\text{OE}}$, L I/O : Don't care

Lower Byte Early Write Cycle

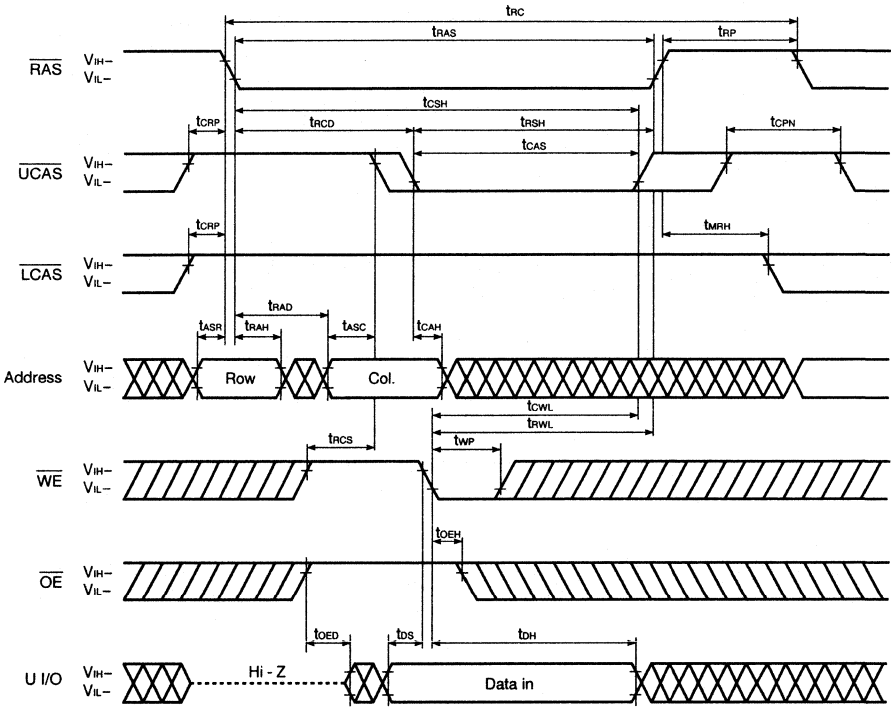


Remark $\overline{OE}$, U I/O : Don't care

Late Write Cycle

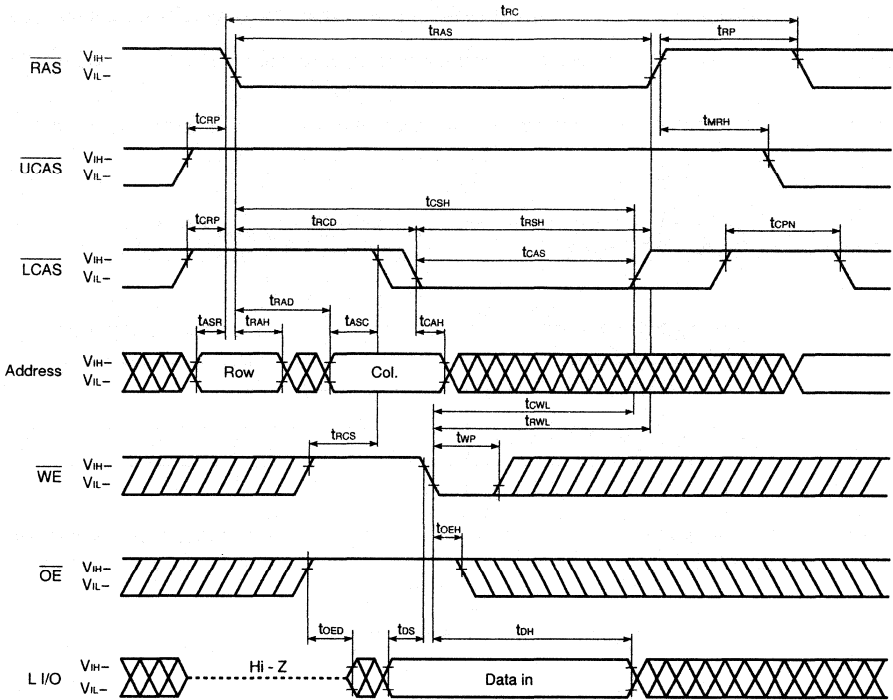


Upper Byte Late Write Cycle



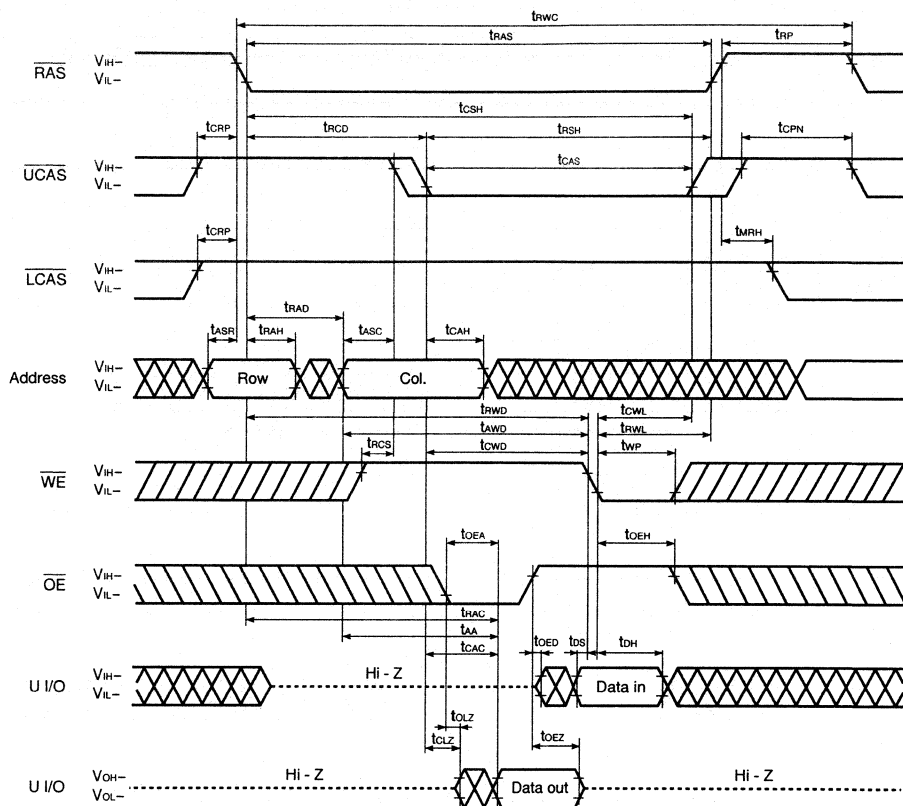
Remark L I/O : Don't care

Lower Byte Late Write Cycle

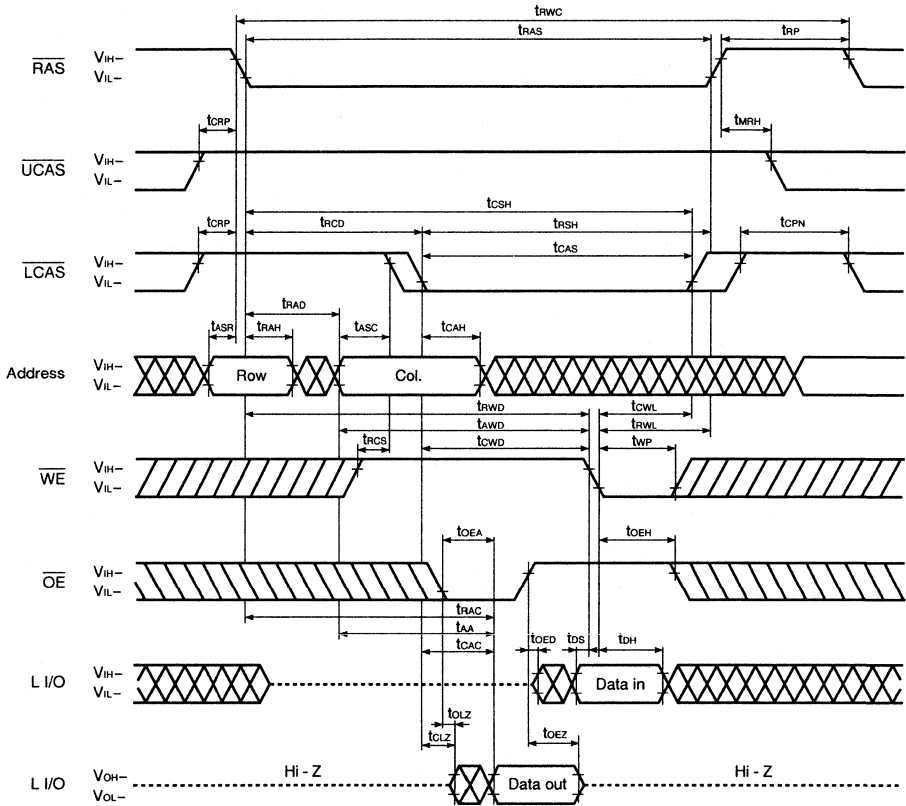


Remark U I/O : Don't care

[illegible]



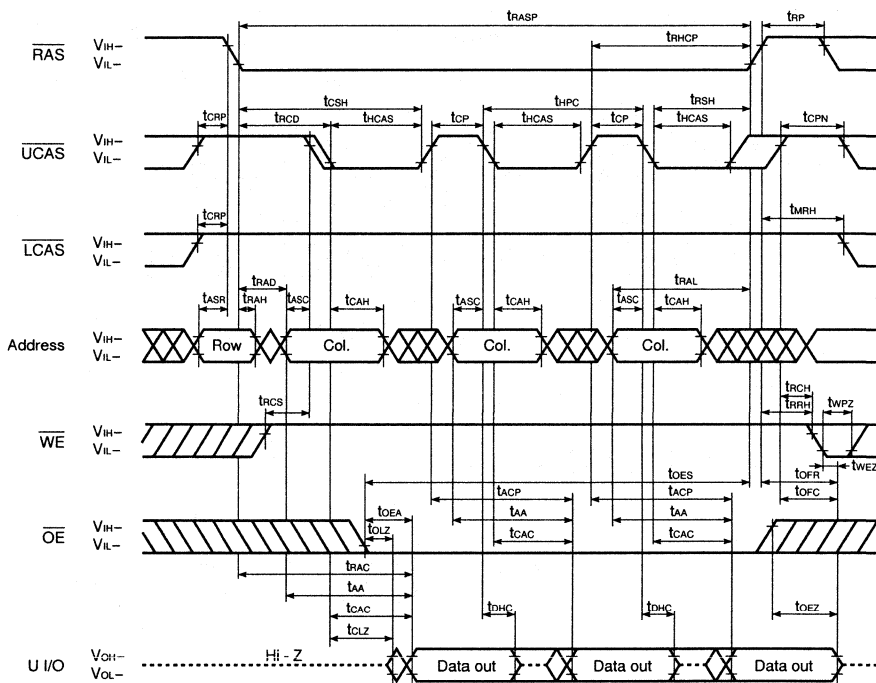
Lower Byte Read Modify Write Cycle



Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

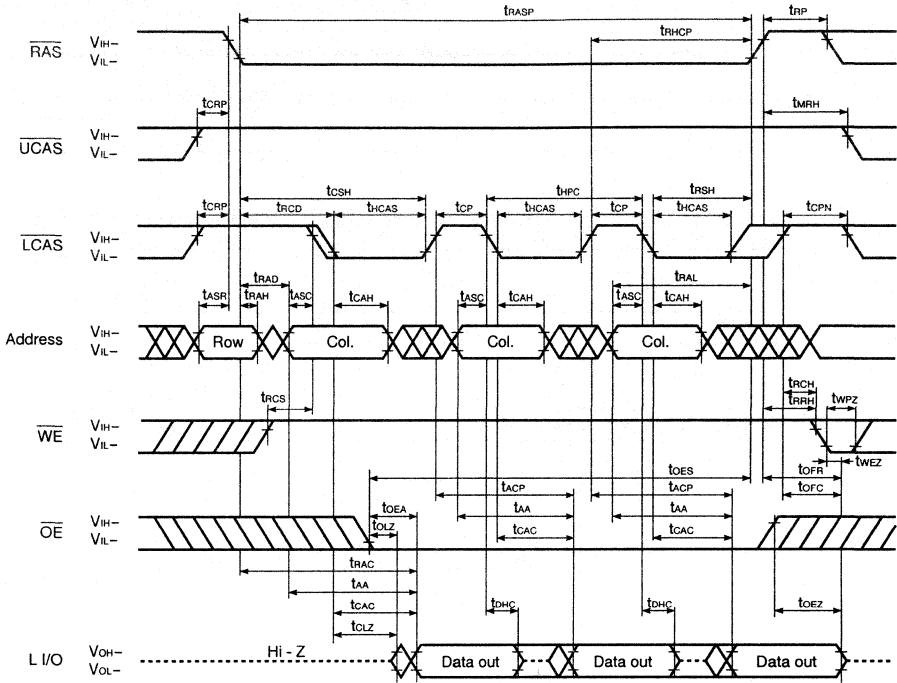
[illegible]

Hyper Page Mode Upper Byte Read Cycle



Remark L I/O : Hi-Z

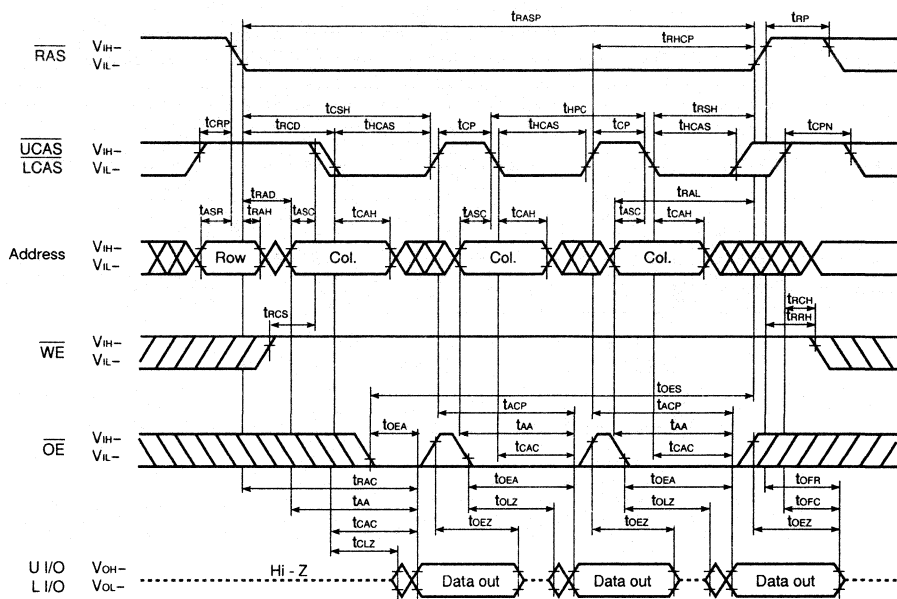
Hyper Page Mode Lower Byte Read Cycle



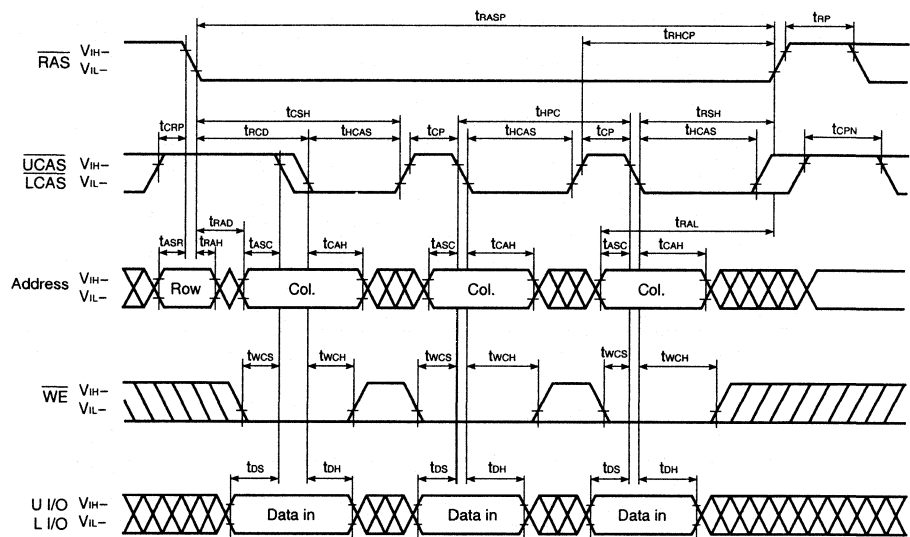
Remark U I/O : Hi-Z

[illegible]

Hyper Page Mode Read Cycle ($\overline{\text{OE}}$ Control)

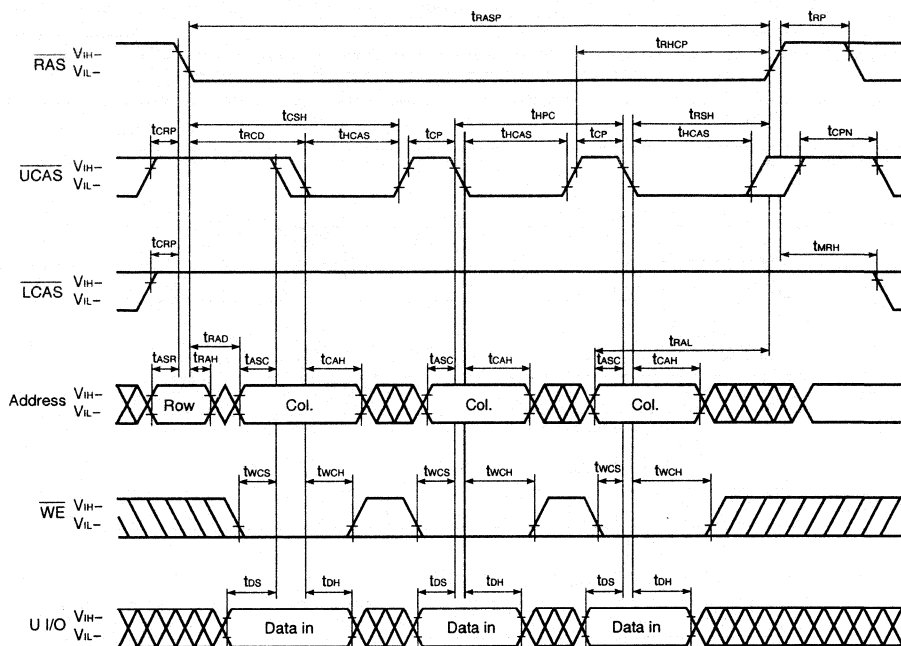


Hyper Page Mode Early Write Cycle



Remark $\overline{OE}$: Don't care

Hyper Page Mode Upper Byte Early Write Cycle

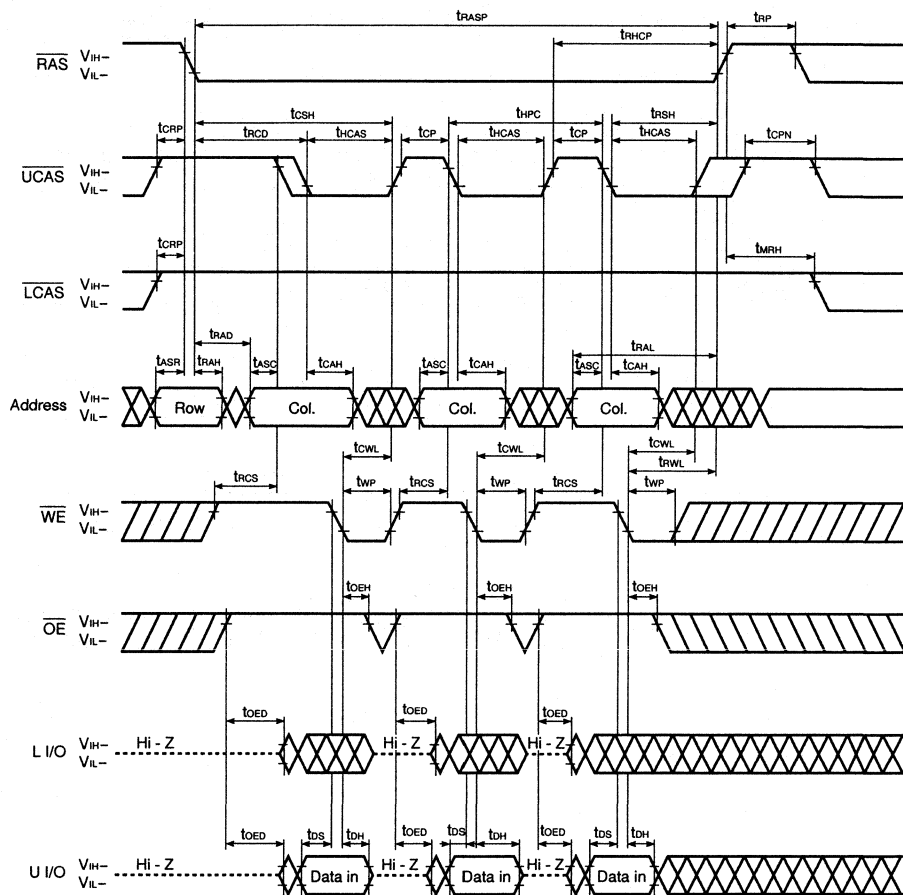


Remark $\overline{OE}$, L I/O : Don't care

[illegible]

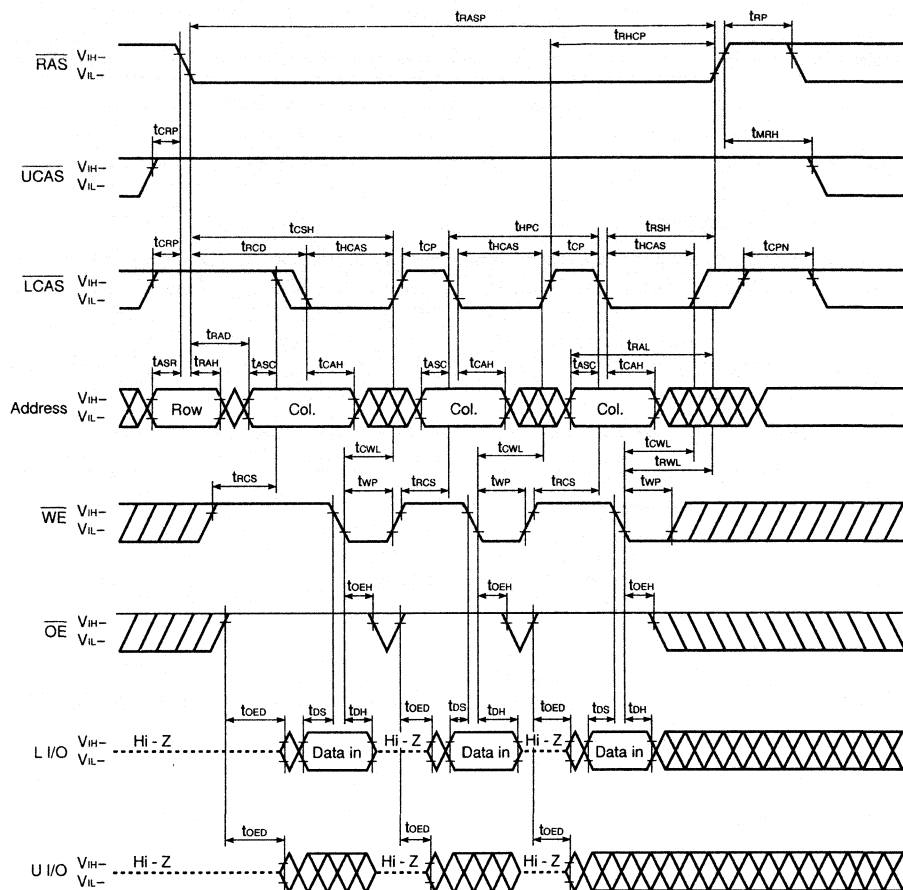
Remark $\overline{OE}$, U I/O : Don't care

Hyper Page Mode Upper Byte Late Write Cycle



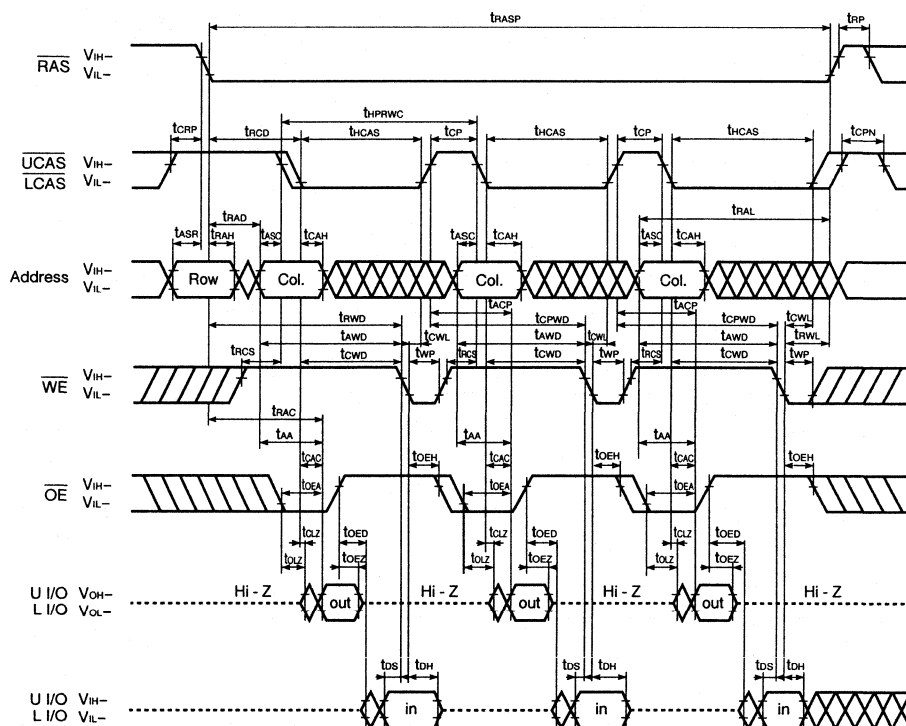
Remark In this cycle, the input data to Lower I/O is ineffective.

Hyper Page Mode Lower Byte Late Write Cycle



Remark In this cycle, the input data to Upper I/O is ineffective.

Hyper Page Mode Read Modify Write Cycle



The timing diagram illustrates the operational sequence of the 74VHC08A. It includes the following signals and parameters:

- RAS**: Row Address Strobe, active low (V_{IH} , V_{IL}). Parameters: t_{RSP} (pulse width), t_{RAS} (setup time before RAS).
- UCAS**: Column Address Strobe, active low (V_{IH} , V_{IL}). Parameters: t_{CRP} (pulse width), t_{CD} (delay from RAS), t_{HPRWC} (high pulse width), t_{CAS} (setup time before UCAS), t_{CP} (pulse width), t_{CAN} (hold time after UCAS), t_{CPN} (fall time), t_{MRH} (maximum rate hold time).
- LCAS**: Local Column Address Strobe, active low (V_{IH} , V_{IL}). Parameter: t_{CRP} (pulse width).
- Address**: Data bus address. Parameters: t_{RAD} (Row Access Delay), t_{RAH} (Row Access Hold), t_{ASC} (Access Setup), t_{CAH} (Column Access Hold), t_{TAD} (Total Access Delay), t_{AL} (Array Latency).
- WE**: Write Enable, active low (V_{IH} , V_{IL}). Parameters: t_{RWL} (Write Enable Low Pulse Width), t_{RDW} (Read Enable Low Pulse Width), t_{CWL} (Write Enable Low Setup), t_{CWD} (Write Enable Low Delay), t_{TRCS} (Refresh Cycle Setup), t_{TRWL} (Write Enable Low Hold), t_{TRWP} (Write Enable Low Pulse Width).
- OE**: Output Enable, active low (V_{IH} , V_{IL}). Parameters: t_{OEH} (Output Enable High Pulse Width), t_{OEA} (Output Enable Active Delay), t_{OLZ} (Output Load Z), t_{OEZ} (Output Load Z), t_{TOEH} (Turn-off Output Enable High), t_{TOEA} (Turn-off Output Enable Active Delay).
- U I/O**: User Input/Output. Parameters: t_{DS} (Data Setup), t_{DH} (Data Hold).
- L I/O**: Local Input/Output. Parameters: t_{DS} (Data Setup), t_{DH} (Data Hold).

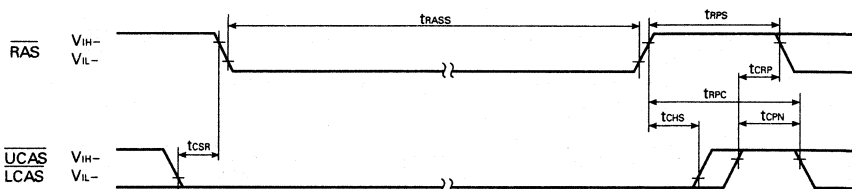
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

The timing diagram illustrates the sequence of signals for the 64K1602 LCD module. The signals and their timing parameters are as follows:

- RAS** (V_{IH} , V_{IL}): Row Address Strobe. Timing parameters: t_{RASP} (pulse width), t_{CRP} (setup time before UCAS), t_{RCD} (delay after UCAS), t_{BPRWC} (pulse width), t_{BPC} (pulse period), t_{BCAS} (delay after LCAS), t_{BPN} (delay before next pulse).
- UCAS** (V_{IH} , V_{IL}): User Command Address Strobe. Timing parameters: t_{CRP} (setup time before RAS), t_{RCD} (delay after RAS), t_{BPRWC} (pulse width), t_{BPC} (pulse period), t_{BCAS} (delay after LCAS), t_{BPN} (delay before next pulse).
- LCAS** (V_{IH} , V_{IL}): Line Command Address Strobe. Timing parameters: t_{CRP} (setup time before RAS), t_{RCD} (delay after RAS), t_{BPRWC} (pulse width), t_{BPC} (pulse period), t_{BCAS} (delay after LCAS), t_{BPN} (delay before next pulse).
- Address** (V_{IH} , V_{IL}): Data Address. Timing parameters: t_{RAD} (setup time before RAS), t_{ASC} (setup time before UCAS), t_{CAH} (setup time before LCAS), t_{LACP} (setup time before RAS), t_{CPWD} (pulse width), t_{CWL} (pulse width), t_{BRS} (pulse width), t_{TWP} (pulse width), t_{RCS} (pulse width), t_{TRW} (pulse width), t_{AWD} (pulse width), t_{CWD} (pulse width), t_{TRWL} (pulse width), t_{TWP} (pulse width).
- WE** (V_{IH} , V_{IL}): Write Enable. Timing parameters: t_{RCD} (delay after RAS), t_{TAA} (pulse width), t_{TAC} (pulse width), t_{TOEA} (pulse width), t_{TOEZ} (pulse width), t_{TOEH} (pulse width).
- OE** (V_{IH} , V_{IL}): Output Enable. Timing parameters: t_{RCD} (delay after RAS), t_{TAA} (pulse width), t_{TAC} (pulse width), t_{TOEA} (pulse width), t_{TOEZ} (pulse width), t_{TOEH} (pulse width).
- L I/O** (V_{OH} , V_{OL}): Low Data Input/Output. Timing parameters: t_{TOS} (pulse width), t_{TSH} (pulse width), t_{TDS} (pulse width), t_{TDS} (pulse width), t_{TDS} (pulse width).
- U I/O** (V_{IH} , V_{IL}): User Data Input/Output. Timing parameters: t_{TOS} (pulse width), t_{TSH} (pulse width), t_{TDS} (pulse width), t_{TDS} (pulse width), t_{TDS} (pulse width).

Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

CAS Before RAS Self Refresh Cycle (Only for the μPD42S4210A)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

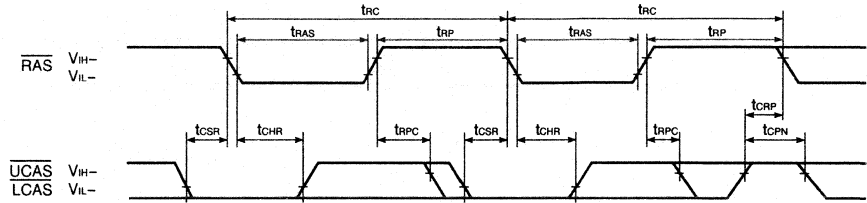
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 512 times within a 8 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh 512 times within a 8 ms interval just before and after setting CAS before RAS self refresh.

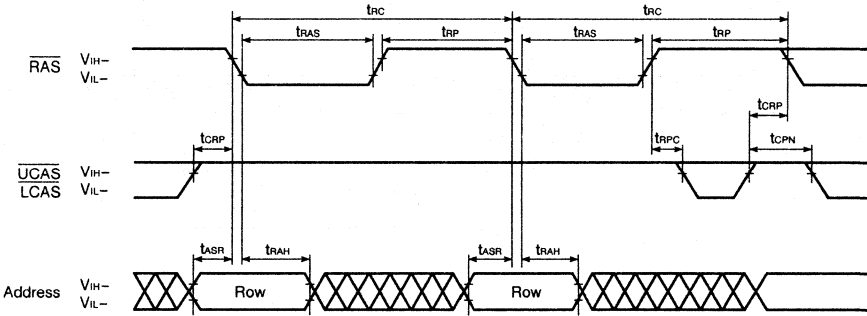
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



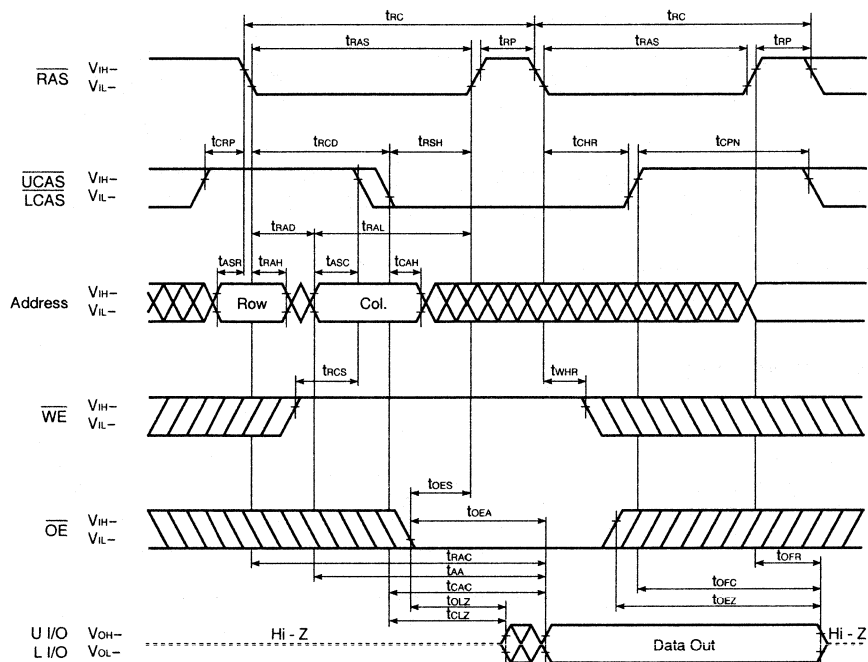
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

RAS Only Refresh Cycle

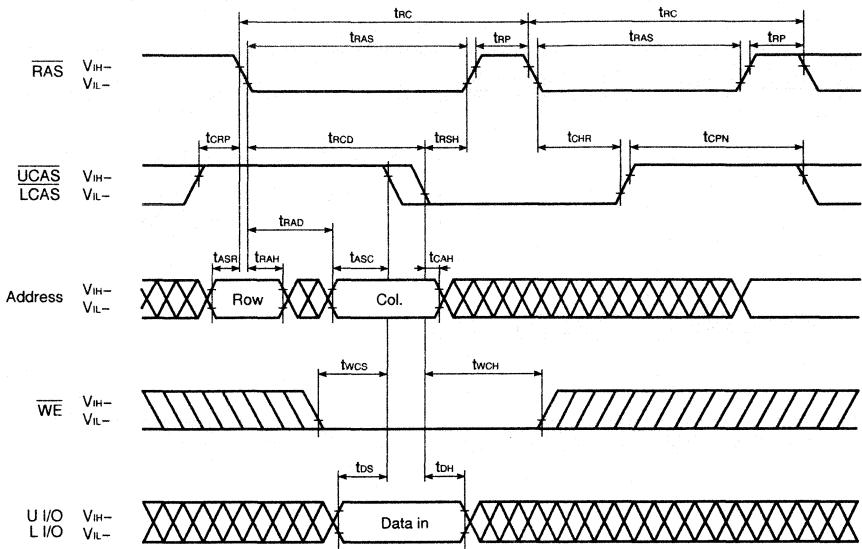


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Hidden Refresh Cycle (Read)



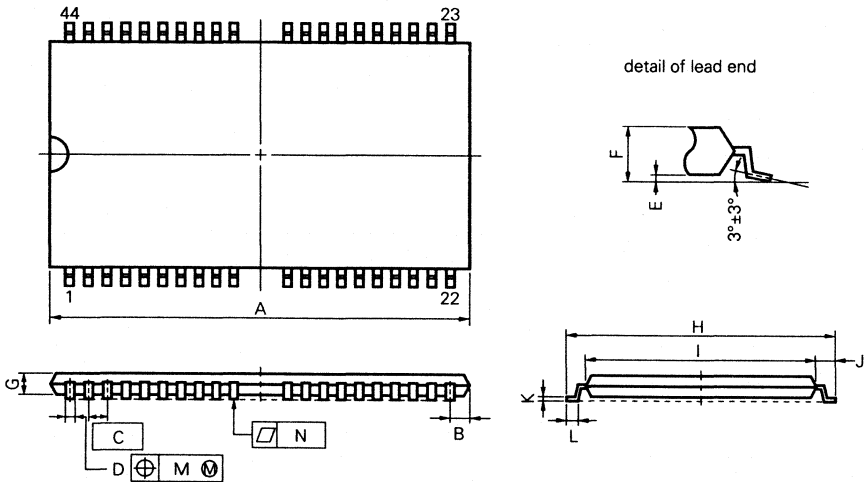
Hidden Refresh Cycle (Write)



Remark OE : Don't care

Package Drawings

44 PIN PLASTIC TSOP(II) (400 mil)



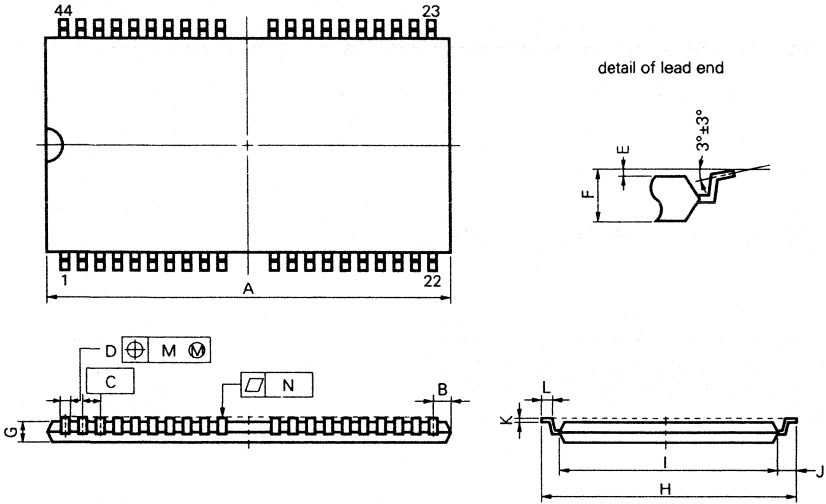
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S44G5-80-7JF-1

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004

44 PIN PLASTIC TSOP(II) (400 mil)

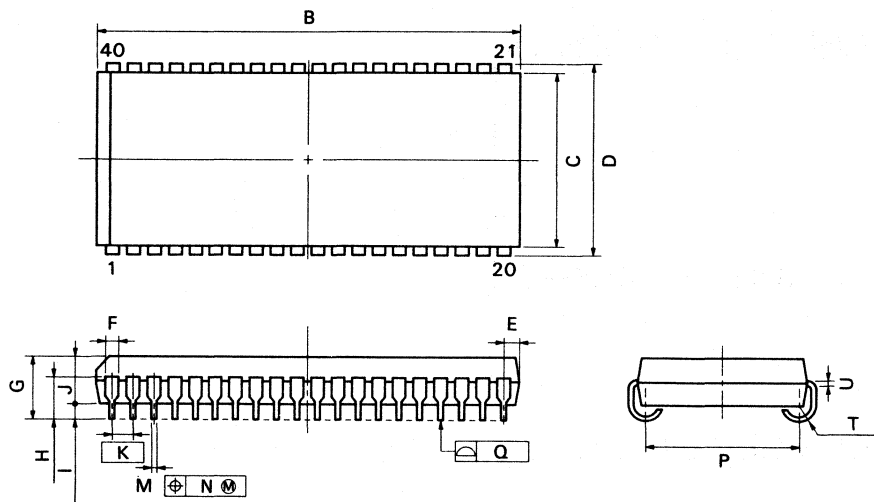


NOTE
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S44G5-80-7KF-1

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004

40PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P40LE-400A-1

ITEM	MILLIMETERS	INCHES
B	26.29 ^{+0.2} _{-0.35}	1.035 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.7	0.028
G	3.5±0.2	0.138±0.008
H	2.4±0.2	0.094 ^{+0.009} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.15	0.006
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD42S4210A, 424210A.

Types of Surface Mount Device

μ PD42S4210AG5-XX-7JF, 424210AG5-XX-7JF : 44-pin Plastic TSOP (II) (400 mil)

μ PD42S4210AG5-XX-7KF, 424210AG5-XX-7KF : 44-pin Plastic TSOP (II) (400 mil) Reverse bent

μ PD42S4210ALE-XX, 424210ALE-XX : 40-pin Plastic SOJ (400 mil)

4M Dynamic RAM

[3.3V $\pm$ 0.3V]



MOS INTEGRATED CIRCUIT

μ PD42S4400L, 424400L

3.3 V OPERATION 4 M-BIT DYNAMIC RAM 1 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μ PD42S4400L, 424400L are 1,048,576 words by 4 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

Besides, the μ PD42S4400L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

These are packaged in 26-pin plastic TSOP(III) and 26-pin plastic SOJ.

Features

- 1,048,576 words by 4 bits organization
- Single +3.3 V $\pm$ 0.3 V power supply
- Fast page mode
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S4400L-A60, 424400L-A60	288 mW	60 ns	120 ns	40 ns
μ PD42S4400L-A70, 424400L-A70	252 mW	70 ns	130 ns	45 ns
μ PD42S4400L-A80, 424400L-A80	216 mW	80 ns	150 ns	50 ns
μ PD42S4400L-A10, 424400L-A10	180 mW	100 ns	180 ns	60 ns

- The μ PD42S4400L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S4400L	1,024 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	0.36 mW (CMOS level input)
μ PD424400L	1,024 cycles/16 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

- Multiplexed address inputs Row address: A0-A9, Column address: A0-A9

The information in this document is subject to change without notice.

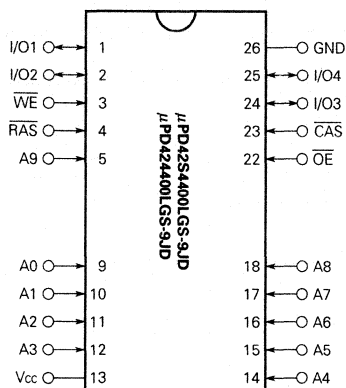
The mark ★ shows revised points.

★ Ordering Information

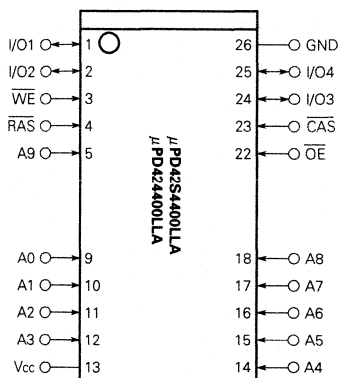
Part number	Access time (MAX.)	Package	Refresh
μPD42S4400LGS-A60-9JD	60 ns	26-pin Plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh
μPD42S4400LGS-A70-9JD	70 ns		$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
μPD42S4400LGS-A80-9JD	80 ns		$\overline{\text{RAS}}$ only refresh
μPD42S4400LGS-A10-9JD	100 ns		Hidden refresh
μPD42S4400LLA-A60	60 ns	26-pin Plastic SOJ (300 mil)	
μPD42S4400LLA-A70	70 ns		
μPD42S4400LLA-A80	80 ns		
μPD42S4400LLA-A10	100 ns		
μPD424400LGS-A60-9JD	60 ns	26-pin Plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
μPD424400LGS-A70-9JD	70 ns		$\overline{\text{RAS}}$ only refresh
μPD424400LGS-A80-9JD	80 ns		Hidden refresh
μPD424400LGS-A10-9JD	100 ns		
μPD424400LLA-A60	60 ns	26-pin Plastic SOJ (300 mil)	
μPD424400LLA-A70	70 ns		
μPD424400LLA-A80	80 ns		
μPD424400LLA-A10	100 ns		

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)

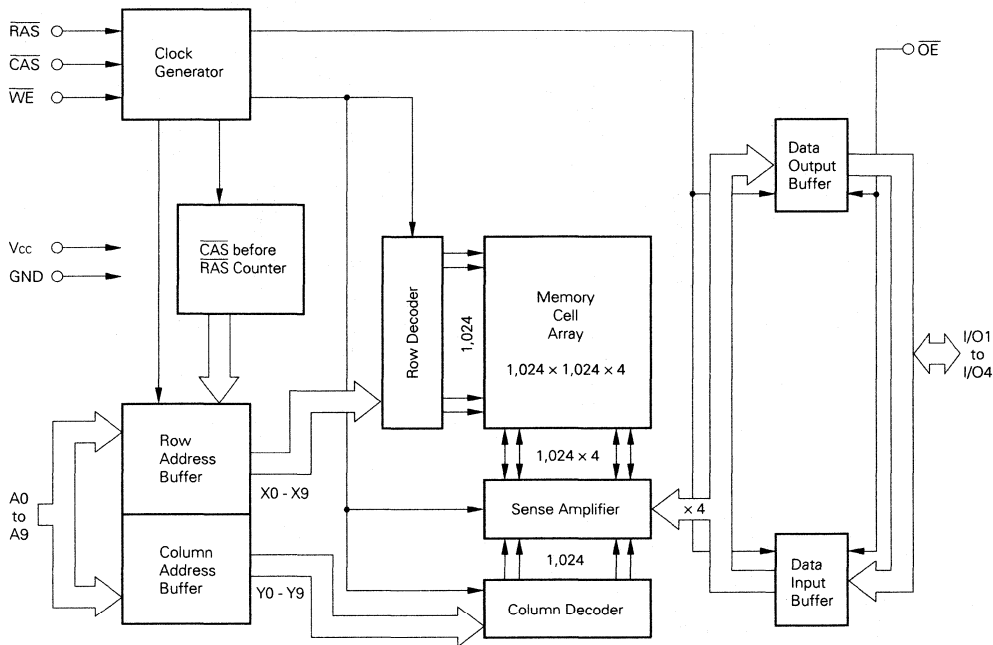


26-pin Plastic SOJ (300 mil)



- A0 to A9 : Address Inputs
- I/O1 to I/O4 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground

Block Diagram



Input/Output Pin Functions

The μPD42S4400L, 424400L have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A9 and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. CAS before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address inputs)	Input	Address bus. Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{Stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	RAS, CAS, WE, OE			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling trc = trc (MIN.) I _O = 0 mA	trac = 60 ns		80	mA	1, 2, 3
				trac = 70 ns		70		
				trac = 80 ns		60		
				trac = 100 ns		50		
Standby current	μPD42S4400L	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$			0.5	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$			0.1		
	μPD424400L		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$			2.0		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$			0.5		
RAS only refresh current		I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ trc = trc (MIN.), I _O = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns trac = 100 ns		80 70 60 50	mA	1, 2, 3, 4
Operating current (Fast page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling tpc = tpc (MIN.), I _O = 0 mA	trac = 60 ns		70	mA	1, 2, 5
				trac = 70 ns		60		
				trac = 80 ns		50		
				trac = 100 ns		40		
CAS before RAS refresh current		I _{CC5}	$\overline{\text{RAS}}$ Cycling trc = trc (MIN.) I _O = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns trac = 100 ns		80 70 60 50	mA	1, 2
CAS before RAS long refresh current (1,024 Cycles / 128 ms, only for the μPD42S4400L)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : trc = 125.0 μs $\overline{\text{RAS}}, \overline{\text{CAS}} :$ V _{CC} - 0.2 V ≤ V _{IH} ≤ V _{IH(MAX.)} 0 V ≤ V _{IL} ≤ 0.2 V Standby : RAS, CAS ≥ V _{CC} - 0.2 V Address : V _{IH} or V _{IL} WE, OE: V _{IH} I _O = 0 mA	trās ≤ 200 ns		100	μA	1, 2
				trās ≤ 1 μs		150	μA	1, 2
CAS before RAS self refresh current (only for the μPD42S4400L)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}} :$ trās = 5 ms V _{CC} - 0.2 V ≤ V _{IH} ≤ V _{IH(MAX.)} 0 V ≤ V _{IL} ≤ 0.2 V I _O = 0 mA			100	μA	2
Input leakage current		I _{I (L)}	V _I = 0 to 3.6 V All other pins not under test = 0 V		-5	+5	μA	
Output leakage current		I _{O (L)}	V _O = 0 to 3.6 V Output is disabled (Hi-Z)		-5	+5	μA	
High level output voltage		V _{OH}	I _O = -2.0 mA		2.4		V	
Low level output voltage		V _{OL}	I _O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

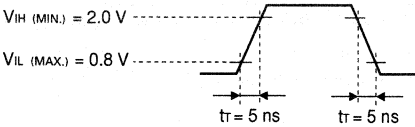
2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

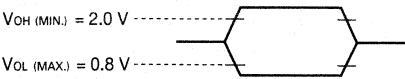
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	trac = 60 ns		trac = 70 ns		trac = 80 ns		trac = 100 ns		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Read / Write Cycle Time	trc	120	–	130	–	150	–	180	–	ns		
RAS Precharge Time	trp	50	–	50	–	60	–	70	–	ns		
CAS Precharge Time	tcpn	10	–	10	–	10	–	10	–	ns		
RAS Pulse Width	trās	60	10,000	70	10,000	80	10,000	100	10,000	ns		
CAS Pulse Width	tcās	20	10,000	20	10,000	20	10,000	25	10,000	ns		
RAS Hold Time	trsh	20	–	20	–	20	–	25	–	ns		
CAS Hold Time	tcsH	60	–	70	–	80	–	100	–	ns		
RAS to CAS Delay Time	trcd	20	40	20	50	25	60	25	70	ns	1	
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	17	50	ns	1	
CAS to RAS Precharge Time	tcpR	10	–	10	–	10	–	10	–	ns	2	
Row Address Setup Time	tasR	0	–	0	–	0	–	0	–	ns		
Row Address Hold Time	trah	10	–	10	–	12	–	12	–	ns		
Column Address Setup Time	tasc	0	–	0	–	0	–	0	–	ns		
Column Address Hold Time	tcaH	15	–	15	–	15	–	20	–	ns		
OE Lead Time Referenced to RAS	toes	0	–	0	–	0	–	0	–	ns		
CAS to Data Setup Time	tclZ	0	–	0	–	0	–	0	–	ns		
OE to Data Setup Time	tolZ	0	–	0	–	0	–	0	–	ns		
OE to Data Delay Time	toed	15	–	15	–	20	–	25	–	ns		
Transition Time (Rise and Fall)	tr	3	50	3	50	3	50	3	50	ns		
Refresh Time	μPD42S4400L	tREF	–	128	–	128	–	128	–	128	ms	3
	μPD424400L		–	16	–	16	–	16	–	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD (MAX.) and trCD (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

2. tCRP (MIN.) requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles preceded by any cycle.
3. This specification is applied only to the μPD42S4400L.

Read Cycle

Parameter	Symbol	$\text{trAC} = 60 \text{ ns}$		$\text{trAC} = 70 \text{ ns}$		$\text{trAC} = 80 \text{ ns}$		$\text{trAC} = 100 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	trAC	–	60	–	70	–	80	–	100	ns	1
Access Time from $\overline{\text{CAS}}$	tCAC	–	20	–	20	–	20	–	25	ns	1
Access Time from Column Address	tAA	–	30	–	35	–	40	–	50	ns	1
Access Time from $\overline{\text{OE}}$	tOEA	–	20	–	20	–	20	–	25	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	trAL	30	–	35	–	40	–	50	–	ns	
Read Command Setup Time	trCS	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	trRH	10	–	10	–	10	–	10	–	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	trCH	0	–	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	tOEZ	0	15	0	15	0	20	0	25	ns	3
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	tOFF	0	15	0	15	0	20	0	25	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD (MAX.) and trCD (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

2. Either trCH (MIN.) or trRH (MIN.) should be met in read cycles.
3. tOFF (MAX.) and tOEZ (MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to VOH or VOL .

Write Cycle

Parameter	Symbol	t _{WAC} = 60 ns		t _{WAC} = 70 ns		t _{WAC} = 80 ns		t _{WAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	15	–	15	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	15	–	15	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	20	–	20	–	20	–	25	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	15	–	15	–	15	–	20	–	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	–	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	–	0	–	0	–	0	–	ns	
Data-in Setup Time	tds	0	–	0	–	0	–	0	–	ns	3
Data-in Hold Time	tdh	15	–	15	–	15	–	20	–	ns	3

- Notes**
1. twp (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch (MIN.) should be met.
 2. If twcs $\geq$ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. tds (MIN.) and tdh (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{WAC} = 60 ns		t _{WAC} = 70 ns		t _{WAC} = 80 ns		t _{WAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	165	–	175	–	200	–	240	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	80	–	90	–	105	–	130	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	40	–	40	–	45	–	55	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	50	–	55	–	65	–	80	–	ns	1

- Note**
1. If twcs $\geq$ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwd $\geq$ trwd (MIN.), tcwd $\geq$ tcwd (MIN.), tawd $\geq$ tawd (MIN.) and tcpwd $\geq$ tcpwd (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	50	—	60	—	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	—	35	—	40	—	45	—	55	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	—	10	—	10	—	15	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35	—	40	—	45	—	55	—	ns	
Read Modify Write Cycle Time	t _{PRWC}	85	—	90	—	100	—	120	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	55	—	60	—	70	—	85	—	ns	1

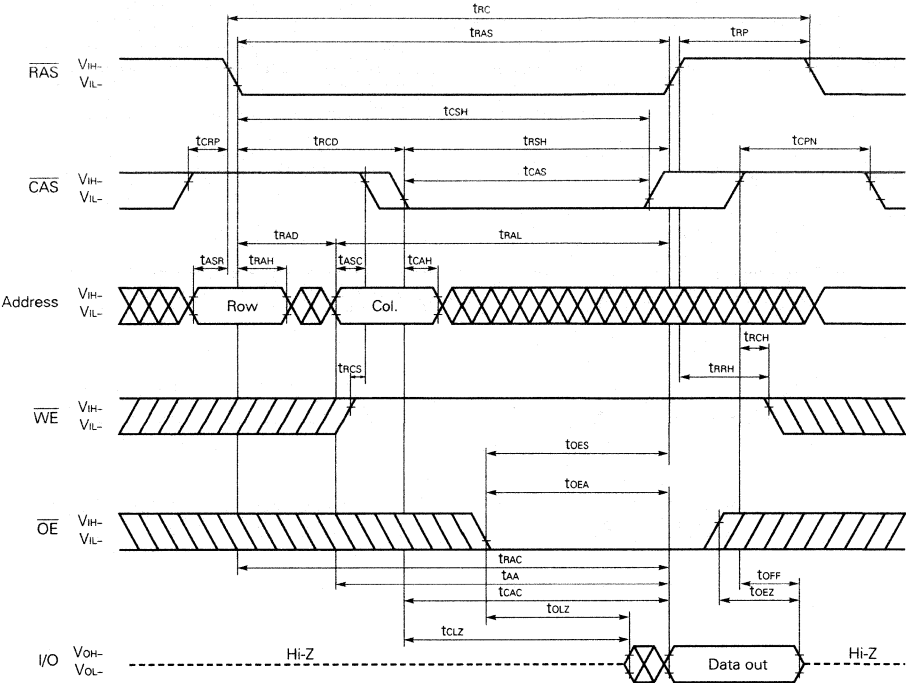
Note 1. If $\text{twcs} \geq \text{twcs}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{trwd} \geq \text{trwd}(\text{MIN.})$, $\text{tcwd} \geq \text{tcwd}(\text{MIN.})$, $\text{tawd} \geq \text{tawd}(\text{MIN.})$ and $\text{tcpwd} \geq \text{tcpwd}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

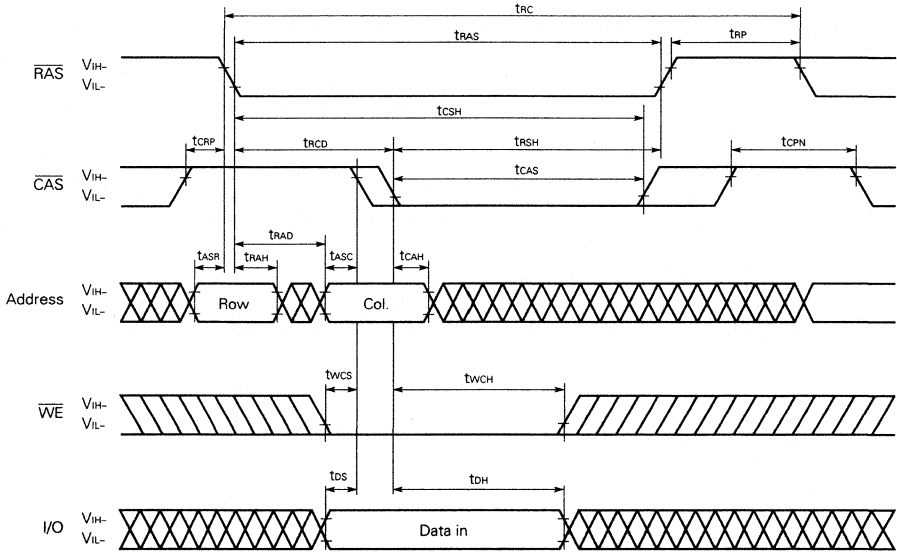
Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ Setup Time	t _{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	15	—	15	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	t _{RASS}	100	—	100	—	100	—	100	—	μs	1
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	t _{RPS}	130	—	130	—	150	—	180	—	ns	1
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	t _{CHS}	-50	—	-50	—	-50	—	-50	—	ns	1
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15	—	15	—	15	—	20	—	ns	

Note 1. This specification is applied only to the μPD42S4400L.

Read Cycle

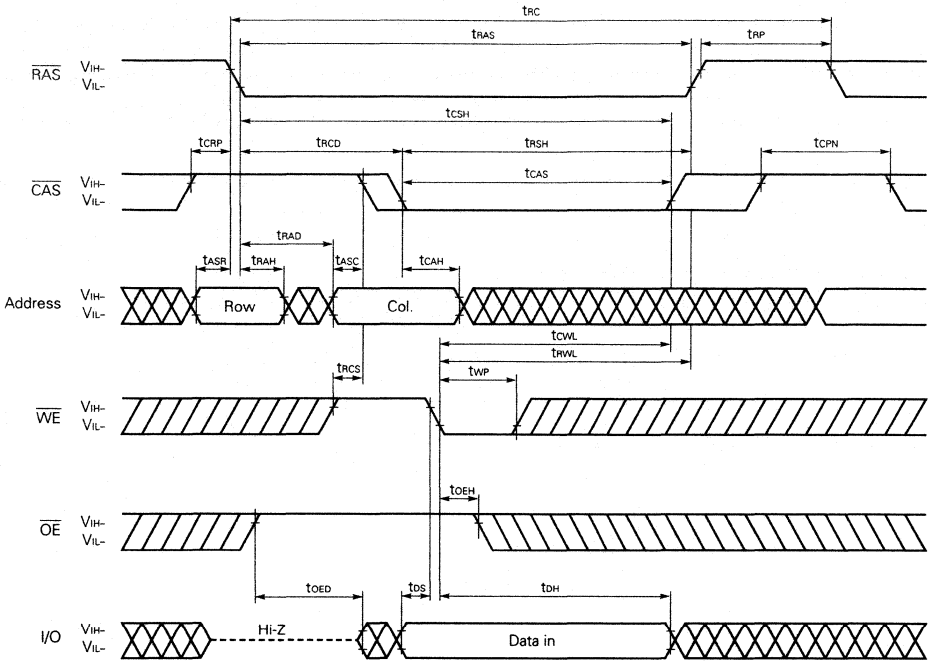


Early Write Cycle

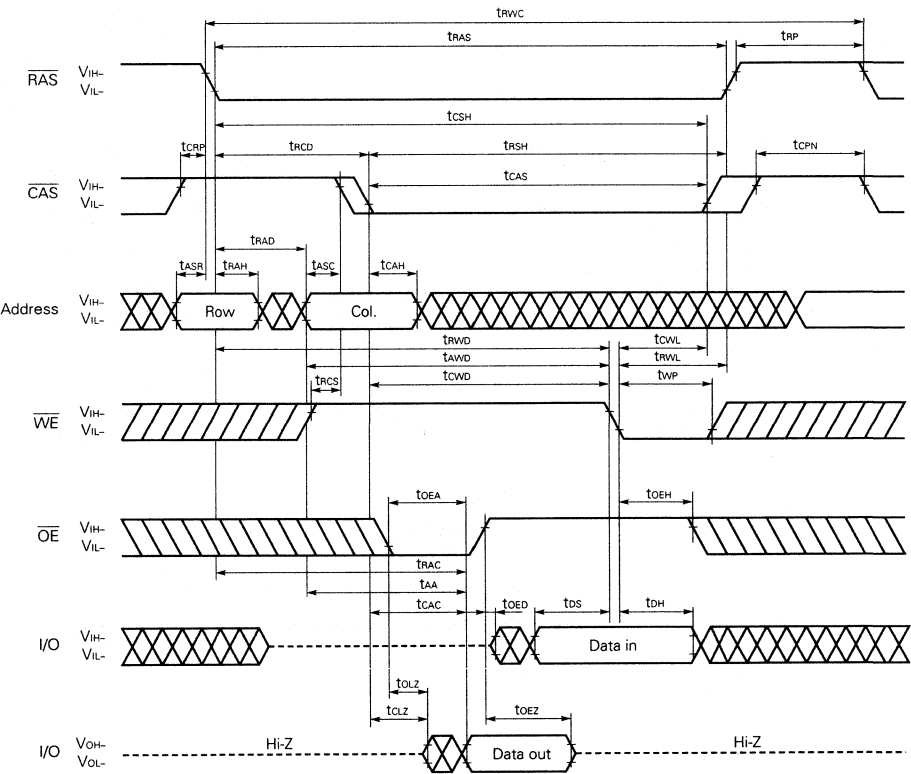


Remark $\overline{\text{OE}}$: Don't care

Late Write Cycle



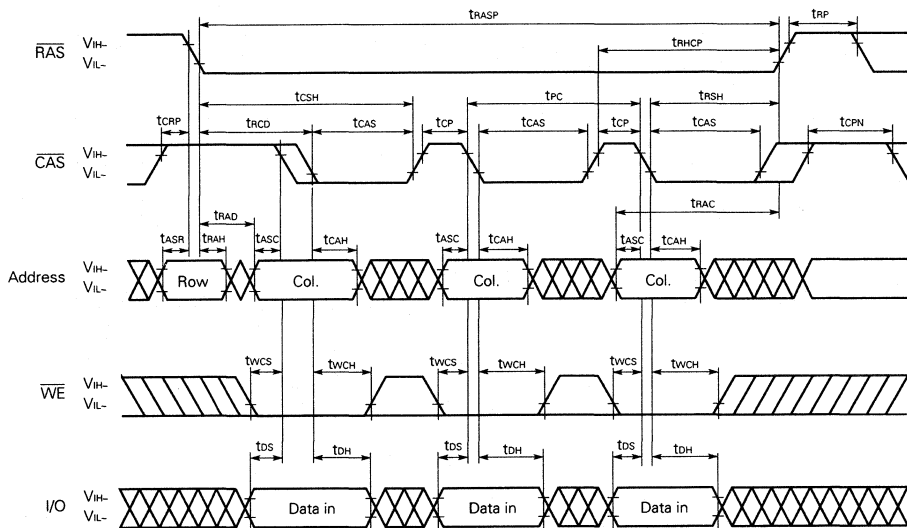
Read Modify Write Cycle



[illegible]

729

Fast Page Mode Early Write Cycle



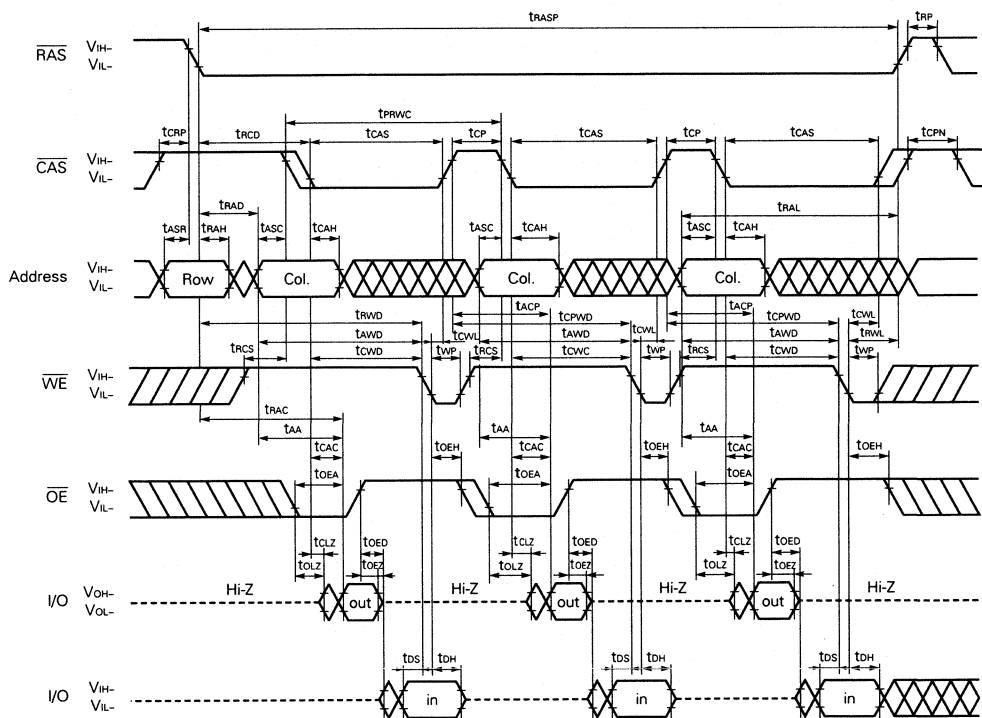
Remarks 1. $\overline{\text{OE}}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

[illegible]

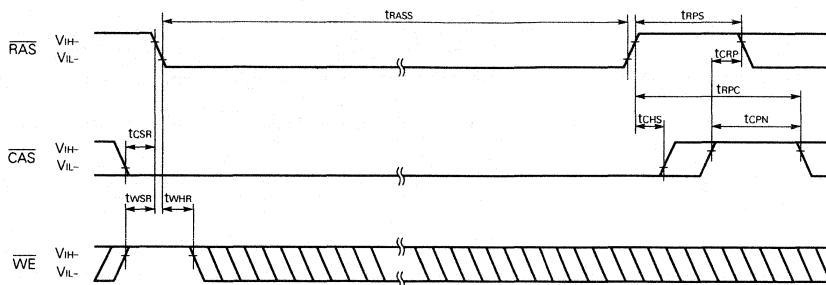
731

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh Cycle (Only for the μ PD42S4400L)



Remark Address, $\overline{\text{OE}}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh can be used independently when used in combination with distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh; However, when used in combination with burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh or with long $\overline{\text{RAS}}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Burst $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Long Refresh

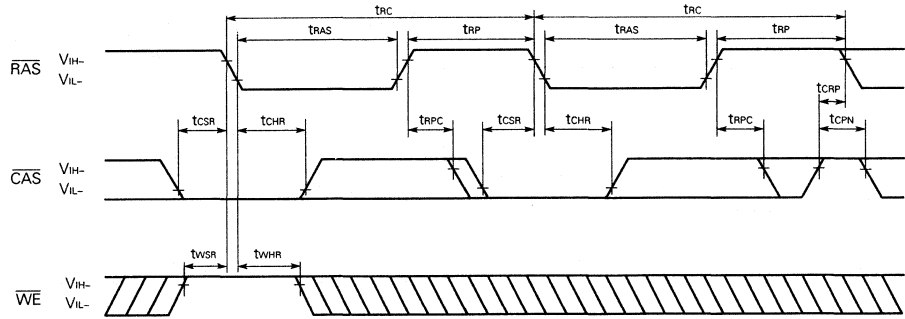
When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh are used in combination, please perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh 1,024 times within a 16 ms interval just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

(2) Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Long $\overline{\text{RAS}}$ Only Refresh

When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and $\overline{\text{RAS}}$ only refresh are used in combination, please perform $\overline{\text{RAS}}$ only refresh 1,024 times within a 16 ms interval just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

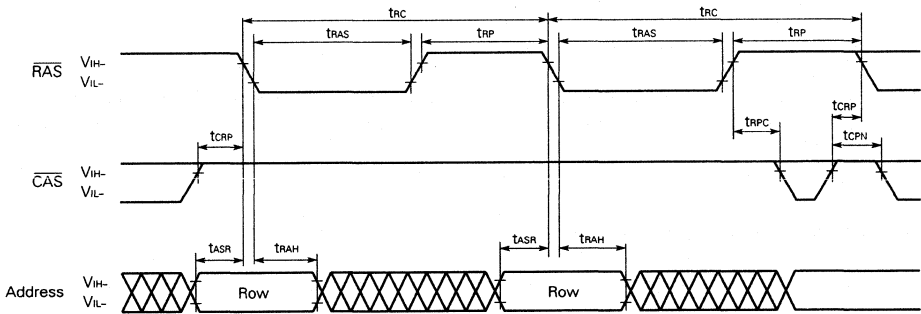
For details, please refer to **How to use DRAM** User's Manual.

$\overline{\text{RAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

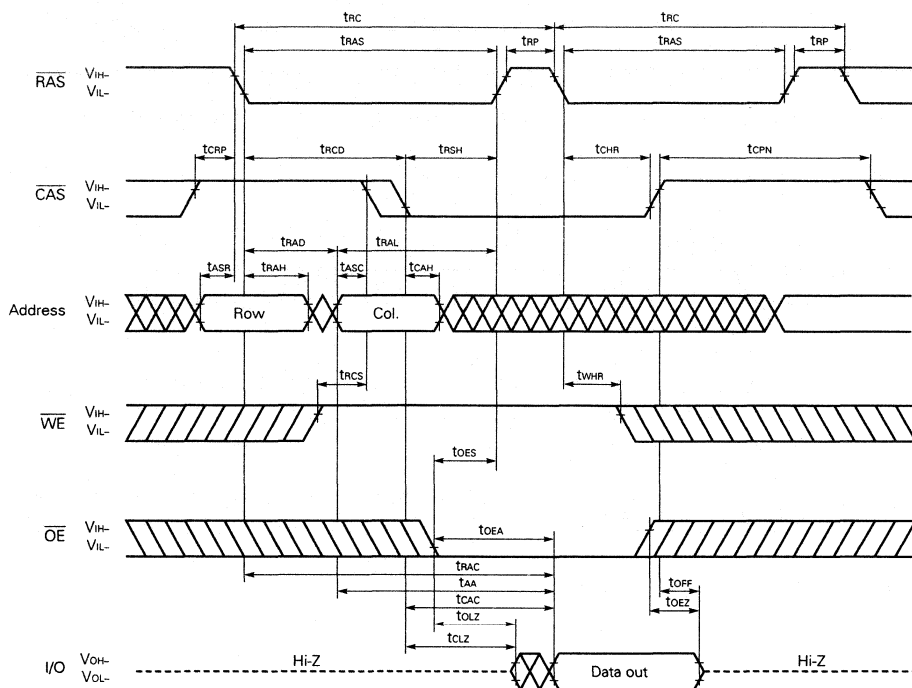


Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

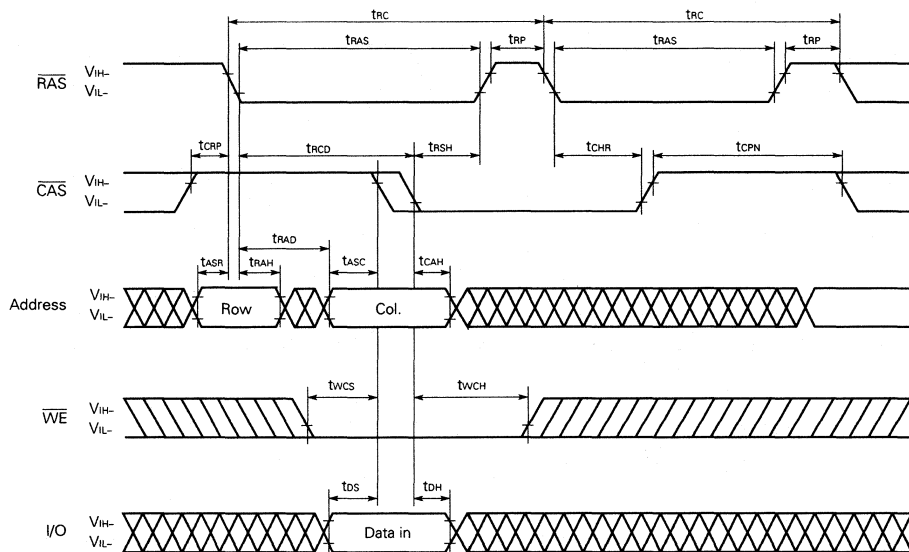
$\overline{\text{RAS}}$ Only Refresh Cycle



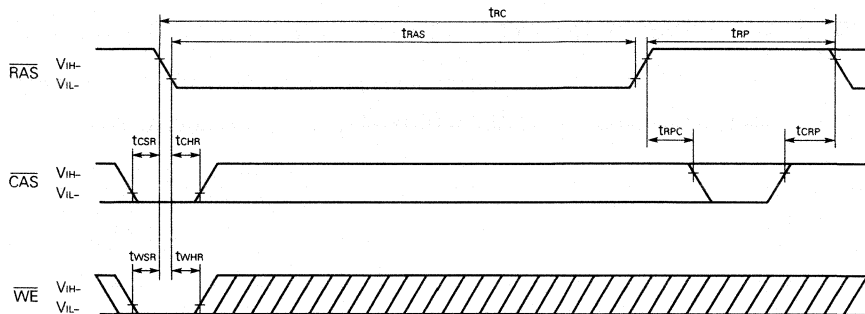
Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O: Hi-Z



Hidden Refresh Cycle (Write)



Remark $\overline{\text{OE}}$: Don't care

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)

Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 8$ -bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 8 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)

Output = "0": Abnormal write

(3) Refresh

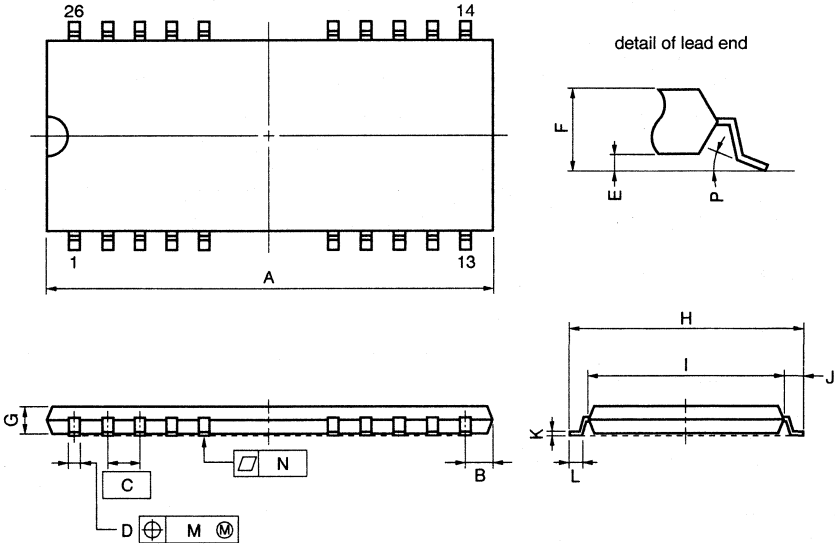
Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

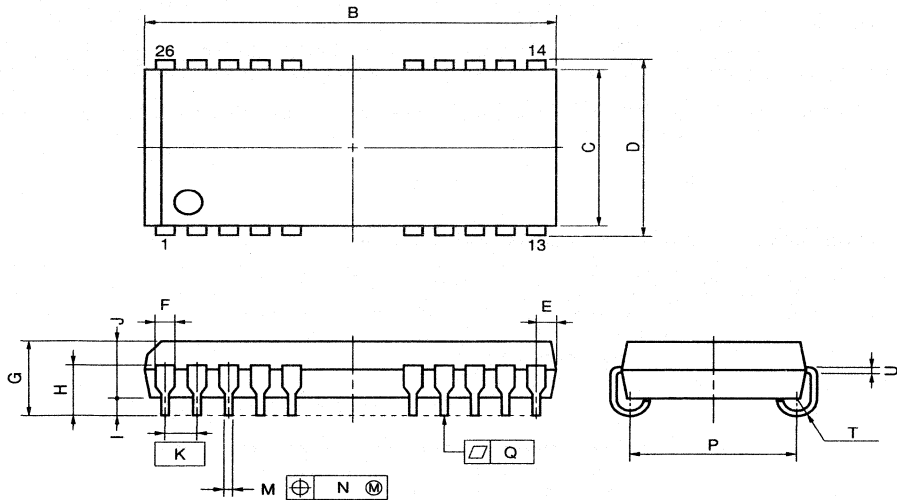
★ Package Drawings

26 PIN PLASTIC TSOP (II) (300 mil)



S26G3-50-9JD

26 PIN PLASTIC SOJ (300 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	17.4 ^{+0.2} _{-0.35}	0.685 ^{+0.008} _{-0.013}
C	7.57	0.298
D	8.47±0.2	0.333 ^{+0.009} _{-0.008}
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.6	0.024
G	3.5±0.2	0.138±0.008
H	2.4±0.2	0.094 ^{+0.009} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.15	0.006
T	R 0.85	R0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

P26LA-50A-2

★ Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S4400L, 424400L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S4400LGS, 424400LGS: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S4400LLA, 424400LLA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days^{Note} (20 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days^{Note} (20 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

MOS INTEGRATED CIRCUIT

μ PD42S4800L, 424800L

3.3 V OPERATION 4 M-BIT DYNAMIC RAM 512 K-WORD BY 8-BIT, FAST PAGE MODE

Description

The μ PD42S4800L, 424800L are 524 288 words by 8 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

Besides, the μ PD42S4800L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

These devices are packed in 28-pin plastic TSOP(II) and 28-pin plastic SOJ.



Features

- 524 288 words by 8 bits organization
- Single +3.3 V $\pm$ 0.3 V power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S4800L-A70, 424800L-A70	288 mW	70 ns	130 ns	45 ns
μ PD42S4800L-A80, 424800L-A80	252 mW	80 ns	150 ns	50 ns
μ PD42S4800L-A10, 424800L-A10	216 mW	100 ns	180 ns	60 ns

- The μ PD42S4800L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S4800L	1 024 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	0.36 mW (CMOS level input)
μ PD424800L	1 024 cycles/16 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

- Multiplexed address inputs ... Row address : A0 to A9, Column address : A0 to A8

The information in this document is subject to change without notice.

The mark ★ shows revised points.

★ Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD42S4800LG5-A70-7JD	70 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S4800LG5-A80-7JD	80 ns		
μ PD42S4800LG5-A10-7JD	100 ns		
μPD42S4800LG5-A70-7KD	70 ns	28-pin Plastic TSOP(II) (400 mil) Reverse bent	
μPD42S4800LG5-A80-7KD	80 ns		
μPD42S4800LG5-A10-7KD	100 ns		
μ PD42S4800LLE-A70	70 ns	28-pin Plastic SOJ (400 mil)	
μ PD42S4800LLE-A80	80 ns		
μ PD42S4800LLE-A10	100 ns		
μ PD424800LG5-A70-7JD	70 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD424800LG5-A80-7JD	80 ns		
μ PD424800LG5-A10-7JD	100 ns		
μPD424800LG5-A70-7KD	70 ns	28-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD424800LG5-A80-7KD	80 ns		
μPD424800LG5-A10-7KD	100 ns		
μ PD424800LLE-A70	70 ns	28-pin Plastic SOJ (400 mil)	
μ PD424800LLE-A80	80 ns		
μ PD424800LLE-A10	100 ns		

Quality Grade

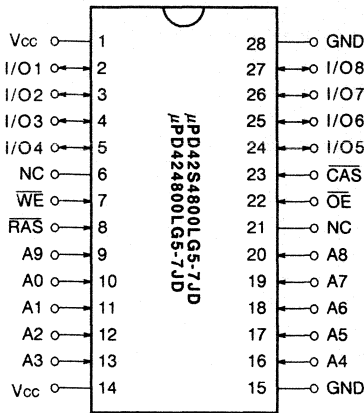
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

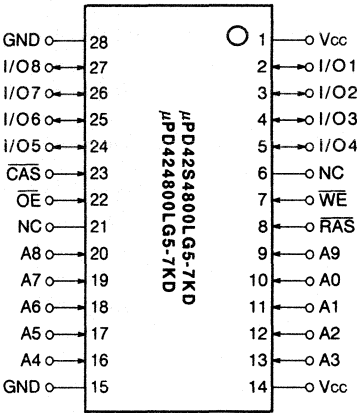


Pin Configurations (Marking side)

28-pin Plastic TSOP(II)
(400 mil)

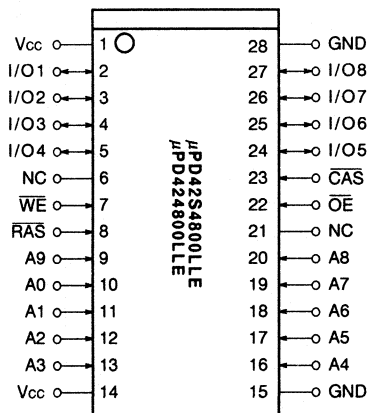


Reverse bent



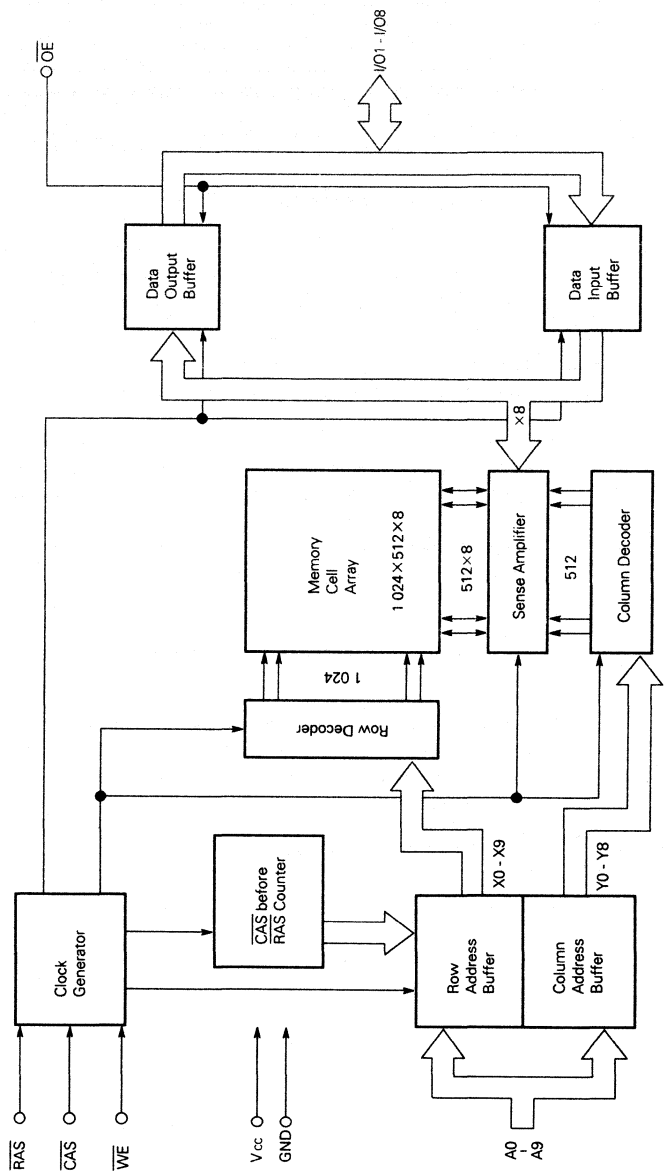
- A0 to A9 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

28-pin Plastic SOJ
(400 mil)



- A0 to A9 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
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- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Input/Output Pin Functions

The μ PD42S4800L, 424800L have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A9 and input/output pins I/O1 to I/O8.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address (A0 to A9) and selecting a corresponding word line. It refreshes memory cell array of one line (4 096-bit) selected by the row address (A0 to A9). It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)	Input	$\overline{\text{CAS}}$ activates data input/output circuit by latching column address (A0 to A8) and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address inputs)	Input	10-bit address bus. Input total 19-bit of address signal, upper 10-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word (8-bit) is selected from 524 288-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs / outputs)	Input/ Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before RAS or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-0.5 to +4.6	V
Supply Voltage	V_{CC}		-0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low Level Input Voltage	V_{IL}		-0.3		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

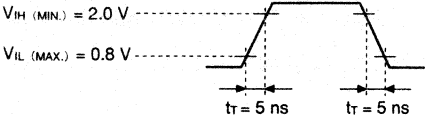
Parameter		Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	RAS, CAS Cycling			80	mA	1, 2, 3
			t _{RC} = t _{RC} (MIN.)			70		
			I _O = 0 mA			60		
Standby current	μ PD42S4800L	I _{CC2}	RAS, CAS $\geq V_{IH}$ (MIN.), I _O = 0 mA			0.5	mA	
			RAS, CAS $\geq V_{CC} - 0.2$ V, I _O = 0 mA			0.1		
	μ PD424800L		RAS, CAS $\geq V_{IH}$ (MIN.), I _O = 0 mA			2		
			RAS, CAS $\geq V_{CC} - 0.2$ V, I _O = 0 mA			0.5		
RAS only refresh current		I _{CC3}	RAS Cycling, CAS $\geq V_{IH}$ (MIN.)			80	mA	1,2,3,4
			t _{RC} = t _{RC} (MIN.), I _O = 0 mA			70		
						60		
Operating current (Fast page mode)		I _{CC4}	RAS $\leq V_{IL}$ (MAX.), CAS Cycling			70	mA	1, 2, 5
			t _{PC} = t _{PC} (MIN.), I _O = 0 mA			60		
						50		
CAS before RAS refresh current		I _{CC5}	RAS Cycling			80	mA	1, 2
			t _{RC} = t _{RC} (MIN.)			70		
			I _O = 0 mA			60		
CAS before RAS long refresh current (1 024 Cycles / 128 ms, only for the μ PD42S4800L)		I _{CC6}	CAS before RAS refresh : 1 024 Cycles / 128 ms			100	μ A	1, 2
			RAS, CAS : $V_{CC}-0.2$ V $\leq V_{IH} \leq V_{IH}(\text{MAX.})$ 0 V $\leq V_{IL} \leq 0.2$ V					
			Standby : RAS, CAS $\geq V_{CC}-0.2$ V Address : V_{IH} or V_{IL} WE, OE : V_{IH} I _O = 0 mA			150		
Self refresh current (CAS before RAS self refresh, only for the μ PD42S4800L)		I _{CC7}	RAS, CAS : $V_{CC}-0.2$ V $\leq V_{IH} \leq V_{IH}(\text{MAX.})$ 0 V $\leq V_{IL} \leq 0.2$ V I _O = 0 mA			100	μ A	2
Input leakage current		I _{I(L)}	V _I = 0 to 3.6 V All other pins not under test = 0 V	-5		+5	μ A	
Output leakage current		I _{O(L)}	V _O = 0 to 3.6 V Output is disabled (Hi-Z)	-5		+5	μ A	
High level output voltage		V _{OH}	I _O = -2.0 mA	2.4			V	
Low level output voltage		V _{OL}	I _O = +2.0 mA			0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during RAS $\leq V_{IL}(\text{MAX.})$ and CAS $\geq V_{IH}(\text{MIN.})$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

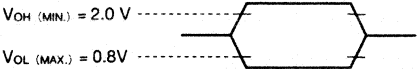
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	$t_{RAC} = 70\text{ ns}$		$t_{RAC} = 80\text{ ns}$		$t_{RAC} = 100\text{ ns}$		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		t_{RC}	130	—	150	—	180	—	ns	
RAS Precharge Time		t_{RP}	50	—	60	—	70	—	ns	
CAS Precharge Time		t_{CPN}	10	—	10	—	10	—	ns	
RAS Pulse Width		t_{RAS}	70	10 000	80	10 000	100	10 000	ns	
CAS Pulse Width		t_{CAS}	20	10 000	20	10 000	25	10 000	ns	
RAS Hold Time		t_{RSH}	20	—	20	—	25	—	ns	
CAS Hold Time		t_{CSH}	70	—	80	—	100	—	ns	
RAS to CAS Delay Time		t_{RCD}	20	50	20	60	25	75	ns	1
RAS to Column Address Delay Time		t_{RAD}	15	35	15	40	17	50	ns	1
CAS to RAS Precharge Time		t_{CRP}	10	—	10	—	10	—	ns	2
Row Address Setup Time		t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time		t_{RAH}	10	—	10	—	12	—	ns	
Column Address Setup Time		t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time		t_{CAH}	15	—	15	—	20	—	ns	
OE Lead Time Referenced to RAS		t_{OES}	0	—	0	—	0	—	ns	
CAS to Data Setup Time		t_{CLZ}	0	—	0	—	0	—	ns	
OE to Data Setup Time		t_{OLZ}	0	—	0	—	0	—	ns	
OE to Data Delay Time		t_{OED}	15	—	15	—	20	—	ns	
Transition Time (Rise and Fall)		t_T	3	50	3	50	3	50	ns	
Refresh Time	μPD42S4800L	t_{REF}	—	128	—	128	—	128	ms	3
	μPD424800L		—	16	—	16	—	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{RAC} (MAX.)$	$t_{RAC} (MAX.)$
$t_{RAD} > t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{AA} (MAX.)$	$t_{RAD} + t_{AA} (MAX.)$
$t_{RCD} > t_{RCD} (MAX.)$	$t_{CAC} (MAX.)$	$t_{RCD} + t_{CAC} (MAX.)$

$t_{RAD} (MAX.)$ and $t_{RCD} (MAX.)$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD} (MAX.)$ and $t_{RCD} \geq t_{RCD} (MAX.)$ will not cause any operation problems.

2. tCRP(MIN.) requirement is applied for $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles preceded by any cycle.
3. This specification is applied only for the μPD42S4800L.

Read Cycle

Parameter	Symbol	t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		t _{TRAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	t _{TRAC}	–	70	–	80	–	100	ns	1
Access Time from $\overline{\text{CAS}}$	t _{TCAC}	–	20	–	20	–	25	ns	1
Access Time from Column Address	t _{TAA}	–	35	–	40	–	50	ns	1
Access Time from $\overline{\text{OE}}$	t _{TOEA}	–	20	–	20	–	25	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{TRAL}	35	–	40	–	50	–	ns	
Read Command Setup Time	t _{TRCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{TRRH}	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{TRCH}	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{TOEZ}	0	15	0	15	0	20	ns	3
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{TOFF}	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
t _{TRAD} ≤ t _{TRAD} (MAX.) and t _{TRCD} ≤ t _{TRCD} (MAX.)	t _{TRAC} (MAX.)	t _{TRAC} (MAX.)
t _{TRAD} > t _{TRAD} (MAX.) and t _{TRCD} ≤ t _{TRCD} (MAX.)	t _{TAA} (MAX.)	t _{TRAD} + t _{TAA} (MAX.)
t _{TRCD} > t _{TRCD} (MAX.)	t _{TCAC} (MAX.)	t _{TRCD} + t _{TCAC} (MAX.)

t_{TRAD}(MAX.) and t_{TRCD}(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(t_{TRAC}, t_{TAA} or t_{TCAC}) is to be used for finding out when output data will be available. Therefore, the input conditions t_{TRAD} ≥ t_{TRAD}(MAX.) and t_{TRCD} ≥ t_{TRCD}(MAX.) will not cause any operation problems.

2. Either t_{TRCH}(MIN.) or t_{TRRH}(MIN.) should be met in read cycles.
3. t_{TOFF}(MAX.) and t_{TOEZ}(MAX.) define the time when the output achieves the condition of Hi - Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		t _{TRAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Pulse Width	t _{WP}	10	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20	–	20	–	25	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15	–	15	–	20	–	ns	
$\overline{\text{WE}}$ Setup Time	t _{WCS}	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0	–	0	–	0	–	ns	
Data-in Setup Time	t _{DS}	0	–	0	–	0	–	ns	3
Data-in Hold Time	t _{DH}	15	–	15	–	20	–	ns	3

- Notes**
1. t_{WP(MIN.)} is applied for late write cycles or read modify write cycles. In early write cycles, t_{WCH(MIN.)} should be met.
 2. If t_{WCS} $\geq$ t_{WCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle.
 3. t_{DS(MIN.)} and t_{DH(MIN.)} are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		t _{TRAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t _{RWC}	175	–	200	–	240	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	90	–	105	–	130	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	40	–	45	–	55	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	55	–	65	–	80	–	ns	1

- Note**
1. If t_{WCS} $\geq$ t_{WCS(MIN.)}, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If t_{RWD} $\geq$ t_{RWD(MIN.)}, t_{CWD} $\geq$ t_{CWD(MIN.)}, t_{AWD} $\geq$ t_{AWD(MIN.)}, and t_{CPWD} $\geq$ t_{CPWD(MIN.)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.



Fast Page Mode

Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	45	–	50	–	60	–	ns	
Access Time from CAS Precharge	t _{ACP}	–	40	–	45	–	55	ns	
RAS Pulse Width	t _{RASP}	70	125 000	80	125 000	100	125 000	ns	
CAS Precharge Time	t _{CP}	10	–	10	–	10	–	ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	40	–	45	–	55	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	90	–	100	–	120	–	ns	
CAS Precharge to WE Delay Time	t _{CPWD}	60	–	70	–	85	–	ns	1

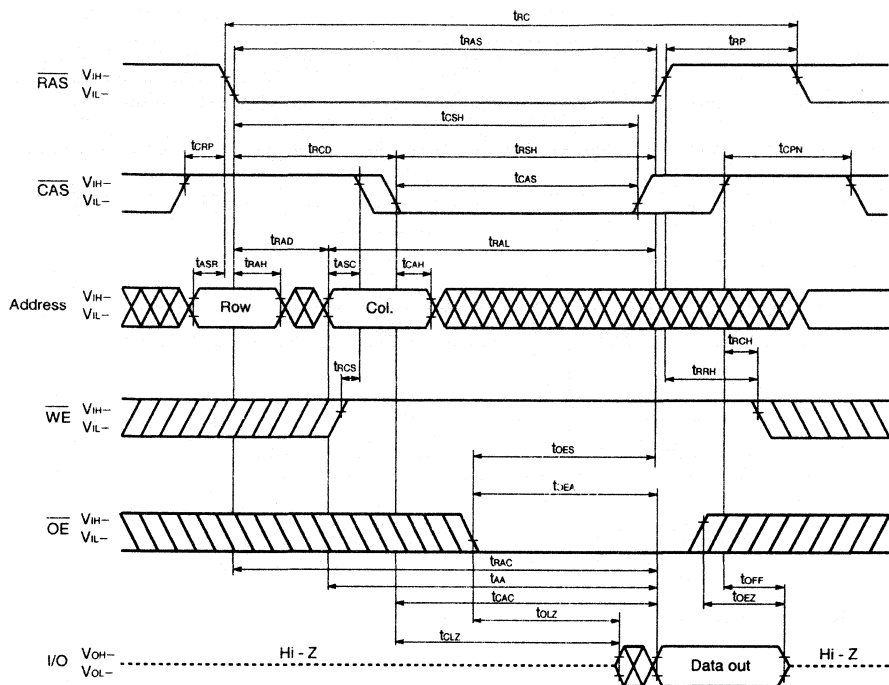
Note 1. If $twcs \geq twcs(MIN.)$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $trwd \geq trwd(MIN.)$, $tcwd \geq tcwd(MIN.)$, $tawd \geq tawd(MIN.)$, and $tcpwd \geq tcpwd(MIN.)$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

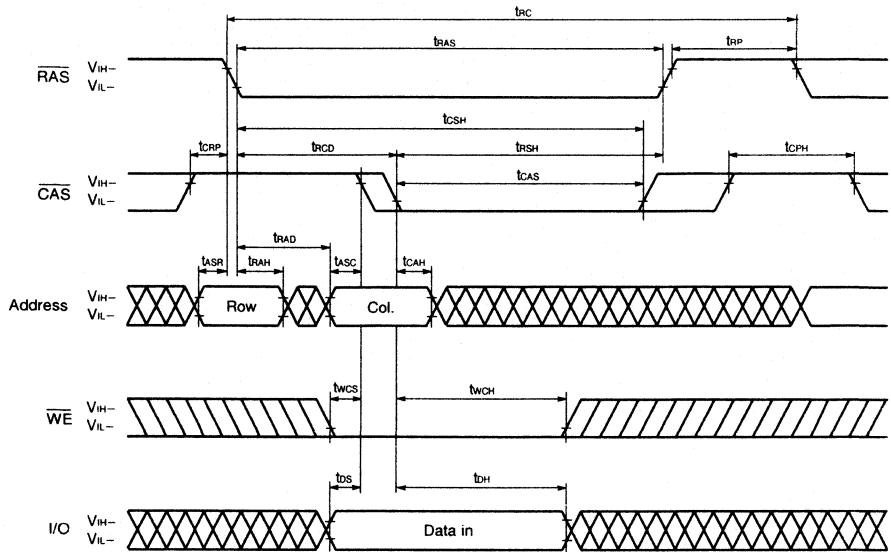
Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	–	5	–	5	–	ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10	–	10	–	10	–	ns	
RAS Precharge CAS Hold Time	t _{RPC}	10	–	10	–	10	–	ns	
RAS Pulse Width (CAS before RAS Self Refresh Cycle)	t _{RASP}	100	–	100	–	100	–	μ s	1
RAS Precharge Time (CAS before RAS Self Refresh Cycle)	t _{RPS}	130	–	150	–	180	–	ns	1
CAS Hold Time (CAS before RAS Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	–50	–	ns	1
WE Hold Time	t _{WHR}	15	–	15	–	20	–	ns	

Note 1. This specification is applied only for the μ PD42S4800L.

Read Cycle

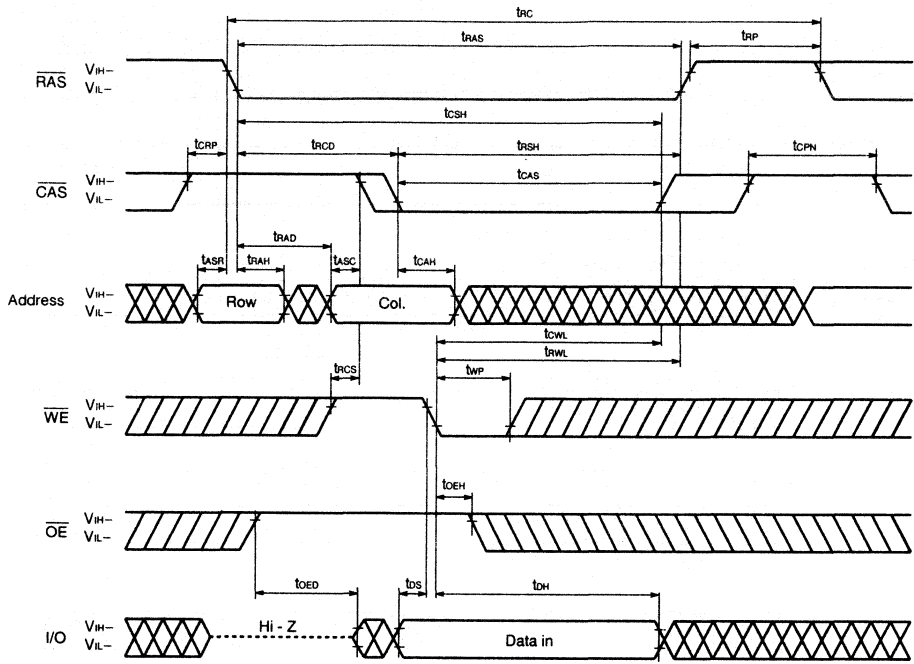


Early Write Cycle

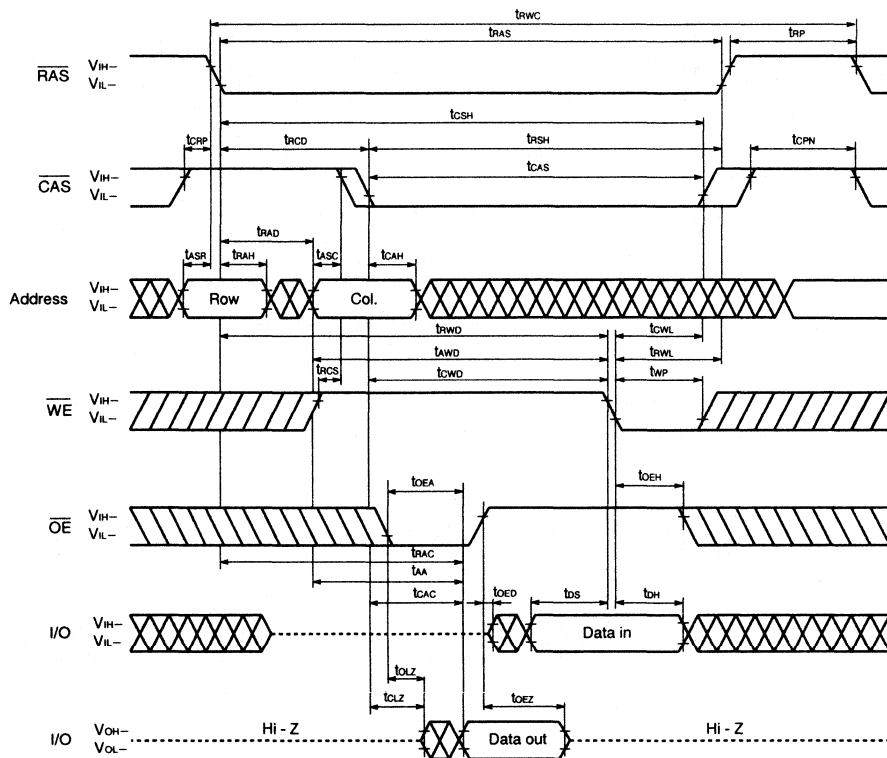


Remark $\overline{OE}$: Don't care

Late Write Cycle



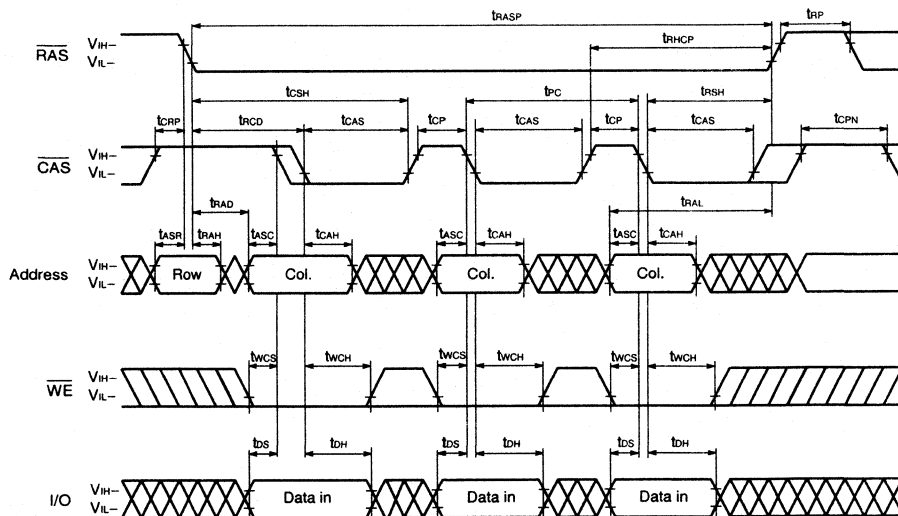
★ Read Modify Write Cycle



[illegible]

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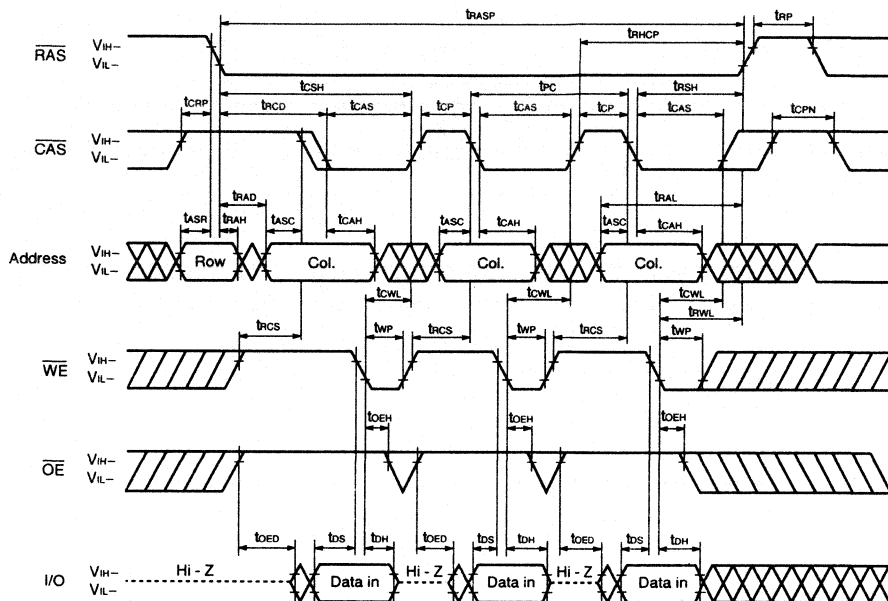
Fast Page Mode Early Write Cycle



Remark $\overline{OE}$: Don't care

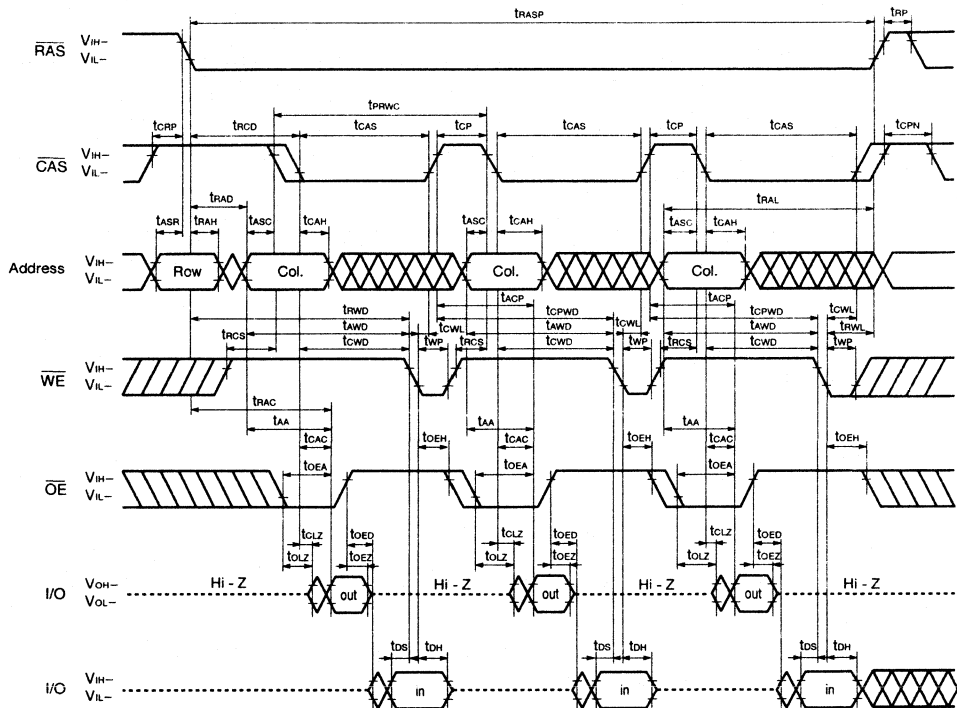
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Late Write Cycle



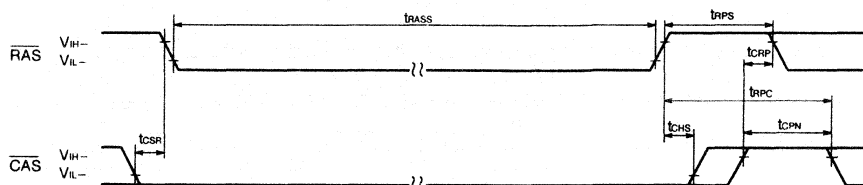
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

★ **Fast Page Mode Read Modify Write Cycle**



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle (Only for the μPD42S4800L)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi - Z

Cautions on Use of CAS Before RAS Self Refresh



CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

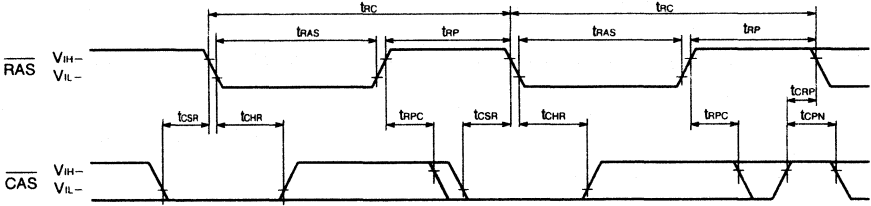
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 1 024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh 1 024 times within an interval of 16 ms or less just before and after setting CAS before RAS self refresh.

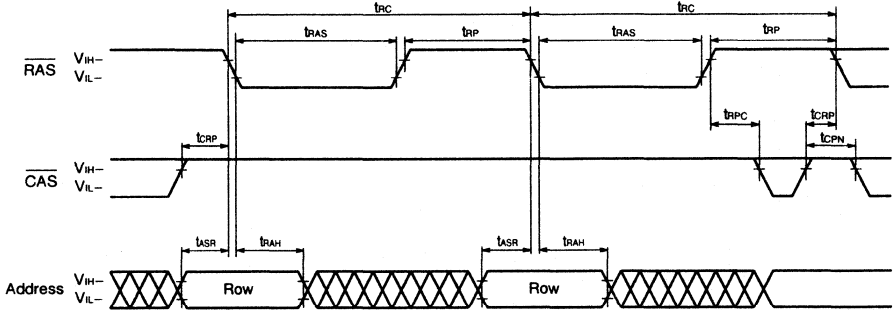
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi - Z

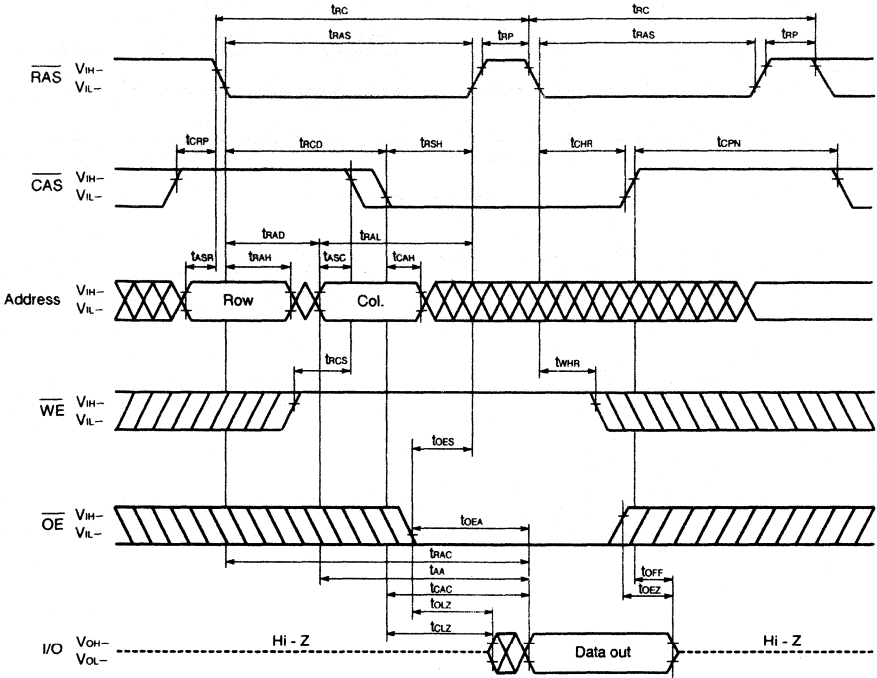
RAS Only Refresh Cycle



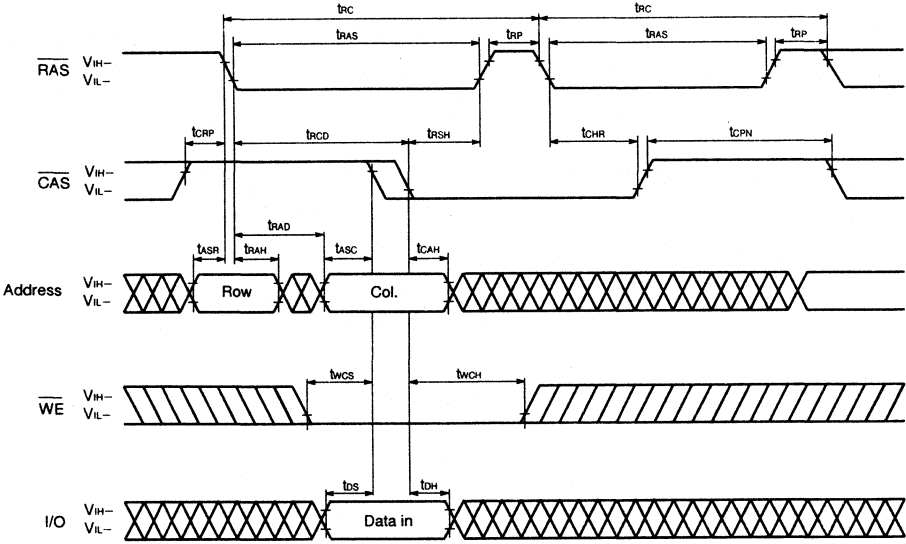
Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi - Z



Hidden Refresh Cycle (Read)



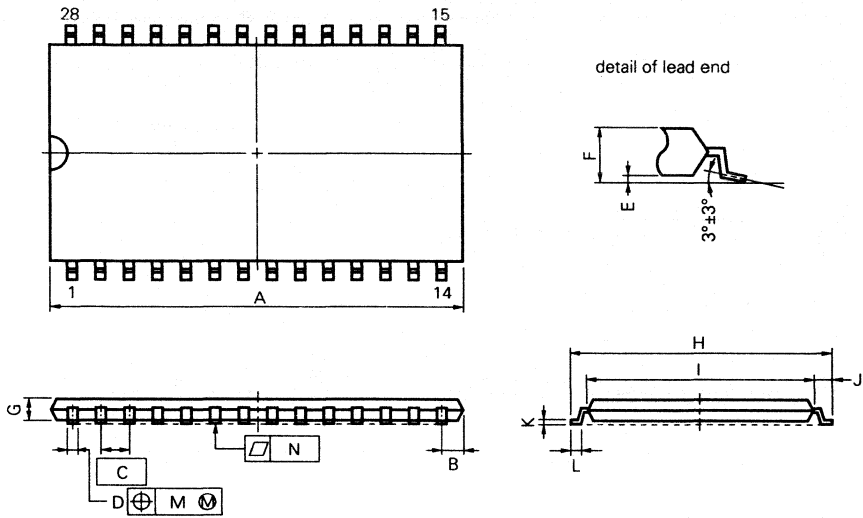
★ Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

28 PIN PLASTIC TSOP(II) (400 mil)



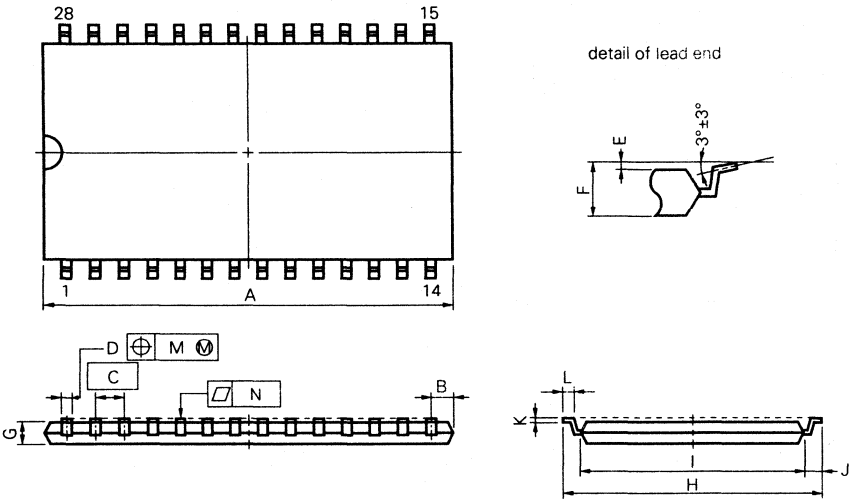
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD-2

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP(II) (400 mil)

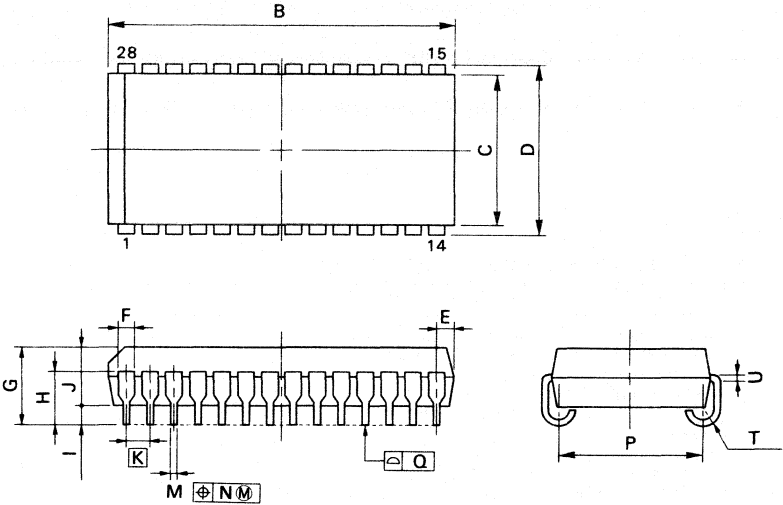


NOTE
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7KD-2

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28PIN PLASTIC SOJ (400 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LA-400A-1

ITEM	MILLIMETERS	INCHES
B	18.67 ^{+0.35} _{-0.35}	0.735 ^{+0.008} _{-0.013}
C	10.16	0.400
D	11.18 ^{±0.2}	0.440 ^{+0.008} _{-0.009}
E	1.08 ^{±0.15}	0.043 ^{+0.006} _{-0.009}
F	0.6	0.024
G	3.5 ^{±0.2}	0.138 ^{+0.008} _{-0.009}
H	2.4 ^{±0.2}	0.094 ^{+0.008} _{-0.009}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40 ^{±0.10}	0.016 ^{+0.004} _{-0.004}
N	0.12	0.005
P	9.40 ^{±0.20}	0.370 ^{+0.008} _{-0.009}
Q	0.15	0.006
T	R0.85	R0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.004}

★ Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S4800L, 424800L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S4800LG5, 424800LG5 : 28-pin plastic TSOP(II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit^{Note}: 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit^{Note}: 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S4800LLE, 424800LLE : 28-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

MOS INTEGRATED CIRCUIT

μ PD42S4260L, 424260L

3.3 V OPERATION 4 M-BIT DYNAMIC RAM

256 K-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

Description

The μ PD42S4260L, 424260L are 262 144 words by 16 bits dynamic CMOS RAMs. The fast page mode and byte read/write mode capability realize high speed access and low power consumption.

Besides, the μ PD42S4260L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

These are packed in 44-pin plastic TSOP (II) and 40-pin plastic SOJ.



Features

- 262 144 words by 16 bits organization
- Single +3.3 V $\pm$ 0.3 V power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S4260L-A70, 424260L-A70	432 mW	70 ns	130 ns	45 ns
μ PD42S4260L-A80, 424260L-A80	396 mW	80 ns	150 ns	50 ns
μ PD42S4260L-A10, 424260L-A10	360 mW	100 ns	180 ns	60 ns

- The μ PD42S4260L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S4260L	512 cycles / 128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	0.36 mW (CMOS level input)
μ PD424260L	512 cycles / 8 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

- Multiplexed address inputs Row address: A0 to A8, Column address: A0 to A8

The information in this document is subject to change without notice.

The mark ★ shows revised points.



Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD42S4260LG5-A70-7JF	70 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD42S4260LG5-A80-7JF	80 ns		
μ PD42S4260LG5-A10-7JF	100 ns		
μPD42S4260LG5-A70-7KF	70 ns	44-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD42S4260LG5-A80-7KF	80 ns		
μPD42S4260LG5-A10-7KF	100 ns		
μ PD42S4260LLE-A70	70 ns	40-pin Plastic SOJ (400 mil)	
μ PD42S4260LLE-A80	80 ns		
μ PD42S4260LLE-A10	100 ns		
μ PD424260LG5-A70-7JF	70 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD424260LG5-A80-7JF	80 ns		
μ PD424260LG5-A10-7JF	100 ns		
μPD424260LG5-A70-7KF	70 ns	44-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD424260LG5-A80-7KF	80 ns		
μPD424260LG5-A10-7KF	100 ns		
μ PD424260LLE-A70	70 ns	40-pin Plastic SOJ (400 mil)	
μ PD424260LLE-A80	80 ns		
μ PD424260LLE-A10	100 ns		

Quality Grade

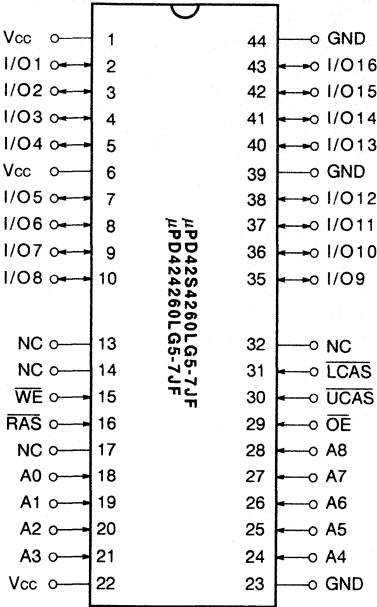
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

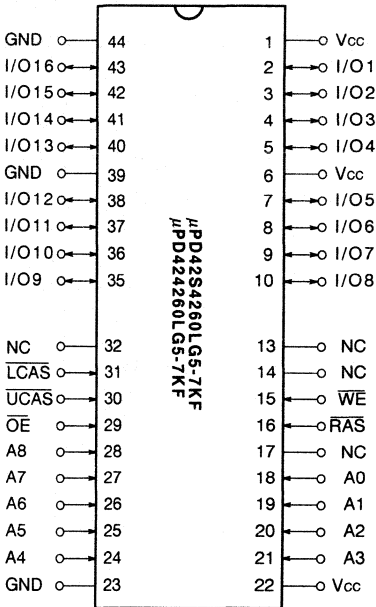
Pin Configurations (Marking Side)



44-pin Plastic TSOP(III)
(400 mil)

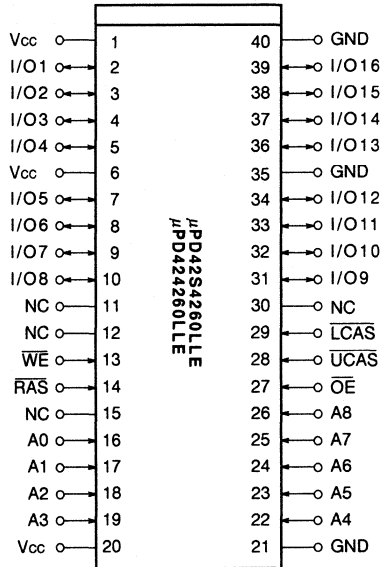


Reverse bent



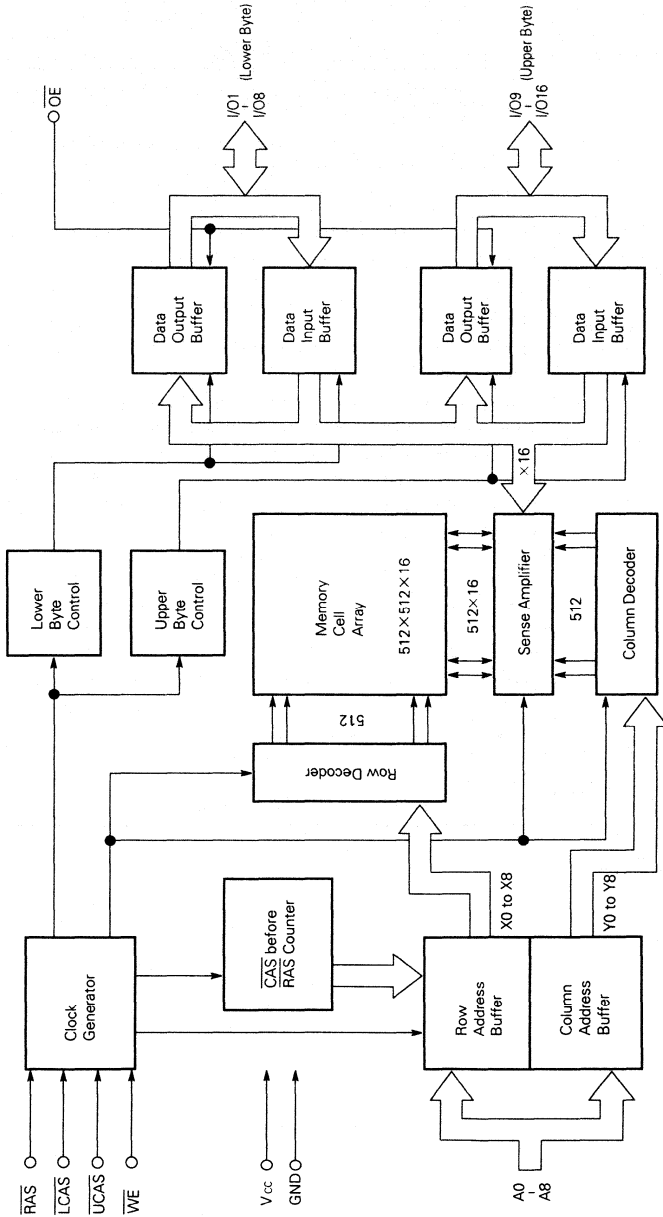
- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
- LCAS : Column Address Strobe (lower)
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

40-pin Plastic SOJ
(400 mil)



- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
- LCAS : Column Address Strobe (lower)
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram





Input/Output Pin Functions

The μPD42S4260L, 424260L have input pins $\overline{RAS}$, $\overline{CAS}$ ^{Note}, $\overline{WE}$, $\overline{OE}$, A0 to A8 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address (A0 to A8) and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address (A0 to A8). It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address (A0 to A8) and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address inputs)	Input	9-bit address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word (16-bit) is selected from 262 144-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-0.5 to +4.6	V
Supply Voltage	V_{CC}		-0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55 to +125	$^{\circ}\text{C}$

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low Level Input Voltage	V_{IL}		-0.3		+0.8	V
Ambient Temperature	T_a		0		70	$^{\circ}\text{C}$

Capacitance ($T_a = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

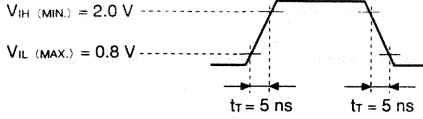
Parameter		Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	RAS, CAS Cycling	trac = 70 ns		120	mA	1, 2, 3
			trc = trc (MIN.)	trac = 80 ns		110		
			I _O = 0 mA	trac = 100 ns		100		
Standby current	μPD42S4260L	I _{CC2}	RAS, CAS ≥ V _{IH} (MIN.), I _O = 0 mA			0.5	mA	
			RAS, CAS ≥ V _{CC} - 0.2 V, I _O = 0 mA			0.1		
	μPD424260L		RAS, CAS ≥ V _{IH} (MIN.), I _O = 0 mA			2		
			RAS, CAS ≥ V _{CC} - 0.2 V, I _O = 0 mA			0.5		
RAS only refresh current		I _{CC3}	RAS Cycling, CAS ≥ V _{IH} (MIN.)	trac = 70 ns		120	mA	1,2,3,4
			trc = trc (MIN.), I _O = 0 mA	trac = 80 ns		110		
				trac = 100 ns		100		
Operating current (Fast page mode)		I _{CC4}	RAS ≤ V _{IL} (MAX.), CAS Cycling	trac = 70 ns		80	mA	1, 2, 5
			tpc = tpc (MIN.), I _O = 0 mA	trac = 80 ns		70		
				trac = 100 ns		60		
CAS before RAS refresh current		I _{CC5}	RAS Cycling	trac = 70 ns		120	mA	1, 2
			trc = trc (MIN.)	trac = 80 ns		110		
			I _O = 0 mA	trac = 100 ns		100		
CAS before RAS long refresh current (512 Cycles / 128 ms, only for the μPD42S4260L)		I _{CC6}	CAS before RAS refresh : 512 Cycles / 128 ms	trac ≤ 200 ns		100	μA	1, 2
			RAS, CAS : V _{CC} -0.2 V ≤ V _{IH} ≤ V _{IH} (MAX.) 0 V ≤ V _{IL} ≤ 0.2 V					
			Standby : RAS, CAS ≥ V _{CC} -0.2 V Address : V _{IH} or V _{IL} WE, OE : V _{IH} I _O = 0 mA	trac ≤ 1 μs		150		
Self refresh current (CAS before RAS self refresh, only for the μPD42S4260L)		I _{CC7}	RAS, CAS : V _{CC} -0.2 V ≤ V _{IH} ≤ V _{IH} (MAX.) 0 V ≤ V _{IL} ≤ 0.2 V I _O = 0 mA			100	μA	2
Input leakage current		I _I (L)	V _I = 0 to 3.6 V All other pins not under test = 0 V	-5		+5	μA	
Output leakage current		I _O (L)	V _O = 0 to 3.6 V Output is disabled (Hi-Z)	-5		+5	μA	
High level output voltage		V _{OH}	I _O = -2.0 mA	2.4			V	
Low level output voltage		V _{OL}	I _O = +2.0 mA			0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (trc and tpc).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during RAS ≤ V_{IL}(MAX.) and CAS ≥ V_{IH}(MIN.).
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

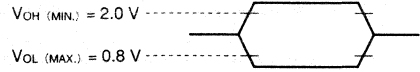
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		t _{RC}	130	–	150	–	180	–	ns	
RAS Precharge Time		t _{RP}	50	–	60	–	70	–	ns	
CAS Precharge Time		t _{CPN}	10	–	10	–	10	–	ns	
RAS Pulse Width		t _{RAS}	70	10 000	80	10 000	100	10 000	ns	
CAS Pulse Width		t _{CAS}	20	10 000	20	10 000	25	10 000	ns	
RAS Hold Time		t _{RSH}	20	–	20	–	25	–	ns	
CAS Hold Time		t _{CSH}	70	–	80	–	100	–	ns	
RAS to $\overline{\text{CAS}}$ Delay Time		t _{RCd}	20	50	20	60	25	75	ns	1
RAS to Column Address Delay Time		t _{RAD}	15	35	15	40	17	50	ns	1
CAS to $\overline{\text{RAS}}$ Precharge Time		t _{CRP}	10	–	10	–	10	–	ns	2
Row Address Setup Time		t _{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time		t _{RAH}	10	–	10	–	12	–	ns	
Column Address Setup Time		t _{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time		t _{CAH}	15	–	15	–	20	–	ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$		t _{OES}	0	–	0	–	0	–	ns	
$\overline{\text{CAS}}$ to Data Setup Time		t _{CLZ}	0	–	0	–	0	–	ns	
$\overline{\text{OE}}$ to Data Setup Time		t _{OLZ}	0	–	0	–	0	–	ns	
$\overline{\text{OE}}$ to Data Delay Time		t _{OED}	15	–	15	–	20	–	ns	
Masked Byte Write Hold Time Referenced to $\overline{\text{RAS}}$		t _{MRH}	0	–	0	–	0	–	ns	
Transition Time (Rise and Fall)		t _T	3	50	3	50	3	50	ns	
Refresh Time	$\mu\text{PD42S4260L}$	t _{REF}	–	128	–	128	–	128	ms	3
	$\mu\text{PD424260L}$		–	8	–	8	–	8	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD (MAX.) and trCD (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

- tCRP (MIN.) requirement is applied for RAS, CAS cycles preceded by any cycle.
- This specification is applied only for the μ PD42S4260L.

Read Cycle

Parameter	Symbol	$\text{trAC} = 70 \text{ ns}$		$\text{trAC} = 80 \text{ ns}$		$\text{trAC} = 100 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	trAC	–	70	–	80	–	100	ns	1
Access Time from $\overline{\text{CAS}}$	tCAC	–	20	–	20	–	25	ns	1
Access Time from Column Address	tAA	–	35	–	40	–	50	ns	1
Access Time from $\overline{\text{OE}}$	tOEA	–	20	–	20	–	25	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	trAL	35	–	40	–	50	–	ns	
Read Command Setup Time	trCS	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	trRH	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	trCH	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	tOEZ	0	15	0	15	0	20	ns	3
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	tOFF	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD (MAX.) and trCD (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

- Either trCH (MIN.) or trRH (MIN.) should be met in read cycles.
- tOFF (MAX.) and tOEZ (MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	10	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	10	–	15	–	20	–	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	20	–	20	–	25	–	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	15	–	15	–	20	–	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	–	0	–	0	–	ns	
Data-in Setup Time	tds	0	–	0	–	0	–	ns	3
Data-in Hold Time	tdh	15	–	15	–	20	–	ns	3

- Notes**
1. t_{wp(MIN.)} is applied for late write cycles or read modify write cycles. In early write cycles, t_{wch(MIN.)} should be met.
 2. If t_{wcs} $\geq$ t_{wcs(MIN.)}, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{ds(MIN.)} and t_{dh(MIN.)} are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	175	–	200	–	240	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	90	–	105	–	130	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	40	–	45	–	55	–	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	55	–	65	–	80	–	ns	1

- Note**
1. If t_{wcs} $\geq$ t_{wcs(MIN.)}, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{rwcd} $\geq$ t_{rwcd(MIN.)}, t_{tcwd} $\geq$ t_{tcwd(MIN.)}, t_{tawd} $\geq$ t_{tawd(MIN.)}, and t_{cpwd} $\geq$ t_{cpwd(MIN.)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	45	–	50	–	60	–	ns	
Access Time from CAS Precharge	t _{ACP}	–	40	–	45	–	55	ns	
RAS Pulse Width	t _{RASP}	70	125 000	80	125 000	100	125 000	ns	
CAS Precharge Time	t _{CP}	10	–	10	–	10	–	ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	40	–	45	–	55	–	ns	
Read Modify Write Cycle Time	t _{PRWC}	90	–	100	–	120	–	ns	
CAS Precharge to WE Delay Time	t _{CPWD}	60	–	70	–	85	–	ns	1

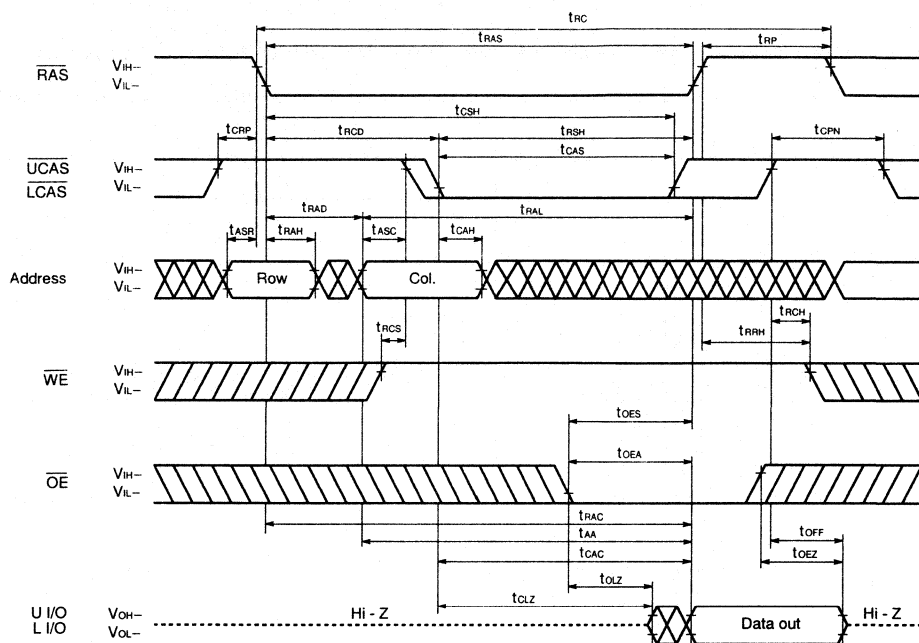
Note 1. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$, and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

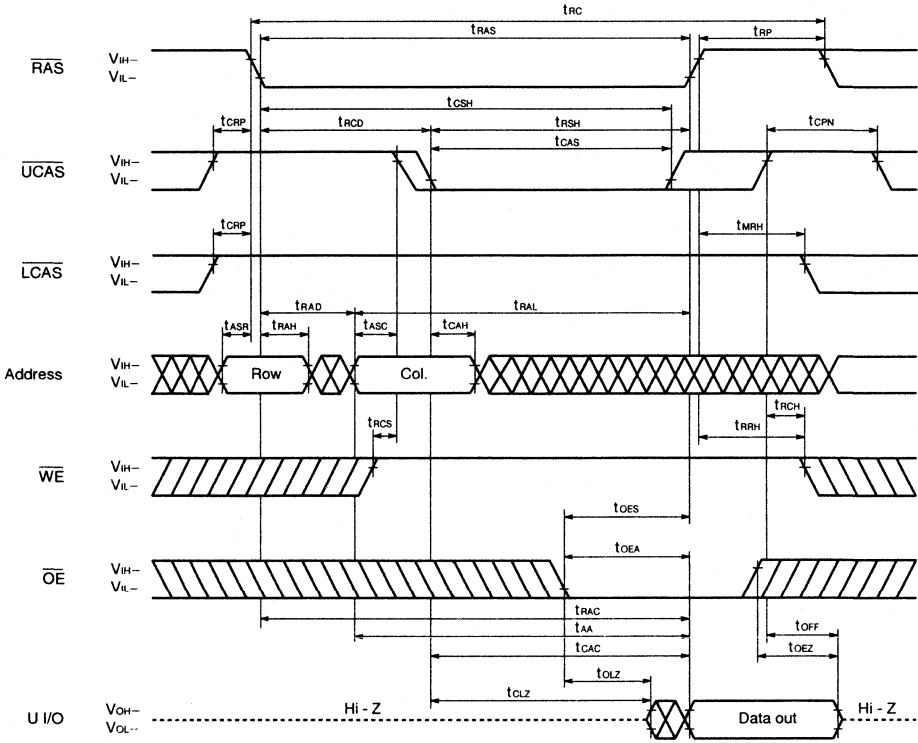
Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	–	5	–	5	–	ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10	–	10	–	10	–	ns	
RAS Precharge CAS Hold Time	t _{RPC}	10	–	10	–	10	–	ns	
RAS Pulse Width (CAS before RAS Self Refresh Cycle)	t _{RASS}	100	–	100	–	100	–	μs	1
RAS Precharge Time (CAS before RAS Self Refresh Cycle)	t _{RPS}	130	–	150	–	180	–	ns	1
CAS Hold Time (CAS before RAS Self Refresh Cycle)	t _{CHS}	–50	–	–50	–	–50	–	ns	1
WE Hold Time (Hidden Refresh Cycle)	t _{WHR}	15	–	15	–	20	–	ns	

Note 1. This specification is applied only for the μPD42S4260L.

Read Cycle

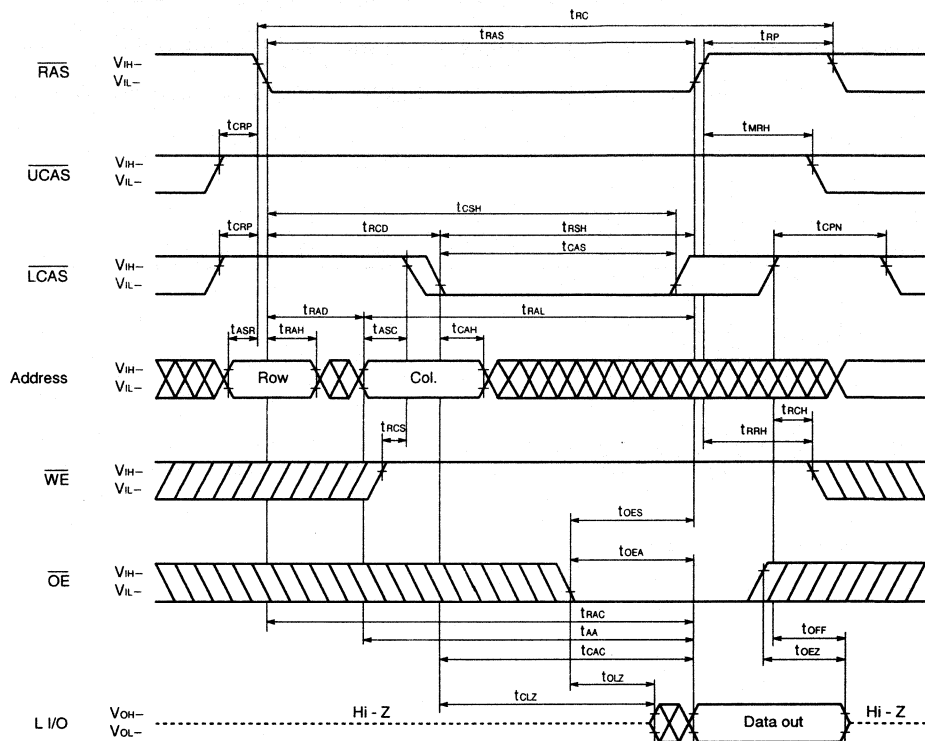


Upper Byte Read Cycle



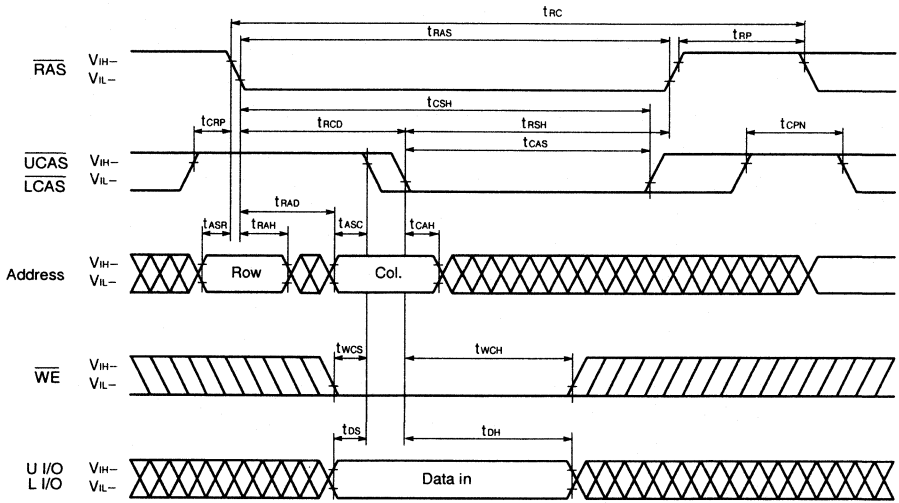
Remark L I/O : Hi-Z

Lower Byte Read Cycle



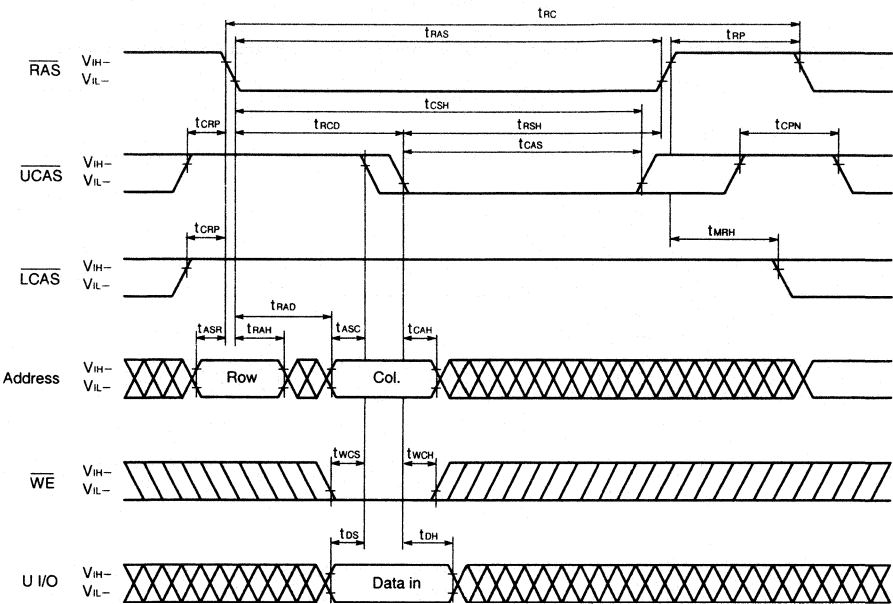
Remark U I/O : Hi-Z

Early Write Cycle



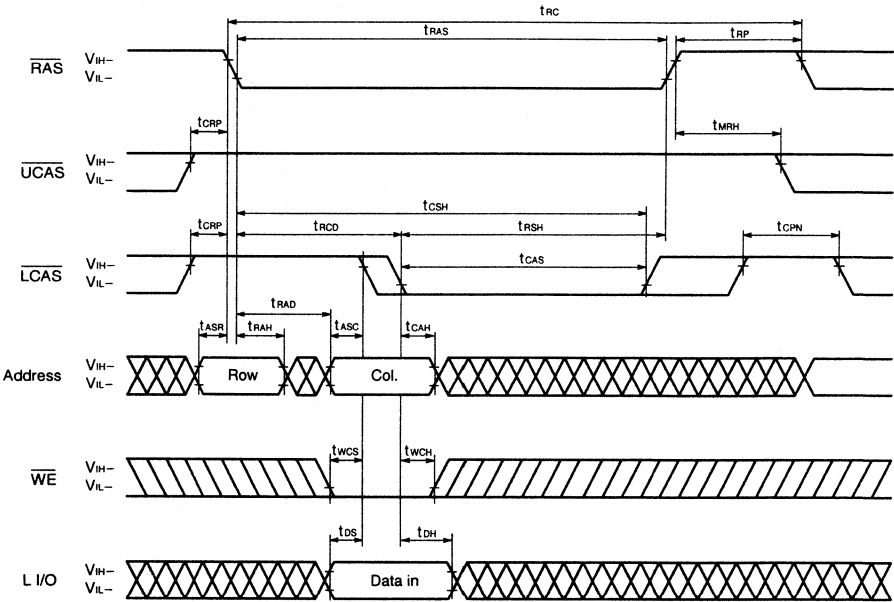
Remark $\overline{\text{OE}}$: Don't care

Upper Byte Early Write Cycle



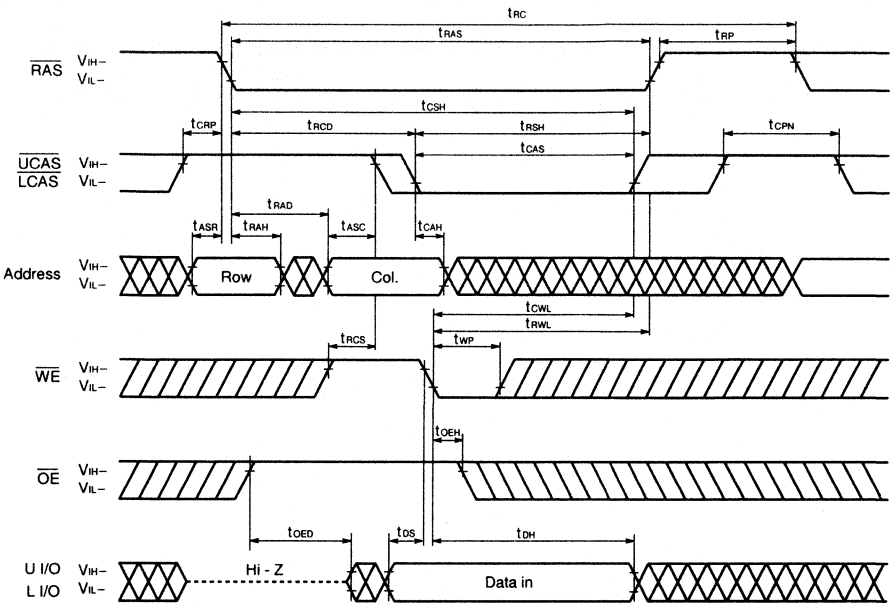
Remark $\overline{OE}$, L I/O : Don't care

Lower Byte Early Write Cycle

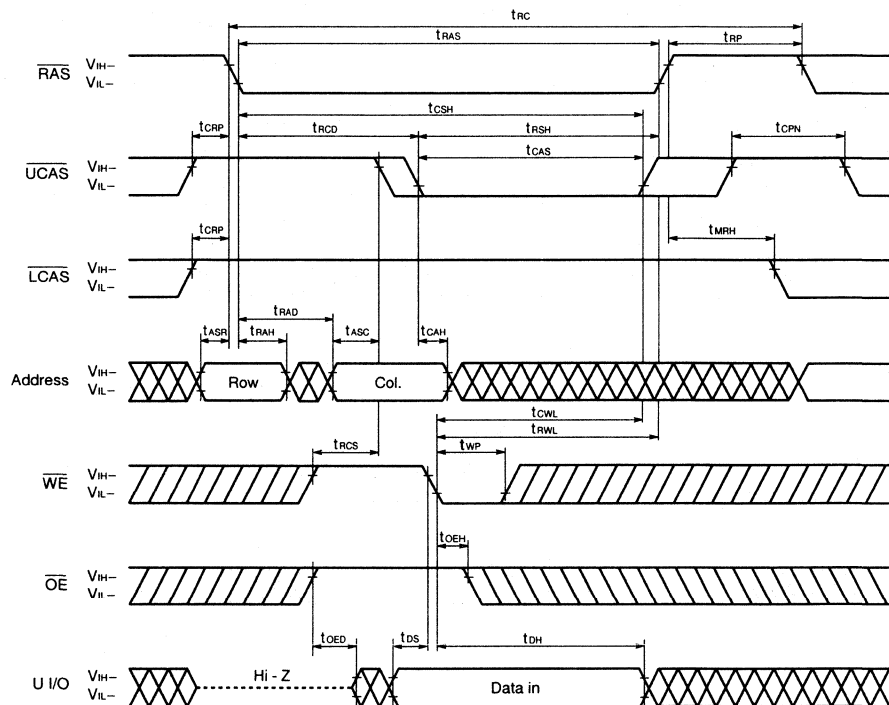


Remark $\overline{OE}$, U I/O : Don't care

Late Write Cycle

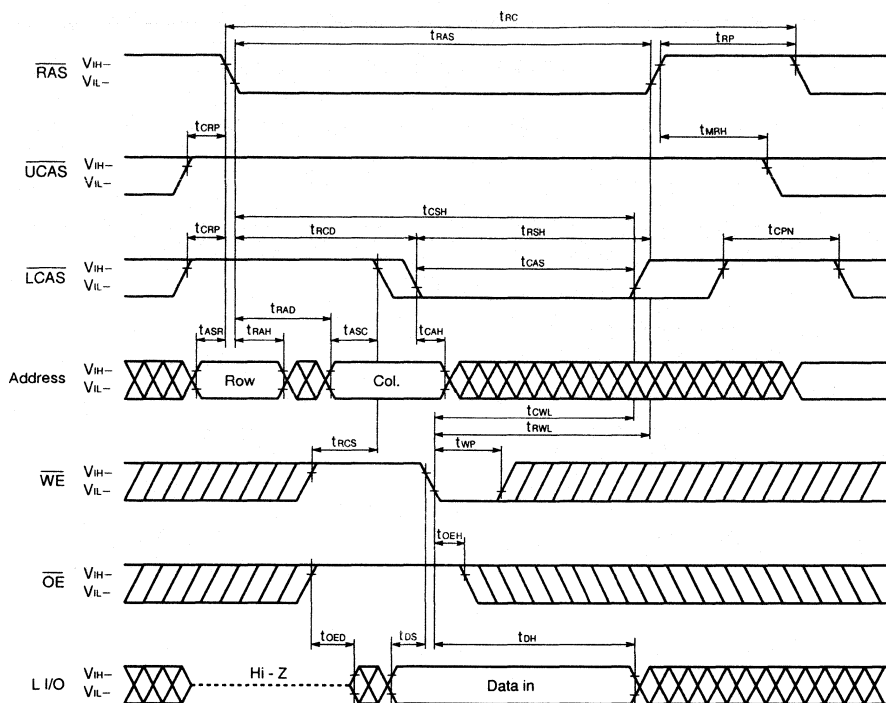


Upper Byte Late Write Cycle



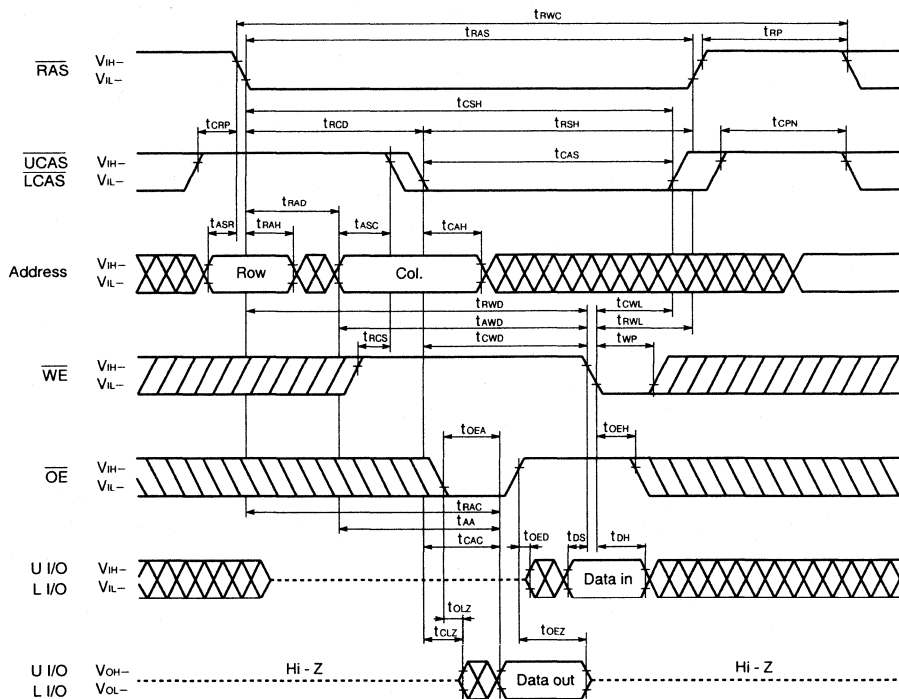
Remark L I/O : Don't care

Lower Byte Late Write Cycle

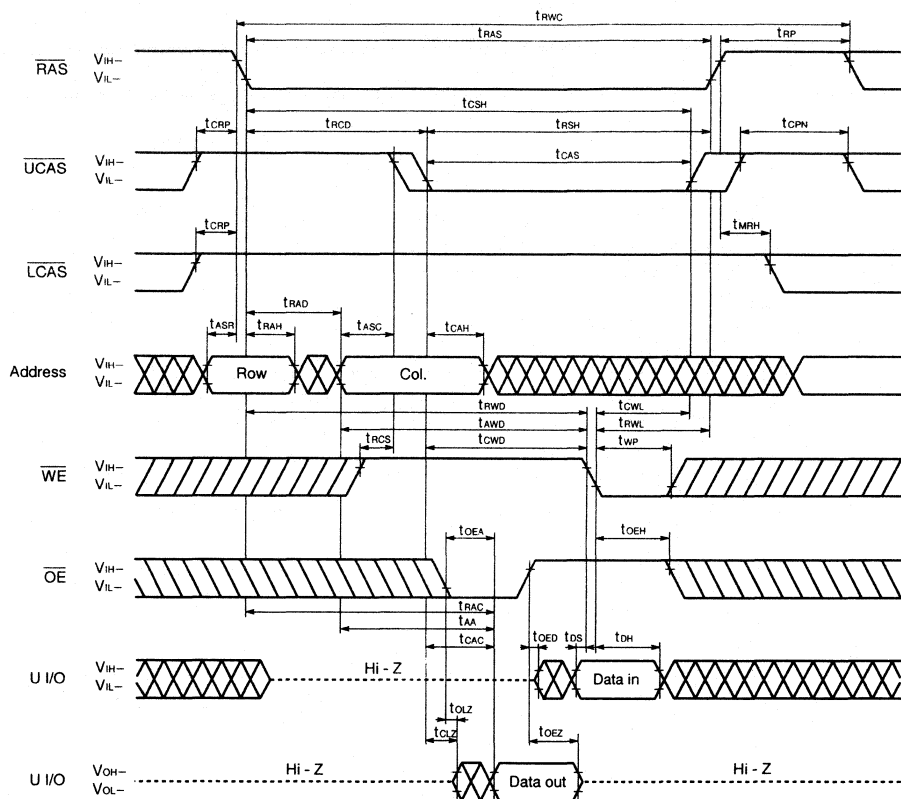


Remark U I/O : Don't care

★ Read Modify Write Cycle

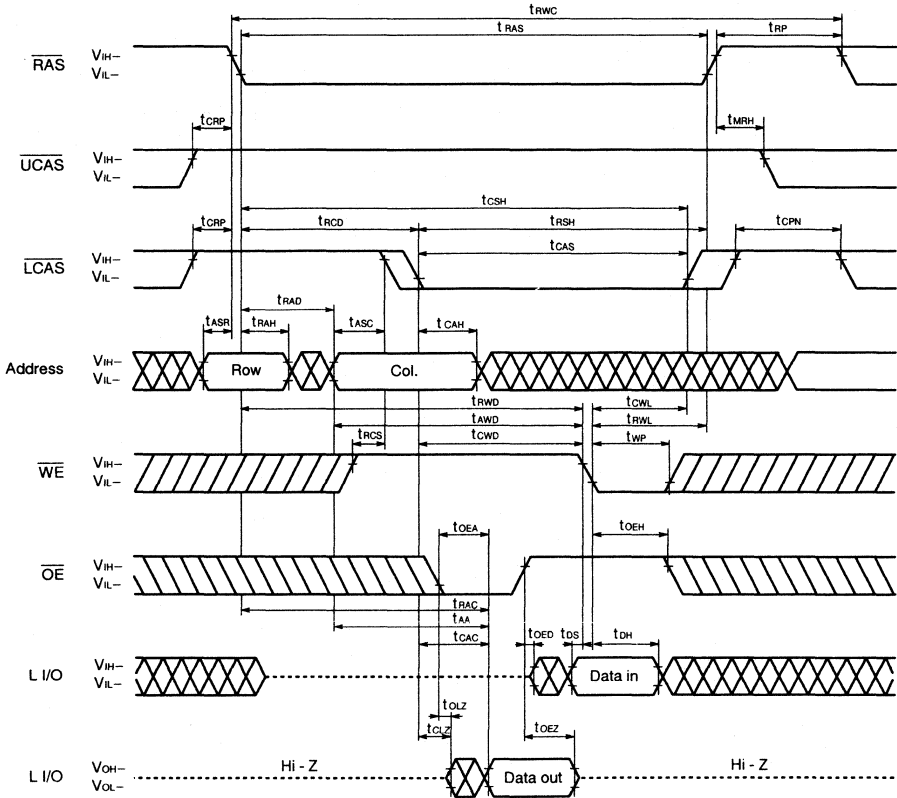


Upper Byte Read Modify Write Cycle



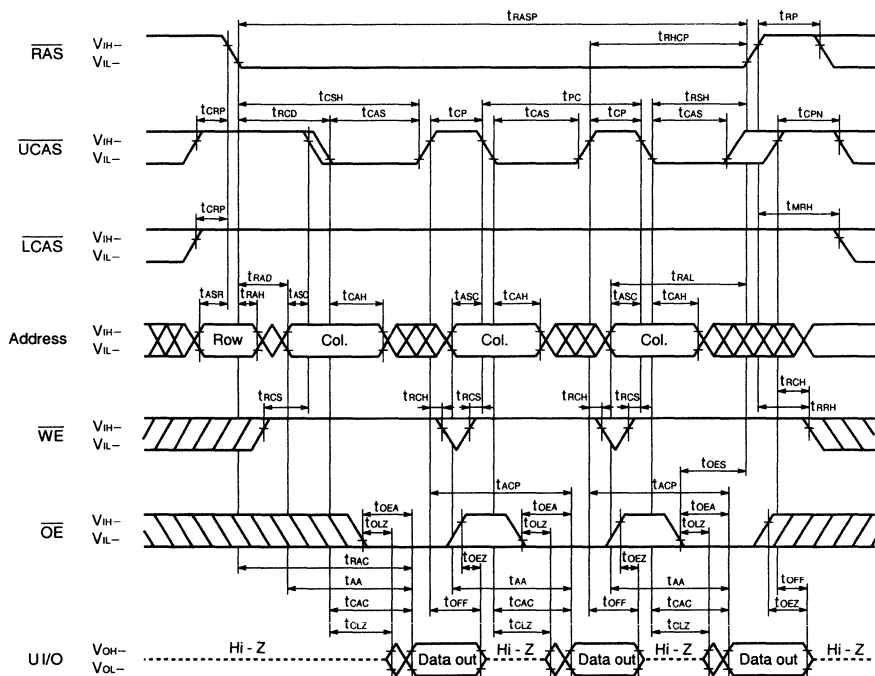
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

★ Lower Byte Read Modify Write Cycle



Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

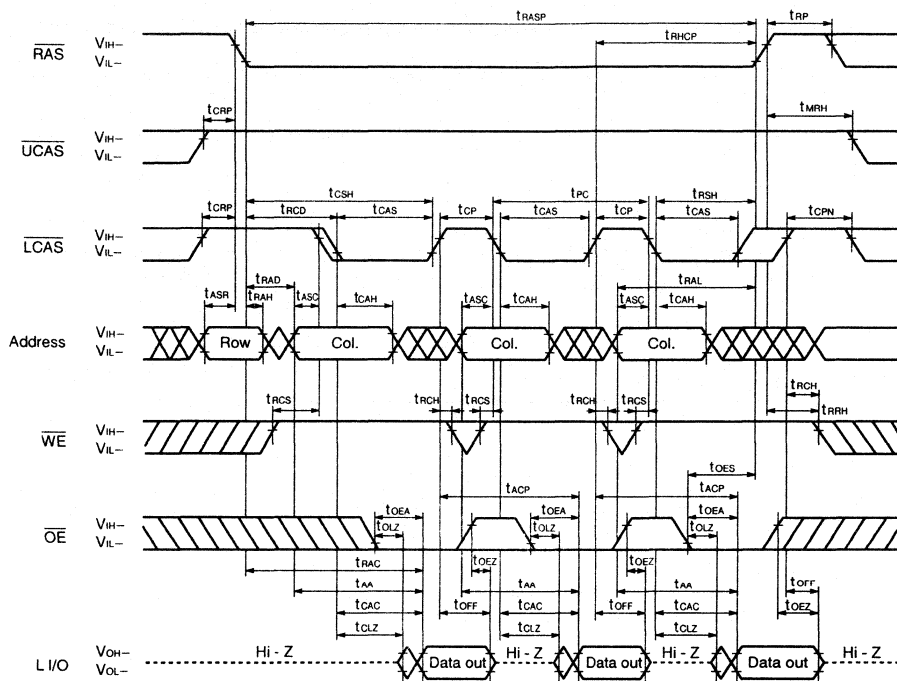
Fast Page Mode Upper Byte Read Cycle



Remark L I/O : Hi-Z

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

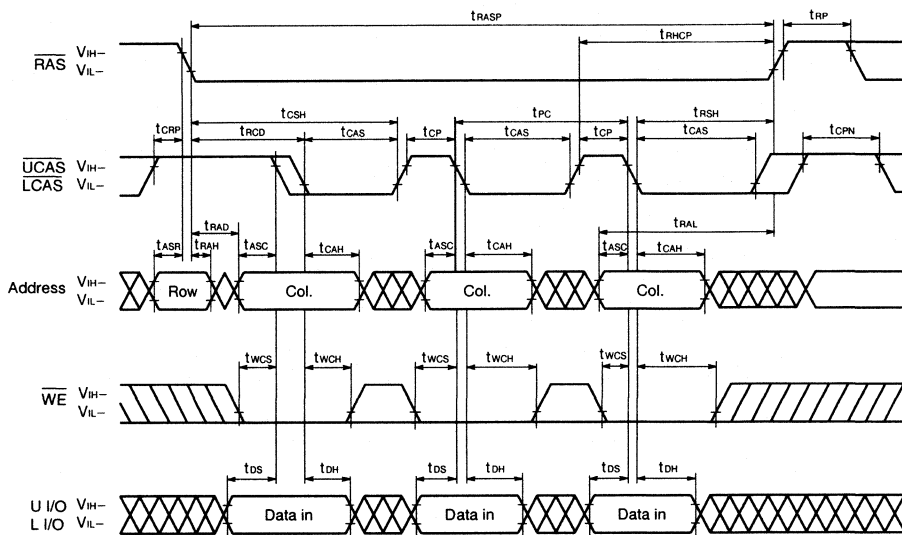
Fast Page Mode Lower Byte Read Cycle



Remark U I/O : Hi-Z

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

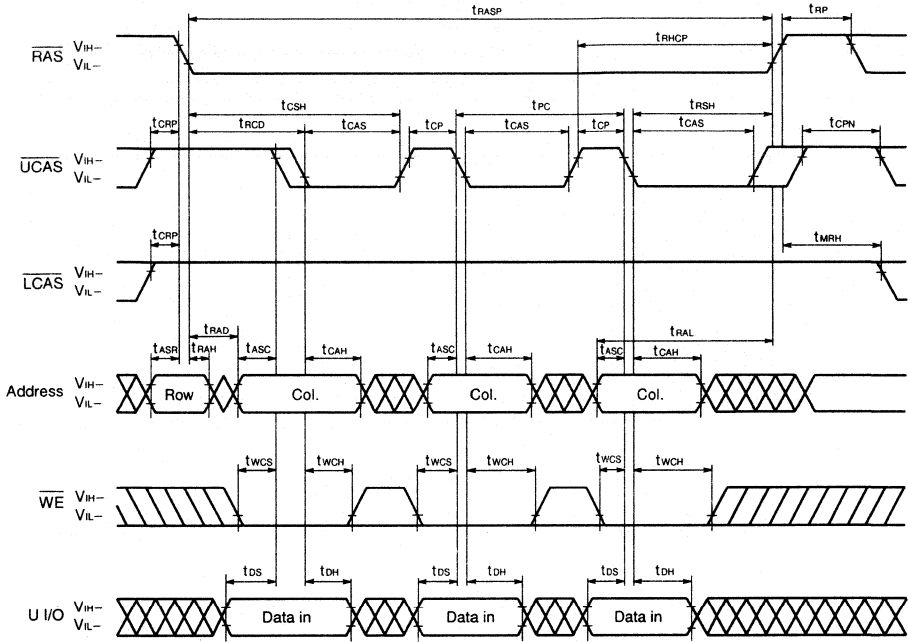
Fast Page Mode Early Write Cycle



Remark $\overline{\text{OE}}$: Don't care

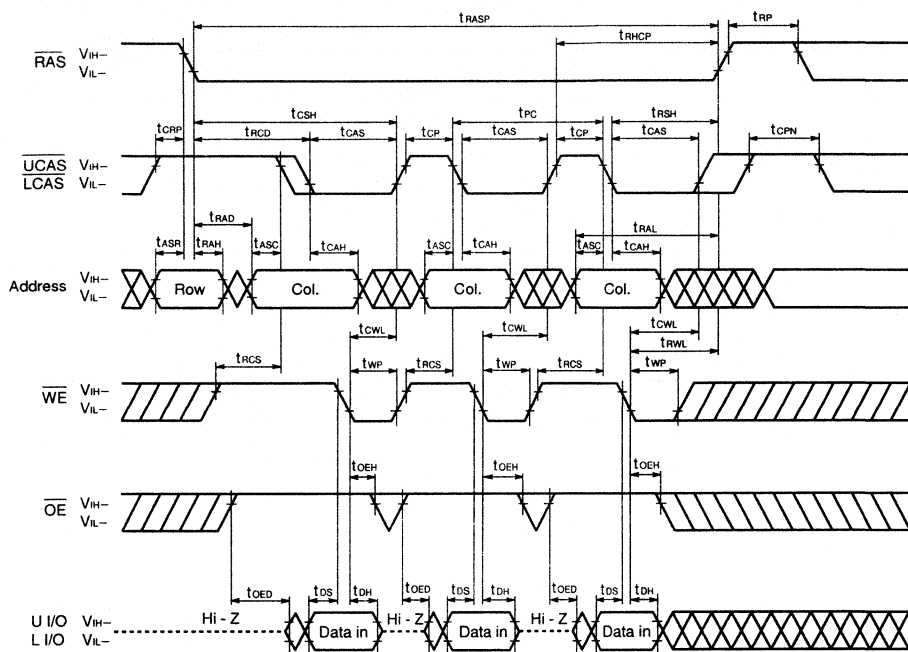
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Upper Byte Early Write Cycle



Remark $\overline{\text{OE}}$, L/I/O : Don't care
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Late Write Cycle

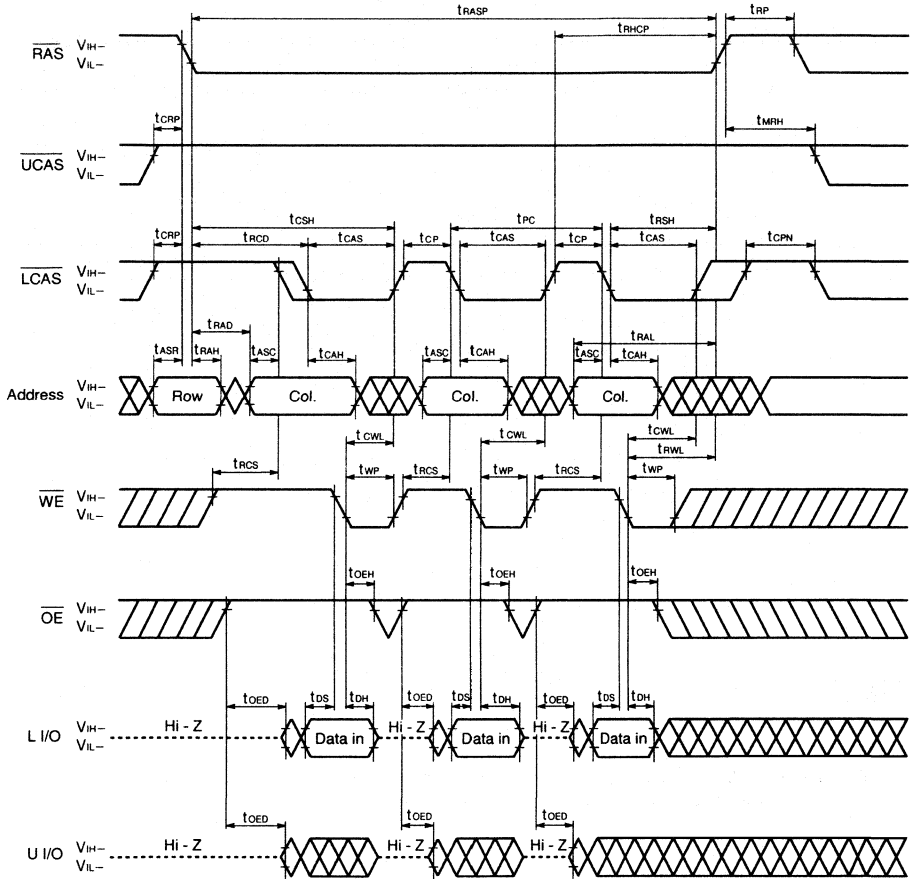


Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

[illegible]

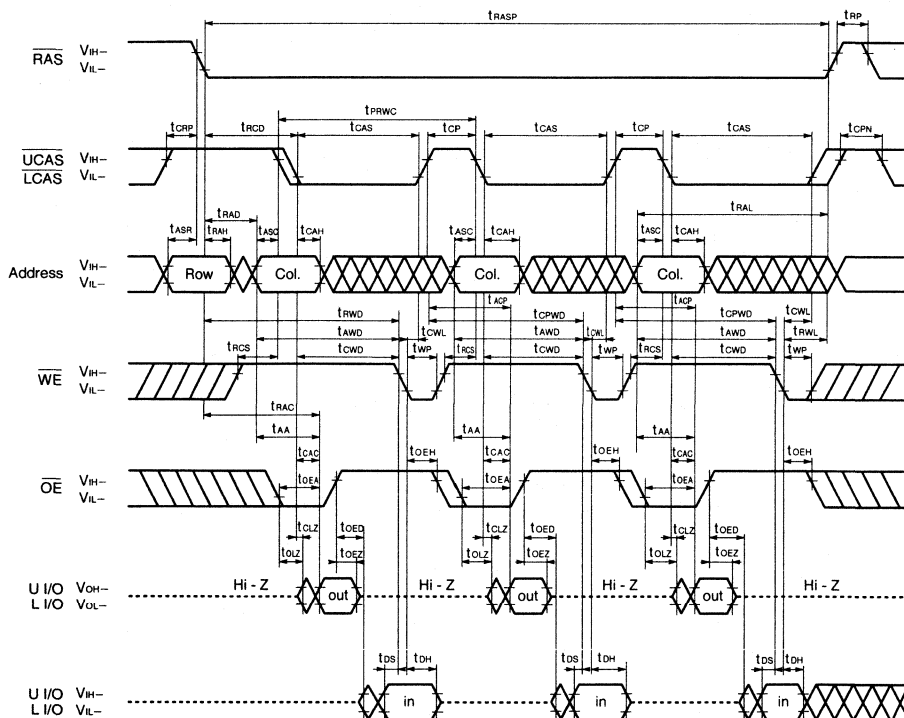
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Lower Byte Late Write Cycle



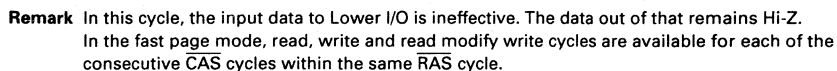
Remark In this cycle, the input data to Upper I/O is ineffective.
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

★ Fast Page Mode Read Modify Write Cycle

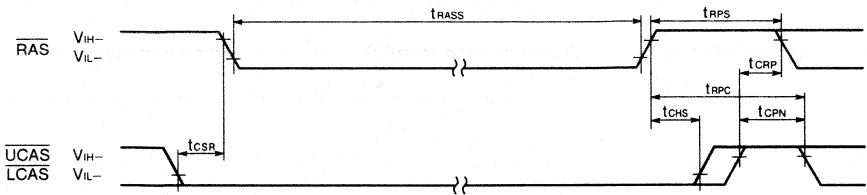


Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

★



CAS Before RAS Self Refresh Cycle (Only for the μPD42S4260L)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Cautions on Use of CAS Before RAS Self Refresh



CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

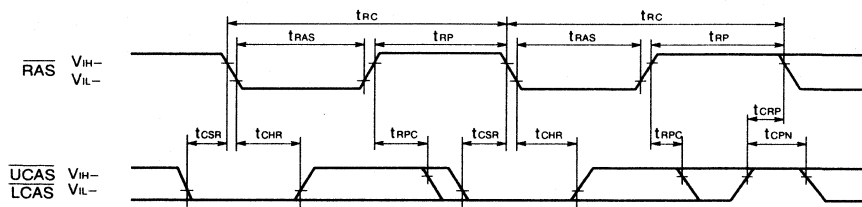
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 512 times within a 8 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh 512 times within an interval of 8 ms or less just before and after setting CAS before RAS self refresh.

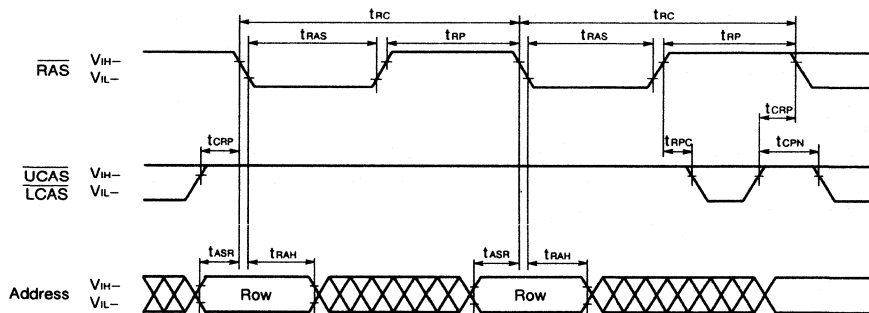
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



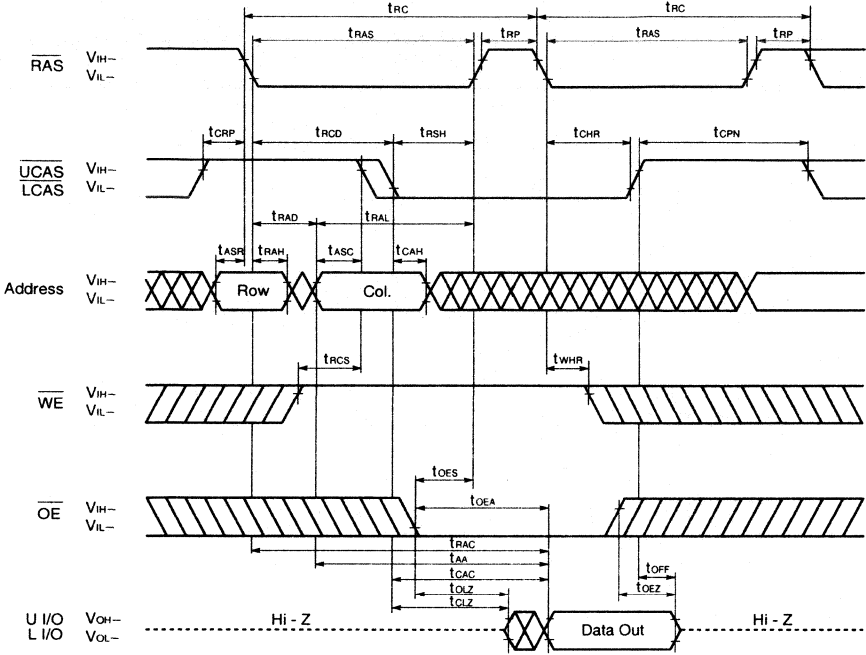
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

RAS Only Refresh Cycle

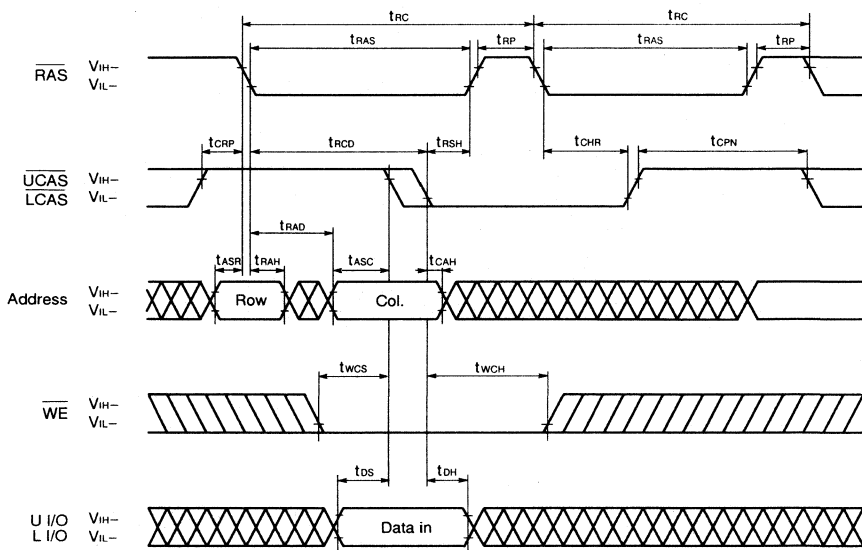


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

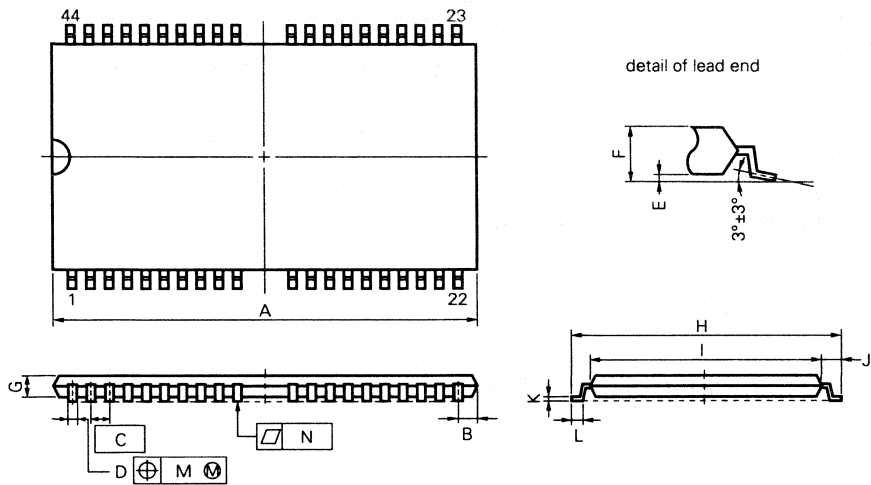


Remark $\overline{\text{OE}}$: Don't care



Package Drawings

44 PIN PLASTIC TSOP(III) (400 mil)

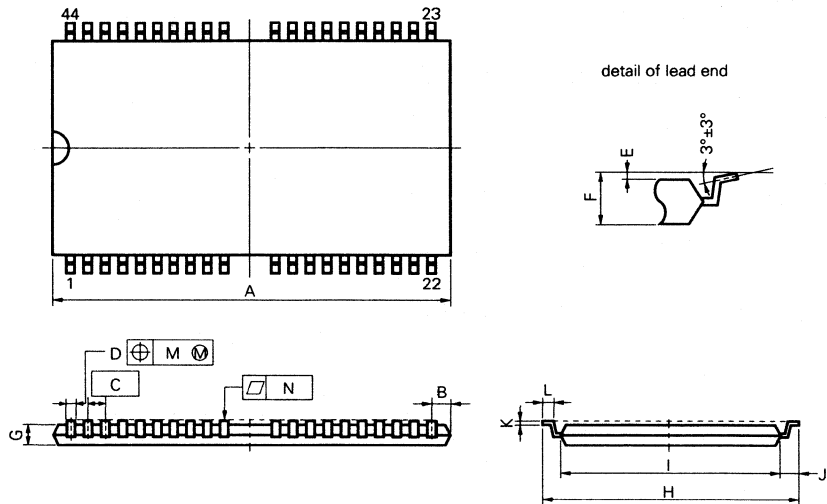


NOTE
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S44G5-80-7JF-1

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004

44 PIN PLASTIC TSOP(III) (400 mil)



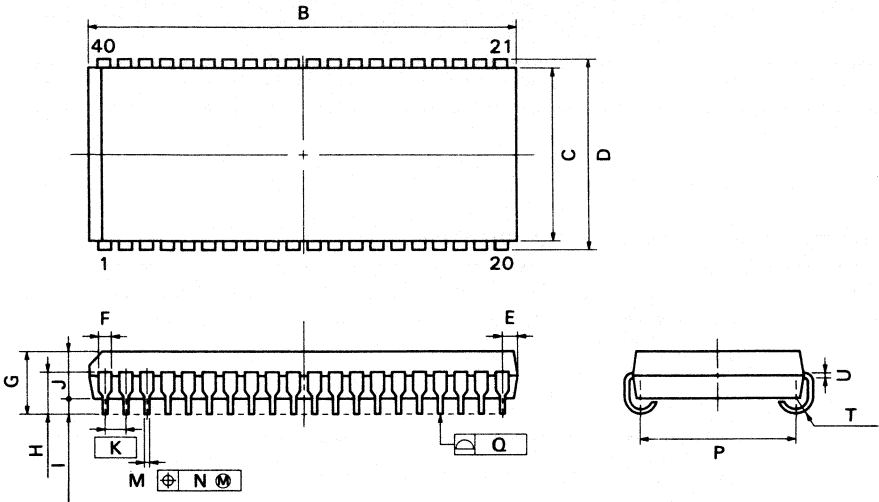
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S44G5-80-7KF-1

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.006}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004

40PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P40LE-400A-1

ITEM	MILLIMETERS	INCHES
B	26.29 ^{+0.2} _{-0.35}	1.035 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18 ^{±0.2}	0.440 ^{±0.008}
E	1.08 ^{±0.15}	0.043 ^{+0.008} _{-0.007}
F	0.7	0.028
G	3.5 ^{±0.2}	0.138 ^{±0.008}
H	2.4 ^{±0.2}	0.094 ^{+0.009} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40 ^{±0.10}	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4 ^{±0.20}	0.370 ^{±0.008}
Q	0.15	0.006
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.08}	0.008 ^{+0.004} _{-0.002}

★ Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met when soldering μPD42S4260L, 424260L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S4260LG5, 424260LG5 : 44-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S4260LLE, 424260LLE : 44-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	—

Note Exposure limit before soldering after dry-pack package is opened.
 Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

Synchronous DRAM



16M-bit Synchronous DRAM**Description**

The μ PD4516421, 4516821, 4516161 are high-speed 16,777,216-bit synchronous dynamic random-access memories, organized as 2,097,152 $\times$ 4 $\times$ 2, 1,048,576 $\times$ 8 $\times$ 2 and 524,288 $\times$ 16 $\times$ 2 (word $\times$ bit $\times$ bank), respectively.

The synchronous DRAMs achieve high-speed data transfer using the pipeline architecture.

All inputs and outputs are synchronized with the positive edge of the clock.

The synchronous DRAMs compatible with Low Voltage TTL (LVTTTL).

The synchronous DRAMs are packaged in 44-pin TSOP (II) ($\times$ 4, $\times$ 8) and 50-pin TSOP (II) ($\times$ 16).

Features

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A11 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 Full Page)
- Programmable wrap sequence (Sequential/Interleave)
- Programmable $\overline{\text{CAS}}$ latency (1, 2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- $\times$ 4, $\times$ 8, $\times$ 16 organization
- Single +3.3 $\pm$ 0.3 V power supply
- LVTTTL compatible
- Byte control ($\times$ 16) by LDQM and UDQM
- 2,048 refresh cycles/32ms
- Burst termination by Burst Stop command and Precharge command

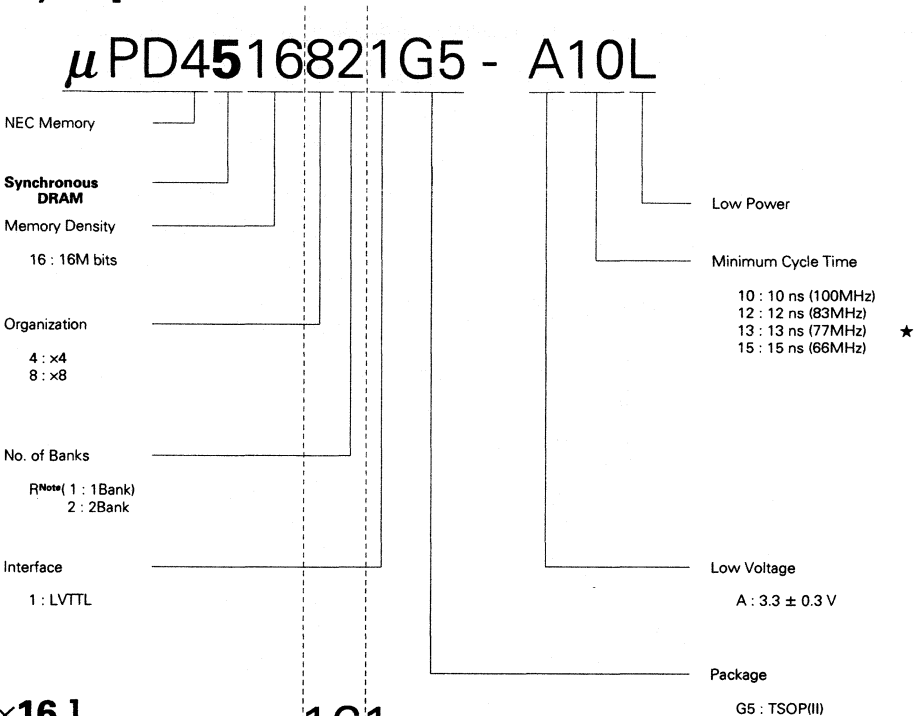
The information in this document is subject to change without notice.

★ Ordering Information

Part number	Organization (word × bit × bank)	Clock frequency MHz (MAX.)	Package
μPD4516421G5-A10-7JF	2M×4×2	100	44-pin Plastic TSOP(II) (400mil)
μPD4516421G5-A12-7JF		83	
μPD4516421G5-A13-7JF		77	
μPD4516421G5-A15-7JF		66	
μPD4516821G5-A10-7JF	1M×8×2	100	44-pin Plastic TSOP(II) (400mil)
μPD4516821G5-A12-7JF		83	
μPD4516821G5-A13-7JF		77	
μPD4516821G5-A15-7JF		66	
μPD4516161G5-A10-7JF	512K×16×2	100	50-pin Plastic TSOP(II) (400mil)
μPD4516161G5-A12-7JF		83	
μPD4516161G5-A13-7JF		77	
μPD4516161G5-A15-7JF		66	

Part Number

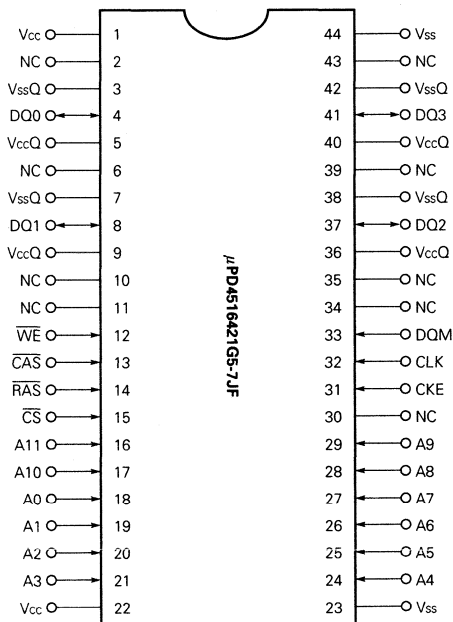
[×4, ×8]



★ Pin Configurations

[μPD4516421]

44-pin Plastic TSOP(II) (400 mil)



A0 to A11^{Note} : Address inputs

DQ0 to DQ3 : Data inputs/outputs

CLK : System clock input

CKE : Clock enable

CS : Chip select

RAS : Row address strobe

CAS : Column address strobe

WE : Write enable

DQM : DQ mask enable

Vcc : Supply voltage

Vss : Ground

VccQ : Supply voltage for DQ

VssQ : Ground for DQ

NC : No connection

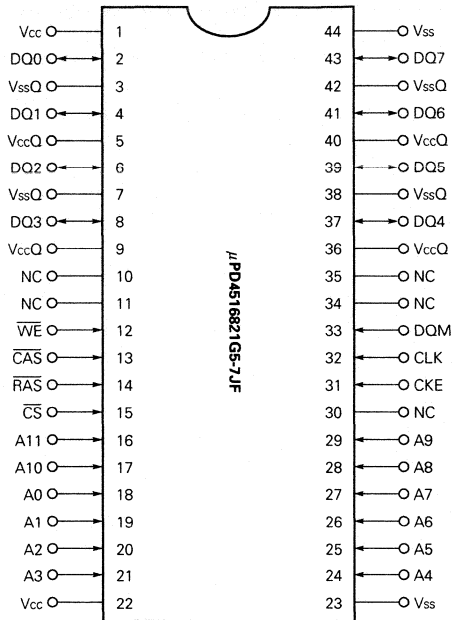
Note A0 to A10: Row address inputs

A0 to A9 : Column address inputs

A11 : Bank select

[μPD4516821]

44-pin Plastic TSOP(II) (400 mil)

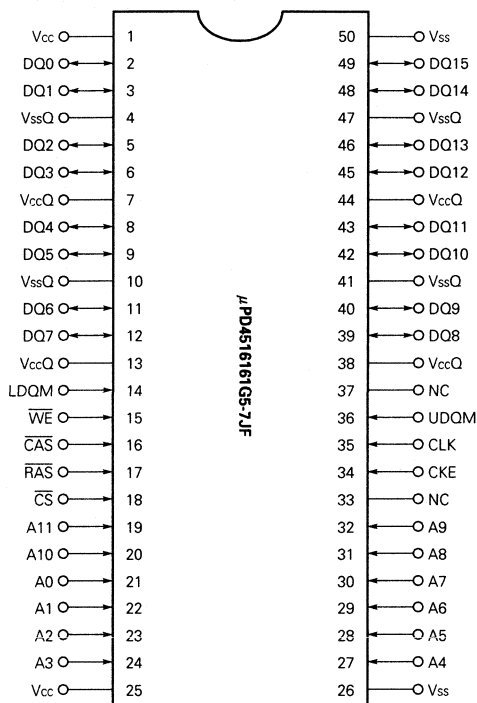


- A0 to A11 : Address inputs
- DQ0 to DQ7 : Data inputs/outputs
- CLK : System clock input
- CKE : Clock enable
- CS : Chip select
- RAS : Row address strobe
- CAS : Column address strobe
- WE : Write enable
- DQM : DQ mask enable
- Vcc : Supply voltage
- Vss : Ground
- VccQ : Supply voltage for DQ
- VssQ : Ground for DQ
- NC : No connection

Note A0 to A10: Row address inputs
A0 to A8 : Column address inputs
A11 : Bank select

[μ PD4516161]

50-pin Plastic TSOP(II) (400 mil)



A0 to A11 : Address inputs
 DQ0 to DQ15 : Data inputs/outputs
 CLK : System clock input
 CKE : Clock enable
 $\overline{CS}$: Chip select
 $\overline{RAS}$: Row address strobe
 $\overline{CAS}$: Column address strobe
 $\overline{WE}$: Write enable
 UDQM : Upper DQ mask enable
 LDQM : Lower DQ mask enable
 V_{cc} : Supply voltage
 V_{ss} : Ground
 $V_{cc}Q$: Supply voltage for DQ
 $V_{ss}Q$: Ground for DQ
 NC : No connection

Note A0 to A10: Row address inputs
 A0 to A7 : Column address inputs
 A11 : Bank select

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1. Input/Output Pin Function

Pin name	Input/Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not asserted and the μ PD4516xxx suspends operation. When the μ PD4516xxx is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.
$\overline{CS}$	Input	$\overline{CS}$ low starts the command input cycle. When $\overline{CS}$ is high, commands are ignored but operations continue.
RAS, $\overline{CAS}$, $\overline{WE}$	Input	RAS, $\overline{CAS}$ and $\overline{WE}$ have the same symbols on conventional DRAM but different functions. For details, refer to the command table.
A0 - A11	Input	Row Address is determined by A0 - A10 at the CLK (clock) rising edge in the activate command cycle. It does not depend on the bit organization. Column Address is determined by A0 - A9 at the CLK rising edge in the read or write command cycle. It depends on the bit organization: A0 - A9 for $\times 4$ device, A0 - A8 for $\times 8$ device and A0 - A7 for $\times 16$ device. A11 is the bank select signal (BS). In command cycle, A11 low selects bank A and A11 high selects bank B. A10 defines the precharge mode. When A10 is high in the precharge command cycle, both banks are precharged; when A10 is low, only the bank selected by A11 is precharged. When A10 high in read or write command cycle, the precharge start automatically after the burst access.
DQM UDQM LDQM	Input	DQM controls I/O buffers. In $\times 16$ products, UDQM and LDQM control upper byte and lower byte I/O buffers, respectively. In read mode, DQM controls the output buffers like a conventional $\overline{OE}$ pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ15	Input/Output	DQ pins have the same function as I/O pins on a conventional DRAM.
Vcc Vss VccQ VssQ	(Power supply)	Vcc and Vss are power supply pins for internal circuits. VccQ and VssQ are power supply pins for the output buffers.

2. Commands

Mode register set command

$$(\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE} = \text{Low})$$

The μPD4516xxx has a mode register that defines how the device operates. In this command, A0 through A11 are the data input pins. After power on, the mode register set command must be executed to initialize the device.

The mode register can be set only when both banks are in idle state.

During the two cycles following this command, the μPD4516xxx cannot accept any other commands.

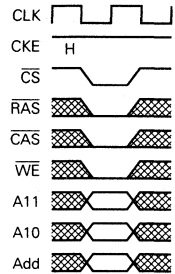


Fig. 1 Mode register set command

Activate command

$$(\overline{CS}, \overline{RAS} = \text{Low}, \overline{CAS}, \overline{WE} = \text{High})$$

The μPD4516xxx has two banks, each with 2048 rows.

This command activates the bank selected by A11 (BS) and a row address selected by A0 through A10.

This command corresponds to a conventional DRAM's $\overline{RAS}$ falling.

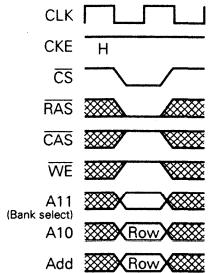


Fig. 2 Row address strobe and bank active command

Precharge command

$$(\overline{CS}, \overline{RAS}, \overline{WE} = \text{Low}, \overline{CAS} = \text{High})$$

This command begins precharge operation of the bank selected by A11 (BS) and A10. When A10 is High, both banks are precharged, regardless of A11. When A10 is Low, only the bank selected by A11 is precharged. A11 low selects bank A and A11 high selects bank B.

After this command, the μPD4516xxx can't accept the activate command to the precharging bank during t_{RP} (precharge to activate command period).

This command corresponds to a conventional DRAM's RAS rising.

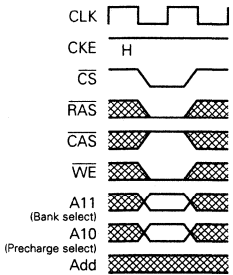


Fig. 3 Precharge command

Write command

$(\overline{CS}, \overline{CAS}, \overline{WE} = \text{Low}, \overline{RAS} = \text{High})$

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data must be input with this write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.

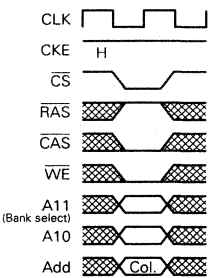


Fig. 4 Column address and write command

Read command

$(\overline{CS}, \overline{CAS} = \text{Low}, \overline{RAS}, \overline{WE} = \text{High})$

This command sets the burst start address given by the column address. Read data is available after $\overline{CAS}$ latency requirements have been met.

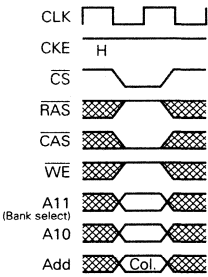


Fig. 5 Column address and read command

CBR (auto) refresh command

$(\overline{CS}, \overline{RAS}, \overline{CAS} = \text{Low}, \overline{WE}, \text{CKE} = \text{High})$

This command is a request to begin the CBR refresh operation. The refresh address and the bank select address are generated internally. Before executing CBR refresh, both banks must be precharged. After this cycle, both banks will be in the idle (precharged) state and ready for a row activate command. During t_{AC} period (from refresh command to refresh or activate command), the μPD4516xxx cannot accept any other command.

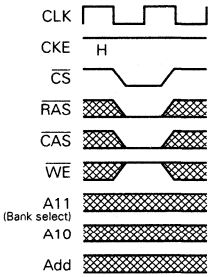


Fig. 6 Auto refresh command

Self refresh entry command

($\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, CKE = Low, $\overline{\text{WE}}$ = High)

After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the μPD4516xxx exits the self refresh mode.

During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.

Before executing self refresh, both banks must be precharged.

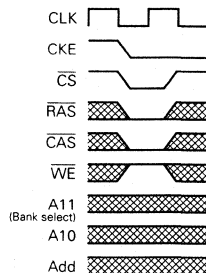


Fig. 7 Self refresh entry command

Burst stop command

($\overline{\text{CS}}$, $\overline{\text{WE}}$ = Low, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = High)

This command terminates the current burst operation.

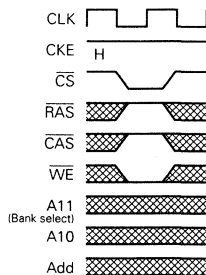


Fig. 8 Burst stop command in Full Page mode

No operation

($\overline{\text{CS}}$ = Low, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ = High)

This command is not a execution command. No operations begin or terminate by this command.

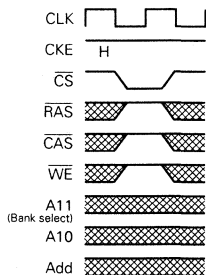
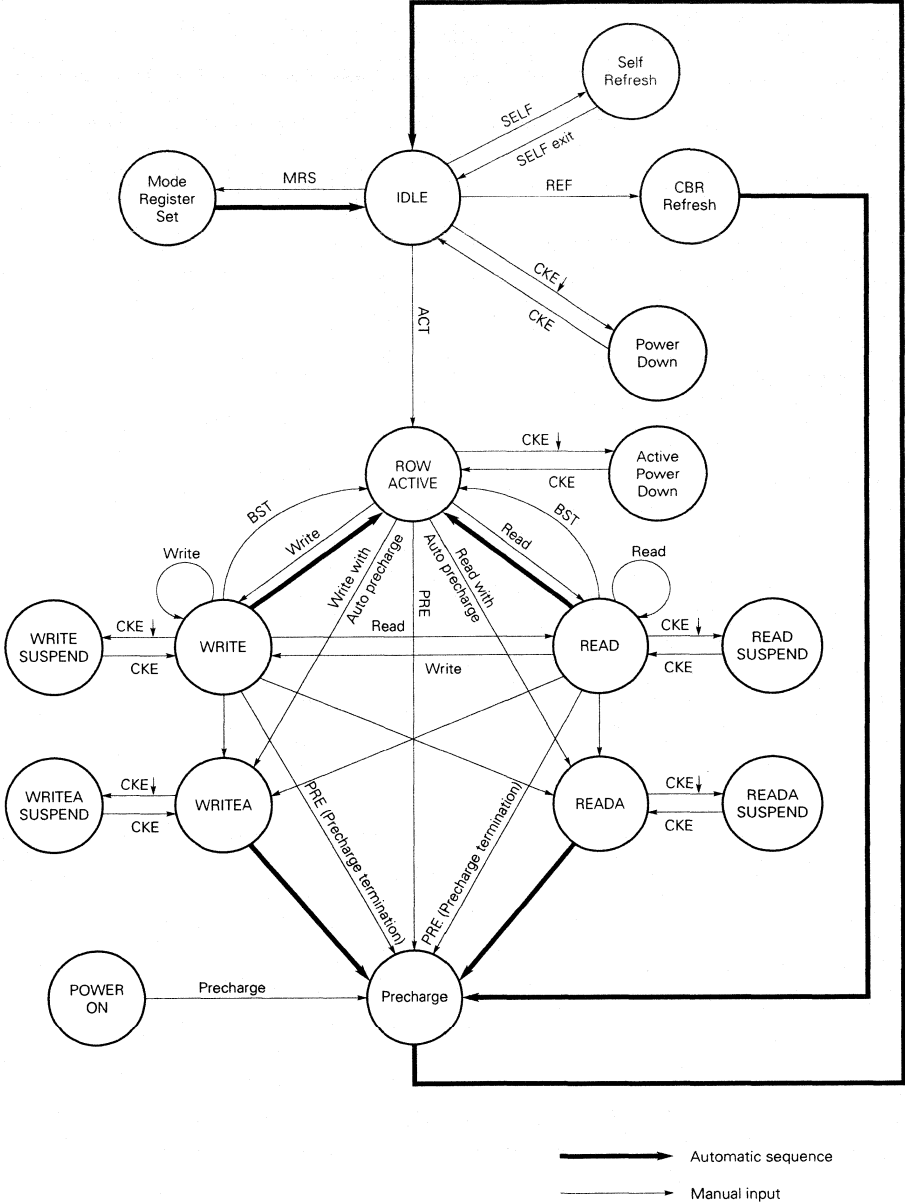


Fig. 9 No operation

3. Simplified State Diagram



4. Truth Table

4.1 Command Truth Table

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9-A0
		n-1	n							
Device deselect	DESL	H	x	H	x	x	x	x	x	x
No operation	NOP	H	x	L	H	H	H	x	x	x
Burst stop	BST	H	x	L	H	H	L	x	x	x
Read	READ	H	x	L	H	L	H	V	L	V
Read with auto precharge	READA	H	x	L	H	L	H	V	H	V
Write	WRIT	H	x	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	x	L	H	L	L	V	H	V
Bank activate	ACT	H	x	L	L	H	H	V	V	V
Precharge select bank	PRE	H	x	L	L	H	L	V	L	x
Precharge all banks	PALL	H	x	L	L	H	L	x	H	x
Mode register set	MRS	H	x	L	L	L	L	L	L	V

4.2 DQM Truth Table

Function	Symbol	CKE		DQM	
		n-1	n	U	L
Data write/output enable	ENB	H	x	L	
Data mask/output disable	MASK	H	x	H	
Upper byte write enable/output enable	ENBU	H	x	L	x
Lower byte write enable/output enable	ENBL	H	x	x	L
Upper byte write inhibit/output disable	MASKU	H	x	H	x
Lower byte write inhibit/output disable	MASKL	H	x	x	H

4.3 CKE Truth Table

Current state	Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
			n-1	n					
Activating	Clock suspend mode entry		H	L	x	x	x	x	x
Any	Clock suspend		L	L	x	x	x	x	x
Clock suspend	Clock suspend mode exit		L	H	x	x	x	x	x
Idle	CBR refresh command	REF	H	H	L	L	L	H	x
Idle	Self refresh entry	SELF	H	L	L	L	L	H	x
Self refresh	Self refresh exit		L	H	L	H	H	H	x
			L	H	H	x	x	x	x
Idle	Power down entry		H	L	x	x	x	x	x
Power down	Power down exit		L	H	x	x	x	x	x

H: High level, L: Low level

x: High or Low level (Don't care), V: Valid Data input

4.4 Operative Command Table^{Notes 1, 2}

(1/3)

Current state	CS	RAS	CAS	WE	Address	Command	Action	Notes
Idle	H	x	x	x	x	DESL	Nop or Power down	3
	L	H	H	x	x	NOP or BST	Nop or Power down	3
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	Row active	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	x	REF/SELF	Refresh or Self refresh	5
Row active	L	L	L	L	Op Code	MRS	Mode register access	
	H	x	x	x	x	DESL	Nop	
	L	H	H	x	x	NOP or BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read:Determine AP	6
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write:Determine AP	6
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Precharge	7
Read	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	H	x	x	x	x	DESL	Continue burst to end → Row active	
	L	H	H	H	x	NOP	Continue burst to end → Row active	
	L	H	H	L	x	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, new read:Determine AP	8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, start write:Determine AP	8, 9
Write	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	H	x	x	x	x	DESL	Continue burst to end → Write recovering	
	L	H	H	H	x	NOP	Continue burst to end → Write recovering	
	L	H	H	L	x	BST	Burst stop → Row active	
Write	L	H	L	H	BA, CA, A10	READ/READA	Term burst, start read:Determine AP	8, 9
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, new write:Determine AP	8
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Term burst precharging	10
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(2/3)

Current state	CS	RAS	CAS	WE	Address	Command	Action	Notes
Read with auto precharge	H	x	x	x	x	DESL	Continue burst to end → Precharging	
	L	H	H	H	x	NOP	Continue burst to end → Precharging	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
Write with auto precharge	L	L	L	L	Op-Code	MRS	ILLEGAL	
	H	x	x	x	x	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	x	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
Precharging	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	H	x	x	x	x	DESL	Nop → Enter idle after t _{NP}	
	L	H	H	H	x	NOP	Nop → Enter idle after t _{NP}	
	L	H	H	L	x	BST	Nop → Enter idle after t _{NP}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
Row activating	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t _{NP}	
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	H	x	x	x	x	DESL	Nop → Enter row active after t _{RCO}	
	L	H	H	H	x	NOP	Nop → Enter row active after t _{RCO}	
	L	H	H	L	x	BST	Nop → Enter row active after t _{RCO}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4, 11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(3/3)

Current state	CS	RAS	CAS	WE	Address	Command	Action	Notes
Write recovering	H	x	x	x	x	DESL	Nop → Enter row active after t_{0H}	
	L	H	H	H	x	NOP	Nop → Enter row active after t_{0H}	
	L	H	H	L	x	BST	Nop → Enter row active after t_{0H}	
	L	H	L	H	BA, CA, A10	READ/READA	Start read, Determine AP	9
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write, Determine AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write recovering with auto precharge	H	x	x	x	x	DESL	Nop → Enter precharge after t_{0H}	
	L	H	H	H	x	NOP	Nop → Enter precharge after t_{0H}	
	L	H	H	L	x	BST	Nop → Enter precharge after t_{0H}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4, 9
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refreshing	H	x	x	x	x	DESL	Nop → Enter idle after t_{0C}	
	L	H	H	x	x	NOP/BST	Nop → Enter idle after t_{0C}	
	L	H	L	x	x	READ/WRIT	ILLEGAL	
	L	L	H	x	x	ACT/PRE/PALL	ILLEGAL	
	L	L	L	x	x	REF/SELF/MRS	ILLEGAL	
Mode register accessing	H	x	x	x	x	DESL	Nop → Enter idle after 2 Clocks	
	L	H	H	H	x	NOP	Nop → Enter idle after 2 Clocks	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	x	x	READ/WRITE	ILLEGAL	
	L	L	x	x	x	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

- Notes**
1. H: High level, L: Low level, x: High or Low level (Don't care), V: Valid data input
 2. All entries assume that CKE was active (High level) during the preceding clock cycle.
 3. If both banks are idle, and CKE is inactive (Low level), μPD4516xxx will enter Power down mode. All input buffers except CKE will be disabled.
 4. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
 5. If both banks are idle, and CKE is inactive (Low level), μPD4516xxx will enter Self refresh mode. All input buffers except CKE will be disabled.
 6. Illegal if t_{RCD} is not satisfied.
 7. Illegal if t_{RAS} is not satisfied.
 8. Must satisfy burst interrupt condition.
 9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
 10. Must mask preceding data which don't satisfy t_{DPL} .
 11. Illegal if t_{RRD} is not satisfied.

4.5 Command Truth Table for CKE^{Note 1}

Current state	CKE n-1	CKE n	$\overline{CS}$	RAS	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
Self refresh (S.R.)	H	x	x	x	x	x	x	INVALID, CLK(n-1) would exit S.R.	
	L	H	H	x	x	x	x	S.R. Recovery	2
	L	H	L	H	H	x	x	S.R. Recovery	2
	L	H	L	H	L	x	x	ILLEGAL	2
	L	H	L	L	x	x	x	ILLEGAL	2
	L	L	x	x	x	x	x	Maintain S.R.	
Self refresh recovery	H	H	H	x	x	x	x	Idle after t_{AC}	
	H	H	L	H	H	x	x	Idle after t_{AC}	
	H	H	L	H	L	x	x	ILLEGAL	
	H	H	L	L	x	x	x	ILLEGAL	
	H	L	H	x	x	x	x	Begin clock suspend next cycle	5
	H	L	L	H	H	x	x	Begin clock suspend next cycle	5
	H	L	L	H	L	x	x	ILLEGAL	
	H	L	L	L	x	x	x	ILLEGAL	
	L	H	x	x	x	x	x	Exit clock suspend next cycle	2
Power down (P.D.)	L	L	x	x	x	x	x	Maintain clock suspend	
	H	x	x	x	x	x	x	INVALID, CLK(n-1) would exit P.D.	
	L	H	x	x	x	x	x	EXIT P.D. → Idle	2
Both banks idle	L	L	x	x	x	x	x	Maintain power down mode	
	H	H	H	x	x	x		Refer to operations in Operative Command Table	
	H	H	L	H	x	x		Refer to operations in Operative Command Table	
	H	H	L	L	H	x		Refer to operations in Operative Command Table	
	H	H	L	L	L	H	x	Refresh	
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	H	L	H	x	x	x		Refer to operations in Operative Command Table	
	H	L	L	H	x	x		Refer to operations in Operative Command Table	
	H	L	L	L	H	x		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	x	Self refresh	3
Any state other than listed above	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	L	x	x	x	x	x	x	Power down	3
	H	H	x	x	x	x	x	Refer to operations in Operative Command Table	
	H	L	x	x	x	x	x	Begin clock suspend next cycle	4
	L	H	x	x	x	x	x	Exit clock suspend next cycle	
	L	L	x	x	x	x	x	Maintain clock suspend	

Notes 1. H: High level, L: Low level, X: High or low level (Don't care)

2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.

3. Power down and Self refresh can be entered only from the both banks idle state.

4. Must be legal command as defined in Operative Command Table.

5. Illegal if t_{SREX} is not satisfied.

4.6 Command Truth Table for Two Banks Operation

CS	RAS	CAS	WE	BA	A10	A9 - A0	Action	"FROM" State	"TO" State
H	x	x	x	x	x	x	NOP	Any	Any
L	H	H	H	x	x	x	NOP	Any	Any
L	H	H	L	x	x	x	BST	(R/W/A)0(I/A)1	A0(I/A)1
								I0(I/A)1	I0(I/A)1
								(R/W/A)1(I/A)0	A1(I/A)0
								I1(I/A)0	I1(I/A)0
L	H	L	H	H	H	CA	Read	(R/W/A)1(I/A)0	RP1(I/A)0
				H	H	CA		A1(R/W)0	RP1A0
				H	L	CA		(R/W/A)1(I/A)0	R1(I/A)0
				H	L	CA		A1(R/W)0	R1A0
				L	H	CA		(R/W/A)0(I/A)1	RP0(I/A)1
				L	H	CA		A0(R/W)1	RP0A1
				L	L	CA		(R/W/A)0(I/A)1	R0(I/A)1
				L	L	CA		A0(R/W)1	R0A1
L	H	L	L	H	H	CA	Write	(R/W/A)1(I/A)0	WP1(I/A)0
				H	H	CA		A1(R/W)0	WP1A0
				H	L	CA		(R/W/A)1(I/A)0	W1(I/A)0
				H	L	CA		A1(R/W)0	W1A0
				L	H	CA		(R/W/A)0(I/A)1	WP0(I/A)1
				L	H	CA		A0(R/W)1	WP0A1
				L	L	CA		(R/W/A)0(I/A)1	W0(I/A)1
				L	L	CA		A0(R/W)1	W0A1
L	L	H	H	H	RA		Activate Row	I1Any0	A1Any0
				L	RA			I0Any1	A0Any1
L	L	H	L	x	H	x	Precharge	(R/W/A/I)0(I/A)1	I0I1
				x	H	x		(R/W/A/I)1(I/A)0	I1I0
				H	L	x		(R/W/A/I)1(I/A)0	I1(I/A)0
				H	L	x		(I/A)1(R/W/A/I)0	I1(R/W/A/I)0
				L	L	x		(R/W/A/I)0(I/A)1	I0(I/A)1
				L	L	x		(I/A)0(R/W/A/I)1	I0(R/W/A/I)1
L	L	L	H	x	x	x	Refresh	I0I1	I0I1
L	L	L	L	Op-Code			Mode Register Access	I0I1	I0I1

Notes 1. Logic level abbreviations

H: High level, L: Low level, x: High or low level (Don't care)

Pin name abbreviation

BA: Bank address (A11)

2. State abbreviations

I = Idle

A = Row active

R = Read with No precharge (No precharge is posted)

W = Write with No precharge (No precharge is posted)

RP = Read with auto precharge (Precharge is posted)

WP = Write with auto precharge (Precharge is posted)

Any = Any State

X0Y1 = Y1X0 = Bank0 is in state "X", Bank1 is in state "Y"

(X/Y)0Z1 = Z1(X/Y)0 = Bank0 is in state "X" or "Y", Bank1 is in state "Z"

3. If the μ PD4516xxx is in a state other than above listed in the "From State" column, the command is illegal.
4. The states listed under "To" might not be entered on the next clock cycle.
Timing restrictions apply.

5. Initialization

Synchronous DRAM must be initialized in the power on sequence, like conventional DRAM. Once power has been applied, a 100 μ s delay must precede any signals being toggled.

During this delay, CKE and DQM must be held high.

After the 100 μ s delay, both banks must be precharged using the precharge command. Once precharge is completed and the minimum t_{RP} is satisfied, the mode register can be programmed.

Two clocks after the Mode register set command, two CBR refresh command that satisfy the t_{RC} on each CBR refresh cycle must be performed.

6. Programming the Mode Register

The mode register is programmed by the Mode register set command using address bits A11 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields;

Options : A11 through A7
 $\overline{\text{CAS}}$ latency: A6 through A4
 Wrap type : A3
 Burst length: A2 through A0

Following mode register programming, no command can be asserted before at least two clocks have elapsed.

$\overline{\text{CAS}}$ Latency

$\overline{\text{CAS}}$ latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available. The NEC SDRAM is capable of reconfiguring its internal architecture based on the value of $\overline{\text{CAS}}$ latency.

The value is determined by the frequency of the clock and the speed grade of the device. The table on page 42 shows the relationship of $\overline{\text{CAS}}$ latency to the clock period and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become high impedance.

The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either "Sequential" or "Interleave". The method chosen will depend on the type of CPU in the system.

Some microprocessor cache system are optimized for sequential addressing and others for interleaved addressing. The table on the page 23 shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequential sequence supports the full page length.

7. Mode Register

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1							

JEDEC Standard Test Set (refresh counter test)

11	10	9	8	7	6	5	4	3	2	1	0
x	x	1	0	0	LTMODE		WT		BL		

Burst Read and Single Write
(for Write Through Cache)

11	10	9	8	7	6	5	4	3	2	1	0
			1	0							

Use in future

11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	1	1	V	V	V	V	V	V	V

Vender Specific

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	LTMODE		WT		BL		

Mode Register Set

V = Valid
x = Don't care

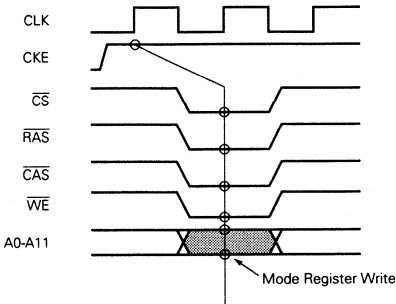
Burst length	Bits2-0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type	0	Sequential
	1	Interleave

Latency mode	Bits6-4	CAS latency
	000	R
	001	1
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R: Reserved

Mode Register Write Timing



7.1 Burst Length and Sequence

[Burst of Two]

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

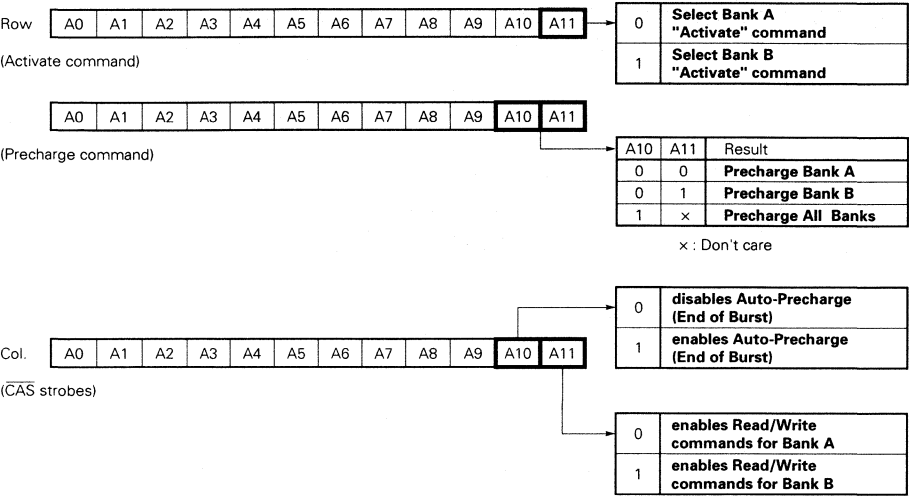
Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

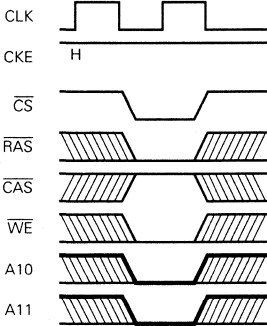
Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 512 (for 2M $\times$ 8 device), 1024 (for 4M $\times$ 4 device) and 256 (for 1M $\times$ 16 device).

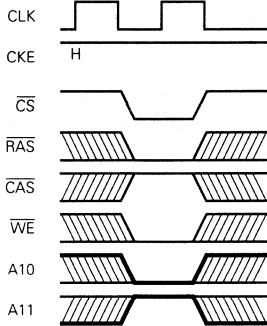
★ 8. Address Bits of Bank-Select and Precharge



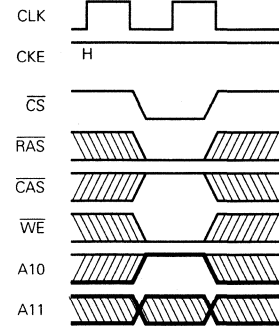
Precharge for Bank A



Precharge for Bank B



Precharge for All Banks



9. Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the read or write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically after the burst access.

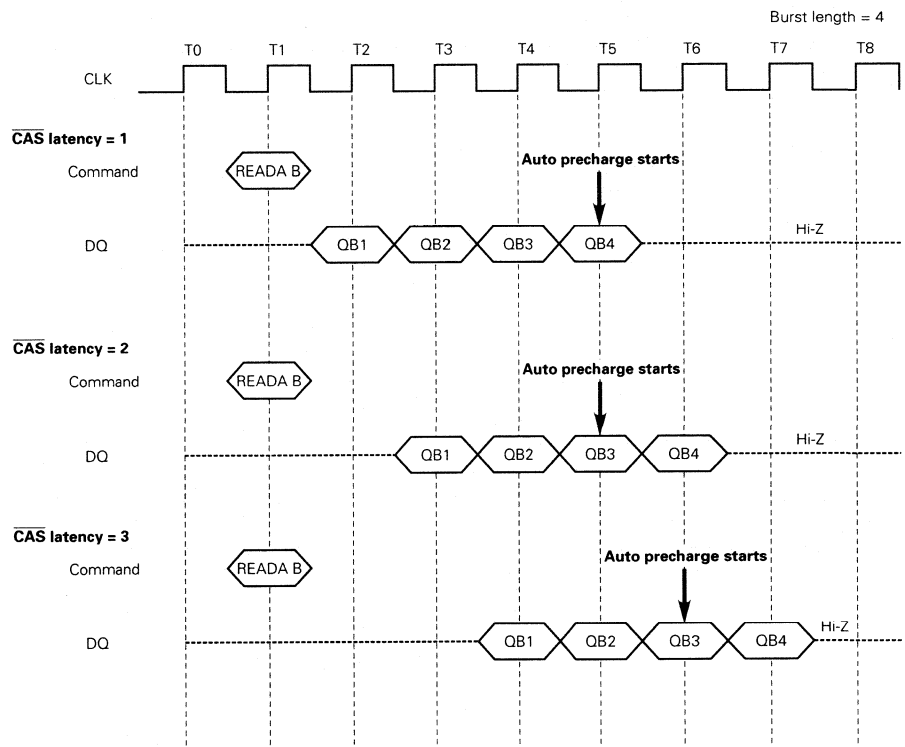
In write cycle, the t_{DAL} must be satisfied to assert the next activate command to the bank being precharged. It is not necessary to know when the precharge starts.

When using auto precharge in READ cycle, knowing when the precharge starts is important because the next activate command to the bank being precharged cannot be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be asserted after t_{RP} has been satisfied.

The clock that begins the auto precharge cycle is depend on both the $\overline{CAS}$ latency programmed into the mode register and whether READ or WRITE cycle.

9.1 Read with Auto Precharge

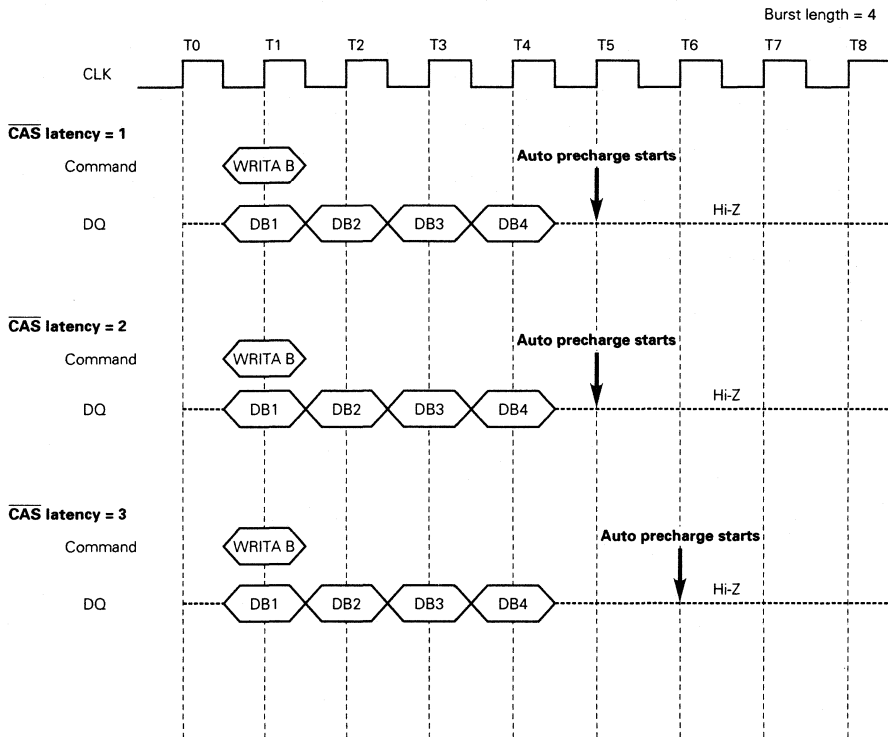
During READ cycle, the auto precharge begins on the clock that indicates the last data word output during the burst is valid ($\overline{CAS}$ latency of 1) or one clock earlier ($\overline{CAS}$ latency of 2 or 3).



Remark READA means Read with Auto precharge

9.2 Write with Auto Precharge

During WRITE cycle, the auto precharge begins one clock after the last data word input to the device ($\overline{\text{CAS}}$ latency of 1 or 2) or two clocks after ($\overline{\text{CAS}}$ latency of 3).



Remark WRITA means Write with Auto precharge

In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid.

In the table below, minus means clocks before the reference; plus means clocks after the reference.

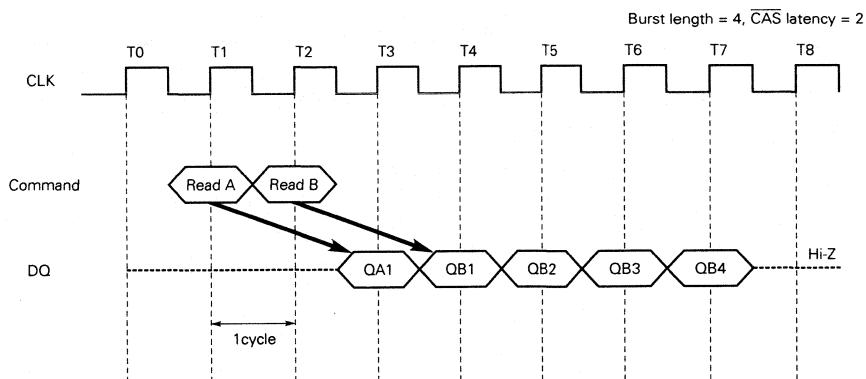
CAS latency	Read	Write
1	0	+1
2	-1	+1
3	-1	+2

10. Read/Write Command Interval

10.1 Read to Read Command Interval

During READ cycle, when new Read command is asserted, it will be effective after $\overline{\text{CAS}}$ latency, even if the previous READ operation does not completed. READ will be interrupted by another READ.

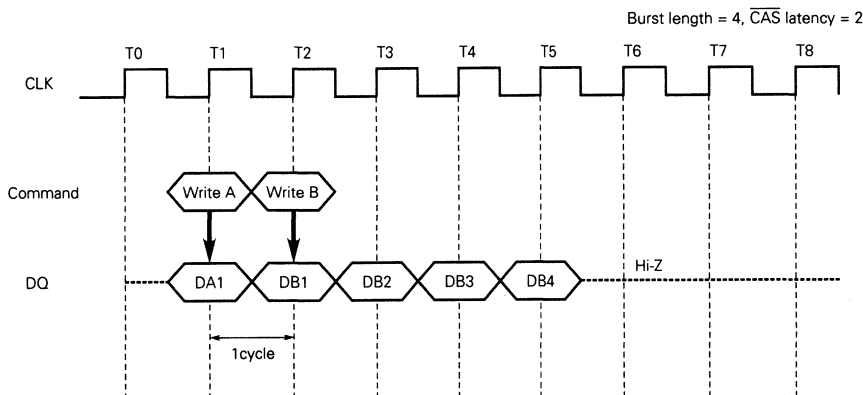
The interval between the commands is 1 cycle minimum. Each Read command can be asserted in every clock without any restriction.



10.2 Write to Write Command Interval

During WRITE cycle, when new Write command is asserted, the previous burst will terminate and the new burst will begin with a new Write command. WRITE will be interrupted by another WRITE.

The interval between the commands is minimum 1. Each Write command can be asserted in every clock without any restriction.

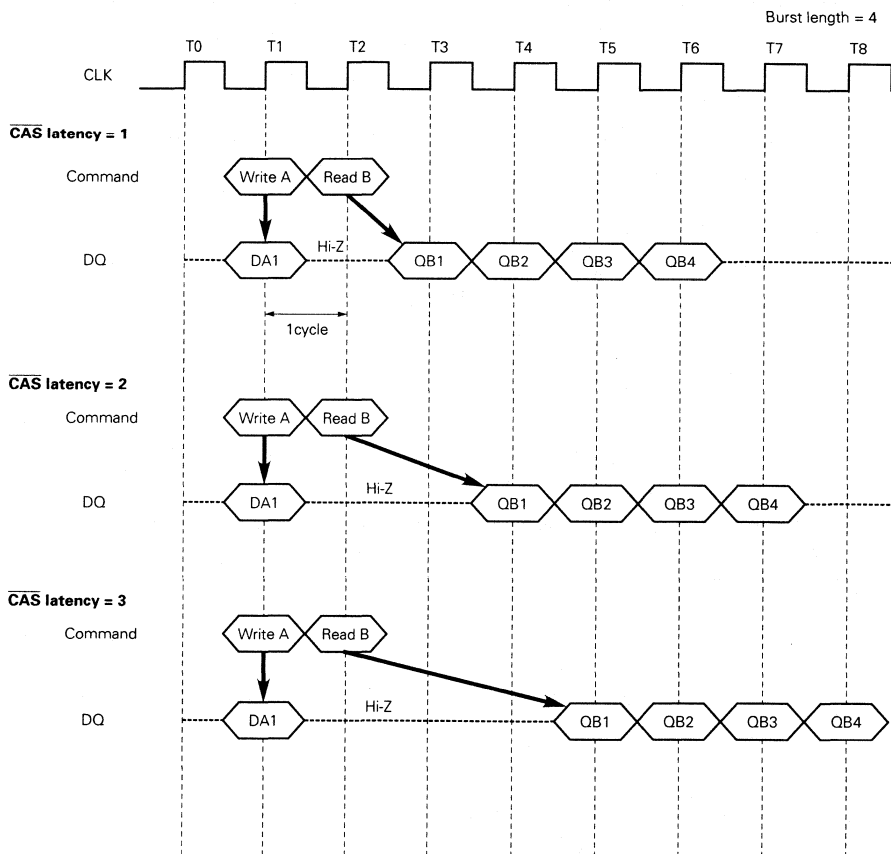


10.3 Write to Read Command Interval

Write command and Read command interval is also 1 cycle.

Only the write data before Read command will be written.

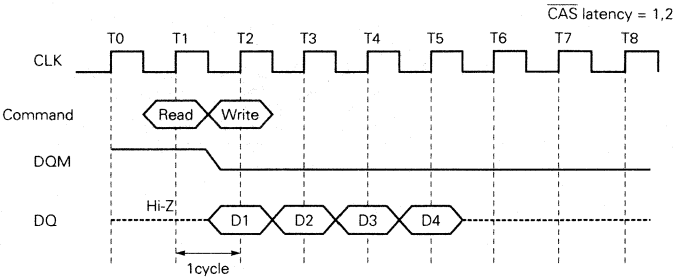
The data bus must be Hi-Z at least one cycle prior to the first Data Out.



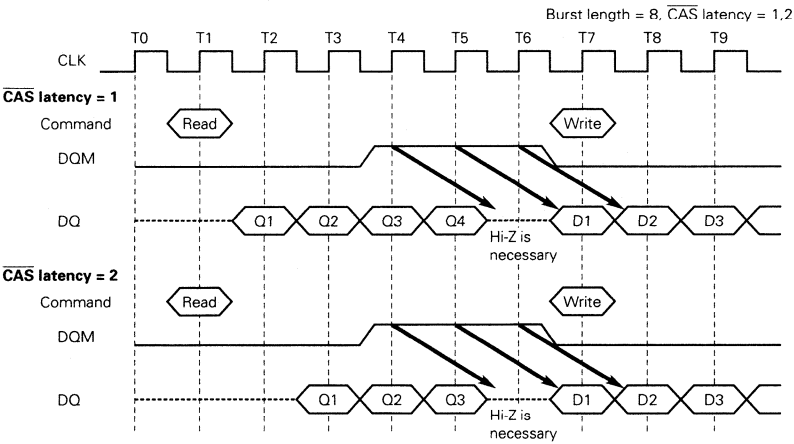
10.4 Read to Write Command Interval

During READ cycle, READ can be interrupted by WRITE. When the $\overline{\text{CAS}}$ latency is 3 and then the burst length is Full page, the burst read cannot be interrupted by WRITE (A Burst Stop command (BST) or a Precharge command can interrupt).

When the $\overline{\text{CAS}}$ latency is 1 or 2, the Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The data bus must be Hi-Z using DQM before WRITE.

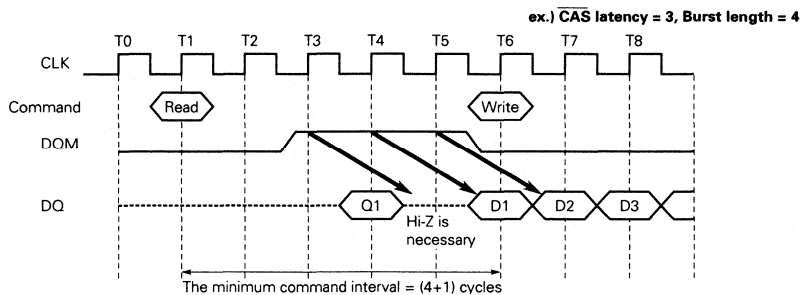


In case $\overline{\text{CAS}}$ latency is 1 or 2, READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.



In case $\overline{\text{CAS}}$ latency is 3 (burst length is not Full page), READ can be interrupted by WRITE.

The minimum command interval is [burst length + 1] cycles. DQM must be High at least 3 clocks prior to the Write command.

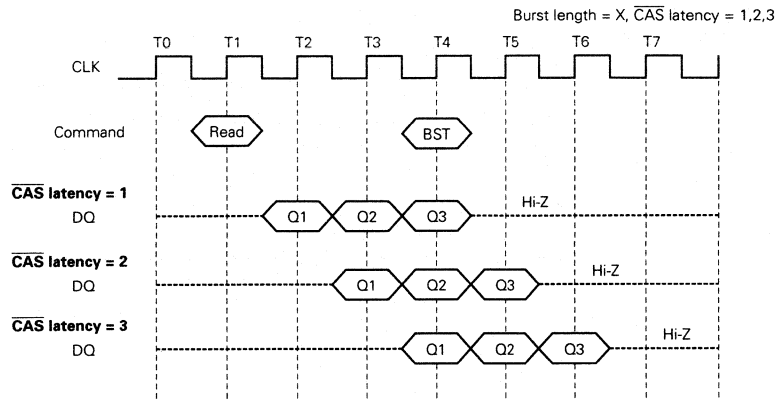


11. Burst Termination

There are two methods to terminate a burst operation other than using a read or a write command. One is the burst stop command and the other is the precharge command.

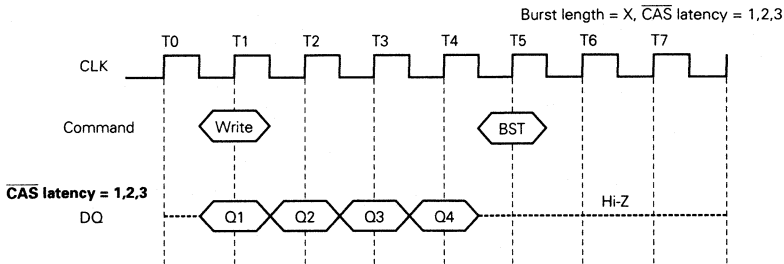
11.1 Burst Stop Command

During READ cycle, when the burst stop command is asserted, the burst read data are terminated and the data bus goes to high-impedance after the $\overline{\text{CAS}}$ latency from the burst stop command.



Remark BST: Burst stop command

During WRITE cycle, when the burst stop command is asserted, the burst read data are terminated and data bus goes to high-impedance at the same clock with the burst stop command.



Remark BST: Burst stop command

11.2 Precharge Termination

11.2.1 Precharge Termination in READ Cycle

During READ cycle, the burst read operation is terminated by a precharge command.

When the precharge command is asserted, the burst read operation is terminated and precharge starts.

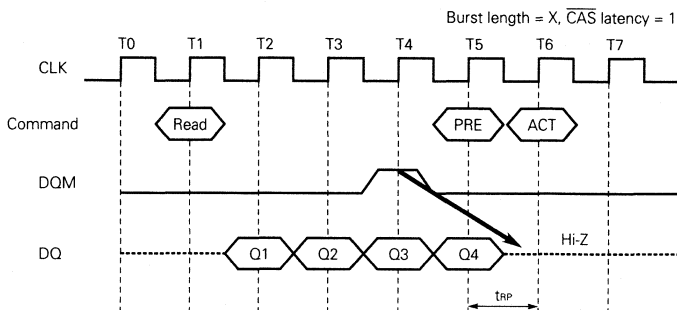
The same bank can be activated again after t_{RP} from the precharge command.

The DQM must be high to mask the invalid data.

When $\overline{CAS}$ latency is 1, the read data will remain valid until the precharge command is asserted.

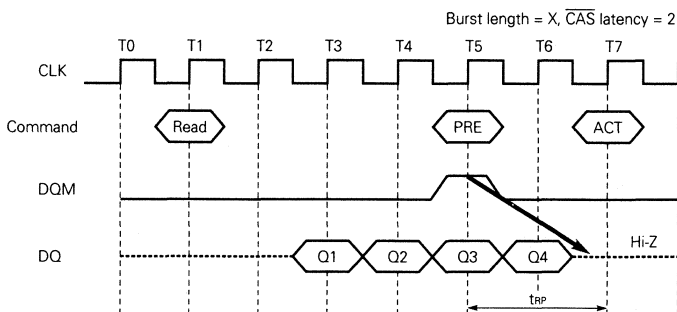
Invalid data may appear one clock after valid data out.

The DQM may be high to mask the invalid data.



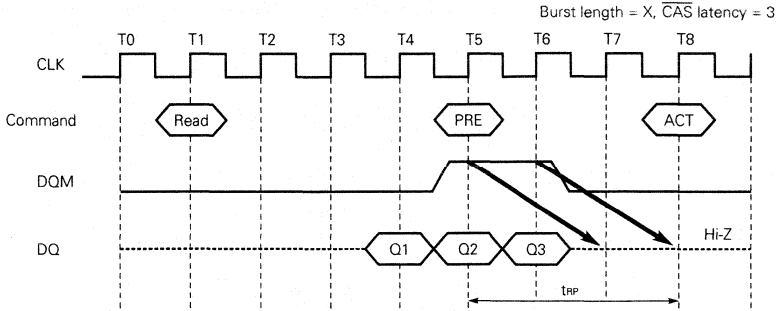
When $\overline{CAS}$ latency is 2, the read data will remain valid until one clock after the precharge command. Invalid data may appear one clock after valid data out.

The DQM may be high to mask the invalid data.



When $\overline{\text{CAS}}$ latency is 3, the read data will remain valid until one clock after the precharge command. Invalid data may appear one and two clocks after valid data out.

The DQM may be high to mask the invalid data.



11.2.2 Precharge Termination in WRITE Cycle

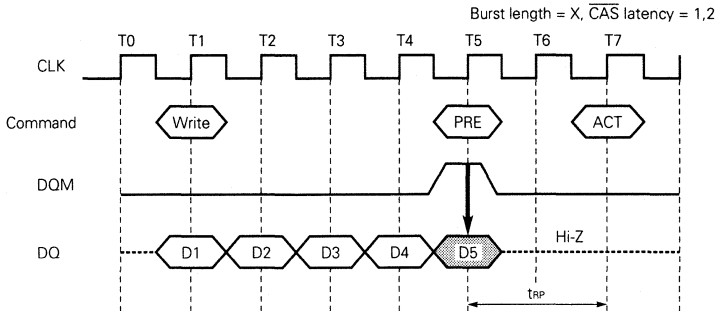
During WRITE cycle, the burst write operation is terminated by a precharge command.

When the precharge command is asserted, the burst write operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command.

The DQM must be high to mask invalid data in.

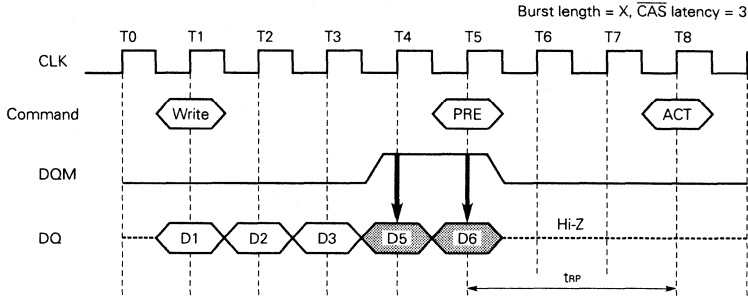
When $\overline{\text{CAS}}$ latency is 1 or 2, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



When $\overline{\text{CAS}}$ latency is 3, the write data written more than one clock prior to the precharge command will be correctly stored.

However, invalid data may be written at one clock before and the same clock as the precharge command.

To prevent this from happening, DQM must be high from one clock prior to the precharge command until the precharge command. This will mask the invalid data.



12. Electrical Specifications (Preliminary)

- All voltage are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute **Power on sequence and Auto Refresh** before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V _T		-1.0 to +4.6	V
Voltage on input pin relative to GND	V _{CC} , V _{CCQ}		-1.0 to +4.6	V
Short circuit output current	I _O		50	mA
Power dissipation	P _D		1	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		3.0	3.3	3.6	V
High level input voltage	V _{IH}		2.0		4.6	V
Low level input voltage	V _{IL}		-0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (T_A=25°C, f=1MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 to A11	2		4	pF
	C _{I2}	CLK, CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQM, UDQM, LDQM	2		4	pF
Data input/output capacitance	C _{I/O}	DQ0 to DQ15	2		5	pF

DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

(1/2)

Parameter	Symbol	Test condition	CAS latency	Grade	Maximum x4 x8 x16			Unit	Notes
Operating current	I _{CC1}	Burst length=1 t _{RC} ≥ t _{RC} (MIN.) I _O =0mA	CL=1	-10	70	75	80	mA	1
				-12	65	70	75		
				-13	60	65	70		
				-15	60	65	70		
			CL=2	-10	75	80	85	mA	1
				-12	70	75	80		
				-13	65	70	75		
				-15	65	70	75		
			CL=3	-10	80	85	90	mA	1
				-12	75	80	85		
				-13	70	75	80		
				-15	65	70	75		
Precharge standby current in Power down mode	I _{CC2P}	CKE ≤ V _{IL} (MAX.) t _{CK} =15ns			3	3	3	mA	
	I _{CC2PS}	CKE ≤ V _{IL} (MAX.) t _{CK} =∞			2	2	2		
Precharge standby current in Non power down mode	I _{CC2N}	CKE ≥ V _{IH} (MIN.) t _{CK} =15ns CS ≥ V _{IH} (MIN.) Input signals are changed one time during 30ns.			20	20	20	mA	
	I _{CC2NS}	CKE ≥ V _{IH} (MIN.) t _{CK} =∞ Input signals are stable.			6	6	6		
Active standby current in Power down mode	I _{CC3P}	CKE ≤ V _{IL} (MAX.) t _{CK} =15ns			3	3	3	mA	
	I _{CC3PS}	CKE ≤ V _{IL} (MAX.) t _{CK} =∞			2	2	2		
Active standby current in Non power down mode	I _{CC3N}	CKE ≥ V _{IH} (MIN.) t _{CK} =15ns CS ≥ V _{IH} (MIN.) Input signals are changed one time during 30 ns.			25	25	25	mA	
	I _{CC3NS}	CKE ≥ V _{IH} (MIN.) t _{CK} =∞ Input signals are stable.			10	10	10		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK} (MIN.) I _O =0mA	CL=1	-10	70	75	90	mA	2
				-12	60	65	80		
				-13	55	60	75		
				-15	55	60	75		
			CL=2	-10	110	120	150		
				-12	90	100	125		
				-13	85	95	115		
				-15	85	95	115		
			CL=3	-10	150	165	210		
				-12	130	145	180		
				-13	120	130	160		
				-15	100	110	140		

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK}(MIN.).

2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK}(MIN.).

DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

(2/2)

Parameter	Symbol	Test condition	CAS latency	Grade	Maximum			Unit	Note
					x4	x8	x16		
Refresh current	I _{CCS}	t _{RC} ≥ t _{RC} (MIN.)	CL=1	-10	90	90	90	mA	1
				-12	80	80	80		
				-13	75	75	75		
				-15	75	75	75		
			CL=2	-10	95	95	95		
				-12	85	85	85		
				-13	80	80	80		
				-15	80	80	80		
			CL=3	-10	100	100	100		
				-12	90	90	90		
				-13	85	85	85		
				-15	80	80	80		
Self refresh Current	I _{CCS}	CKE ≤ 0.2V		**	2	2	2	mA	
				**L	100	100	100		

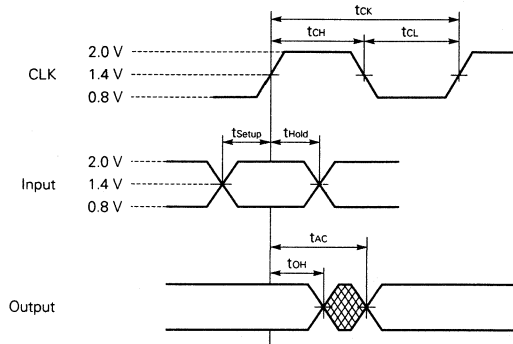
Note 1. I_{CCS} is measured on condition that addresses are changed only one time during t_{CK}(MIN.).

DC Characteristics 2 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I _{I(L)}	V _I =0 to 3.6V, all other pins not under test =0V	-1.0		+1.0	μA
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O =0 to 3.6V	-1.0		+1.0	μA
High level output voltage	V _{OH}	I _O =-2mA	2.4			V
Low level output voltage	V _{OL}	I _O =+2mA			0.4	V

AC Characteristics (Recommended Operating Conditions unless otherwise noted)**Test Conditions**

- AC measurements assume $t_r=1\text{ns}$.
- Reference level for measuring timing of input signals is 1.4V. Transition times are measured between V_{IH} and V_{IL} .
- If t_r is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH}(\text{MIN.})$ and $V_{IL}(\text{MAX.})$.
- An access time is measured at 1.4V.

**Synchronous Characteristics**

(1/2)

Parameter		Symbol	-10		-12		-13		-15		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
★ Clock cycle time	CAS latency=3	t_{CK3}	10	(100MHz)	12	(83MHz)	13	(77MHz)	15	(66MHz)	ns	
	CAS latency=2	t_{CK2}	15	(66MHz)	18	(55MHz)	19.5	(50MHz)	19.5	(50MHz)	ns	
	CAS latency=1	t_{CK1}	30	(33MHz)	36	(28MHz)	39	(25MHz)	39	(25MHz)	ns	
Access time from CLK	CAS latency=3	t_{AC3}		9		11		12		14	ns	1
	CAS latency=2	t_{AC2}		12		15		16.5		16.5	ns	2
	CAS latency=1	t_{AC1}		27		33		36		36	ns	2
CLK high level width		t_{CH}	3.5		4		5		5		ns	
CLK low level width		t_{CL}	3.5		4		5		5		ns	
Data-out hold time		t_{OH}	4		4		4		4		ns	
Data-out low-impedance time		t_{LZ}	0		0		0		0		ns	
Data-out high-impedance time		t_{HZ}		10		10		10		10	ns	
Data-in setup time		t_{DS}	3		3.5		3.5		3.5		ns	
Data-in hold time		t_{DH}	1		1.5		1.5		1.5		ns	
Address setup time		t_{AS}	3		3.5		3.5		3.5		ns	
Address hold time		t_{AH}	1		1.5		1.5		1.5		ns	
CKE setup time		t_{CKS}	3		3.5		3.5		3.5		ns	
CKE hold time		t_{CKH}	1		1.5		1.5		1.5		ns	
★ CKE setup time (Power down exit)		t_{CKSP}	3		3.5		3.5		3.5		ns	

Notes 1. Loading capacitance is 50 pF.

2. Loading capacitance is 80 pF.

Synchronous Characteristics

(2/2)

Parameter	Symbol	-10		-12		-13		-15		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Command (CS, RAS, CAS, WE, DQM) setup time	t _{CMS}	3		3.5		3.5		3.5		ns	
Command (CS, RAS, CAS, WE, DQM) hold time	t _{CMH}	1		1.5		1.5		1.5		ns	

Asynchronous Characteristics

Parameter	Symbol	-10		-12		-13		-15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT Command period	t _{RC}	100		120		130		130		ns	
ACT to PRE Command period	t _{RAS}	70	120,000	84	120,000	91	120,000	91	120,000	ns	
PRE to ACT Command period	t _{RP}	30		36		39		39		ns	
Delay time ACT to READ/ WRITE Command	t _{RCD}	30		36		39		39		ns	
ACT(0) to ACT(1) Command period	t _{RRD}	30		36		39		39		ns	
Data-in to PRE Command period	$\overline{\text{CAS}}$ latency=3	t _{DPL3}	1CLK+10		1CLK+12		1CLK+13		1CLK+15	ns	
	$\overline{\text{CAS}}$ latency=2	t _{DPL2}	15		18		19.5		19.5	ns	
	$\overline{\text{CAS}}$ latency=1	t _{DPL1}	15		18		19.5		19.5	ns	
Data-in to ACT (REF) Command period (Auto precharge)	$\overline{\text{CAS}}$ latency=3	t _{DAL3}	2CLK+30		2CLK+36		2CLK+39		2CLK+45	ns	
	$\overline{\text{CAS}}$ latency=2	t _{DAL2}	1CLK+30		1CLK+36		1CLK+39		1CLK+39	ns	
	$\overline{\text{CAS}}$ latency=1	t _{DAL1}	1CLK+30		1CLK+36		1CLK+39		1CLK+39	ns	
Self refresh exit time	t _{SREX}	20		24		26		26		ns	
Transition time	t _T	1	30	1	30	1	30	1	30	ns	
Refresh time	t _{REF}		32		32		32		32	ms	

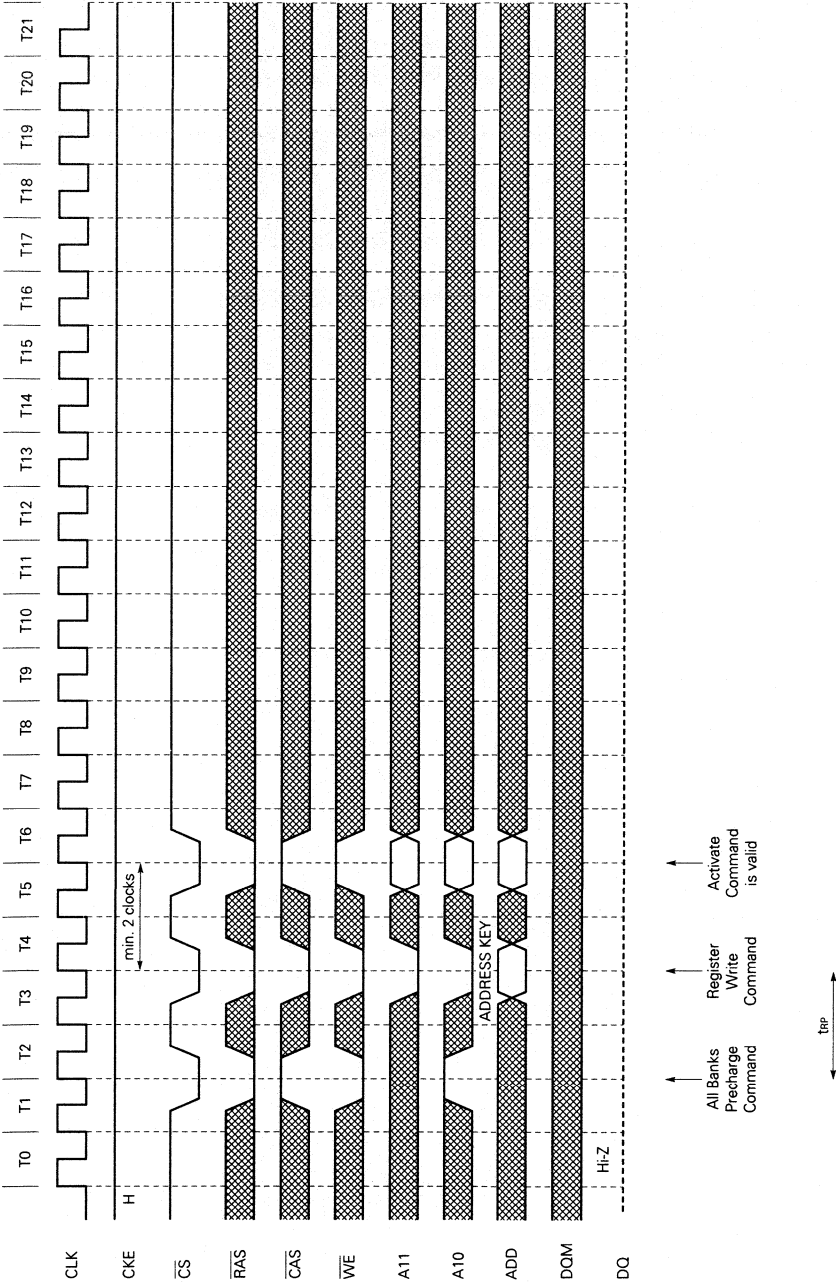
12.3 Relationship between Frequency and Latency

★

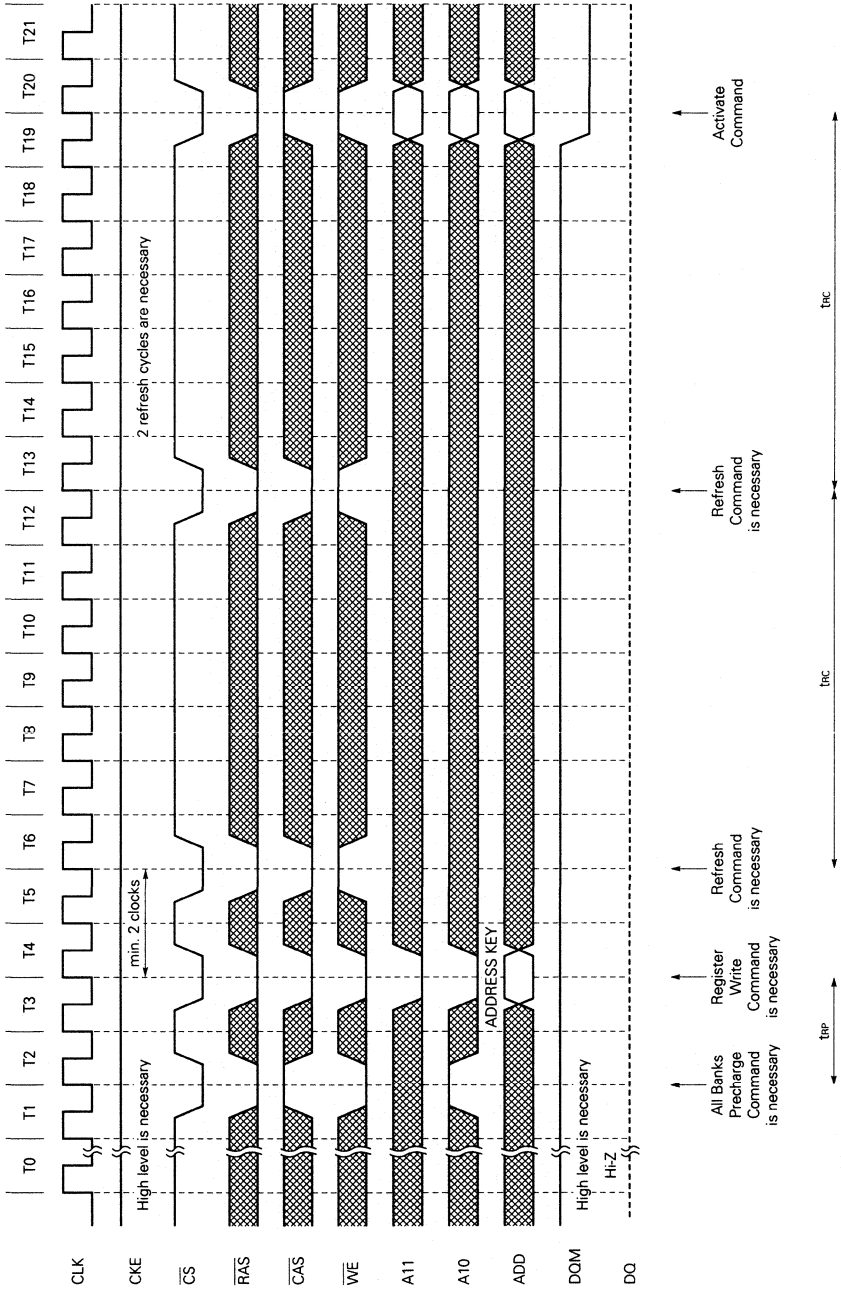
Speed version	-10			-12			-13			-15		
Clock cycle time [ns]	10	15	30	12	18	36	13	19.5	39	15	19.5	39
Frequency [MHz]	100	66	33	83	55	28	77	50	25	66	50	25
CAS latency	3	2	1	3	2	1	3	2	1	3	2	1
[trcd]	3	2	1	3	2	1	3	2	1	3	2	1
RAS latency (CAS latency + [trcd])	6	4	2	6	4	2	6	4	2	6	4	2
[trc]	10	7	4	10	7	4	10	7	4	10	7	4
[trac]	7	5	3	7	5	3	7	5	3	7	5	3
[trrd]	3	2	1	3	2	1	3	2	1	3	2	1
[trp]	3	2	1	3	2	1	3	2	1	3	2	1
[tdpl]	2	1	1	2	1	1	2	1	1	2	1	1
[tdal]	5	3	2	5	3	2	5	3	2	5	3	2
[tsrex]	2	2	1	2	2	1	2	2	1	2	2	1

12.4 Mode Register Write

Burst length = 4 CAS latency = 2

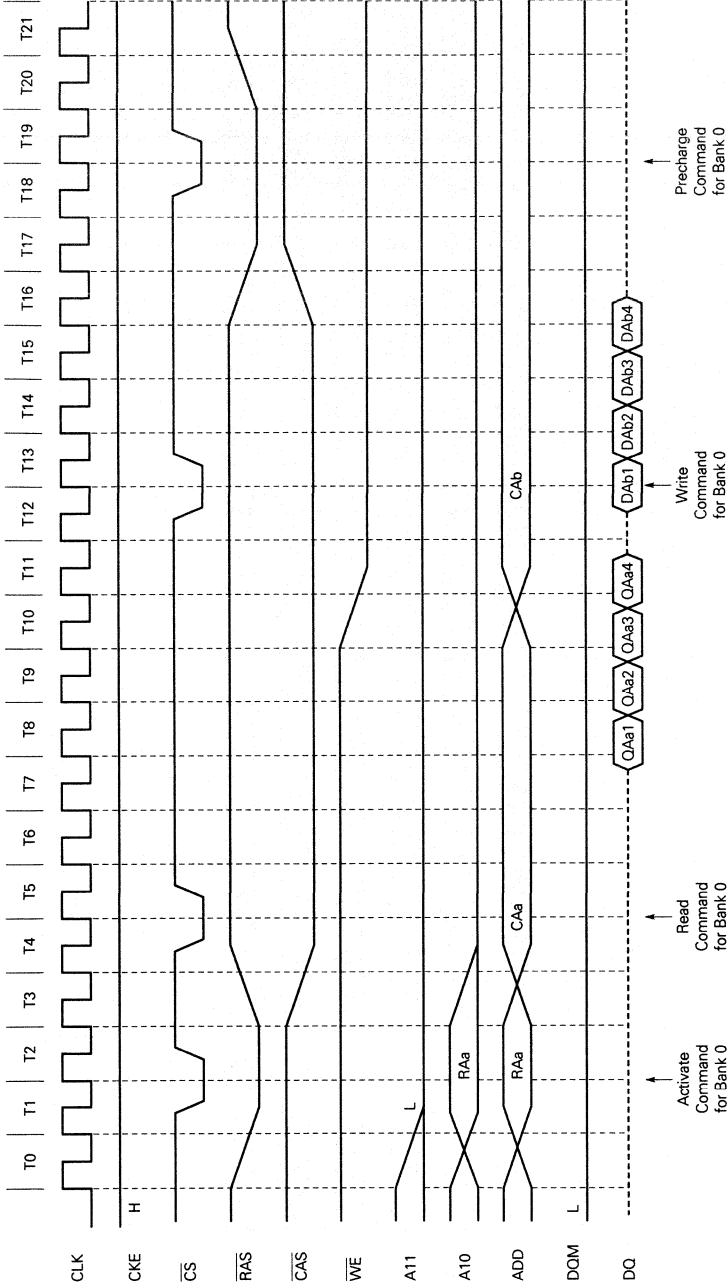


12.5 Power on Sequence and Auto Refresh

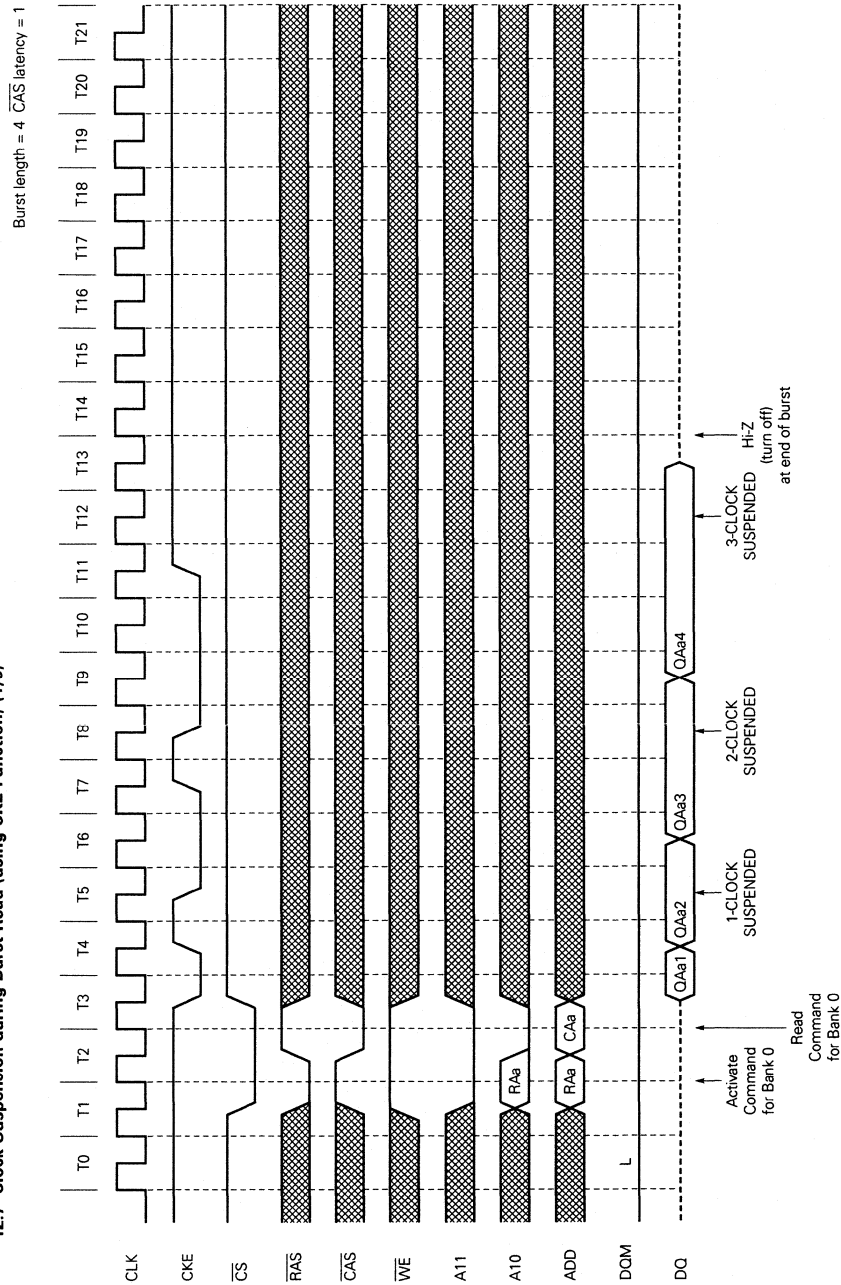


12.6 $\overline{\text{CS}}$ Function (Only $\overline{\text{CS}}$ signal needs to be asserted at minimum rate)

at 100MHz Burst length = 4 $\overline{\text{CAS}}$ latency = 3

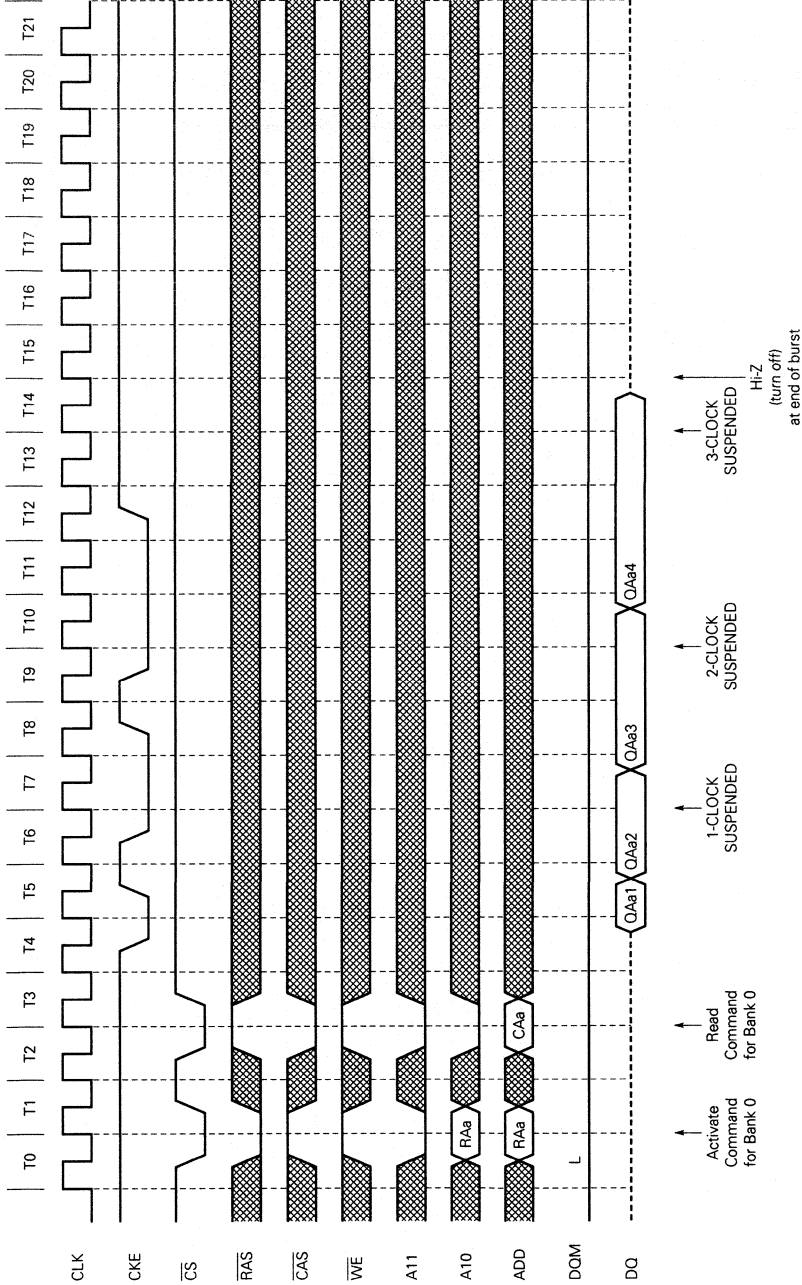


12.7 Clock Suspension during Burst Read (using CKE Function) (1/3)



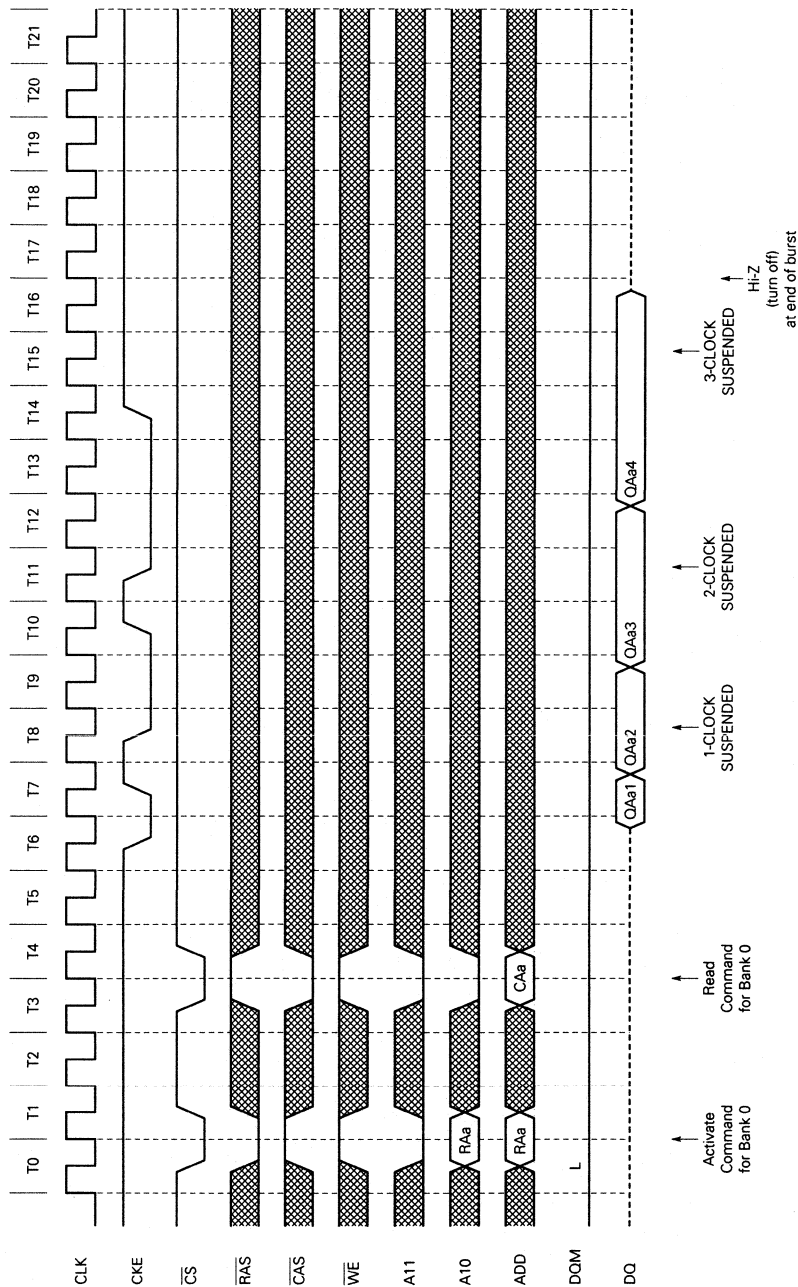
Clock Suspension during Burst Read (using CKE Function) (2/3)

Burst length = 4 CAS latency = 2



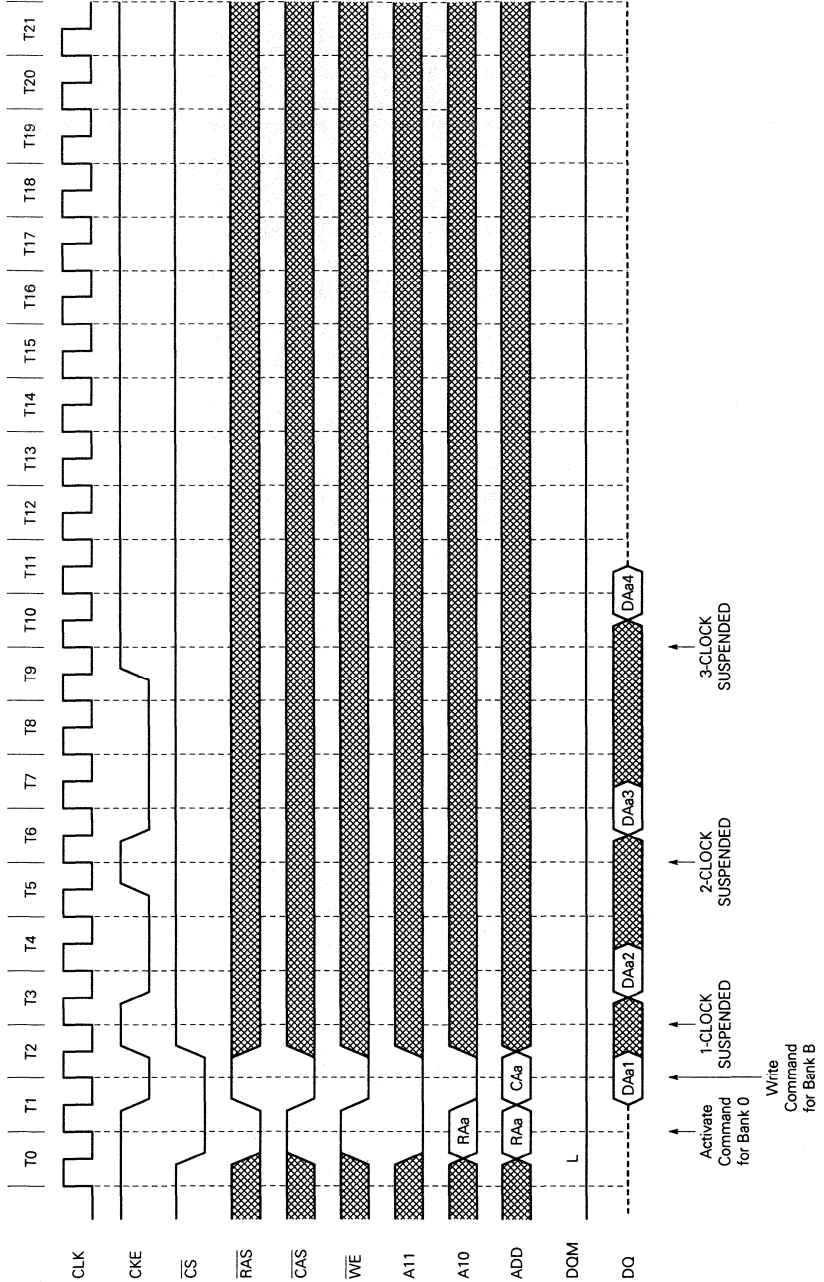
Clock Suspension during Burst Read (using CKE Function) (3/3)

Burst length = 4 CAS latency = 3



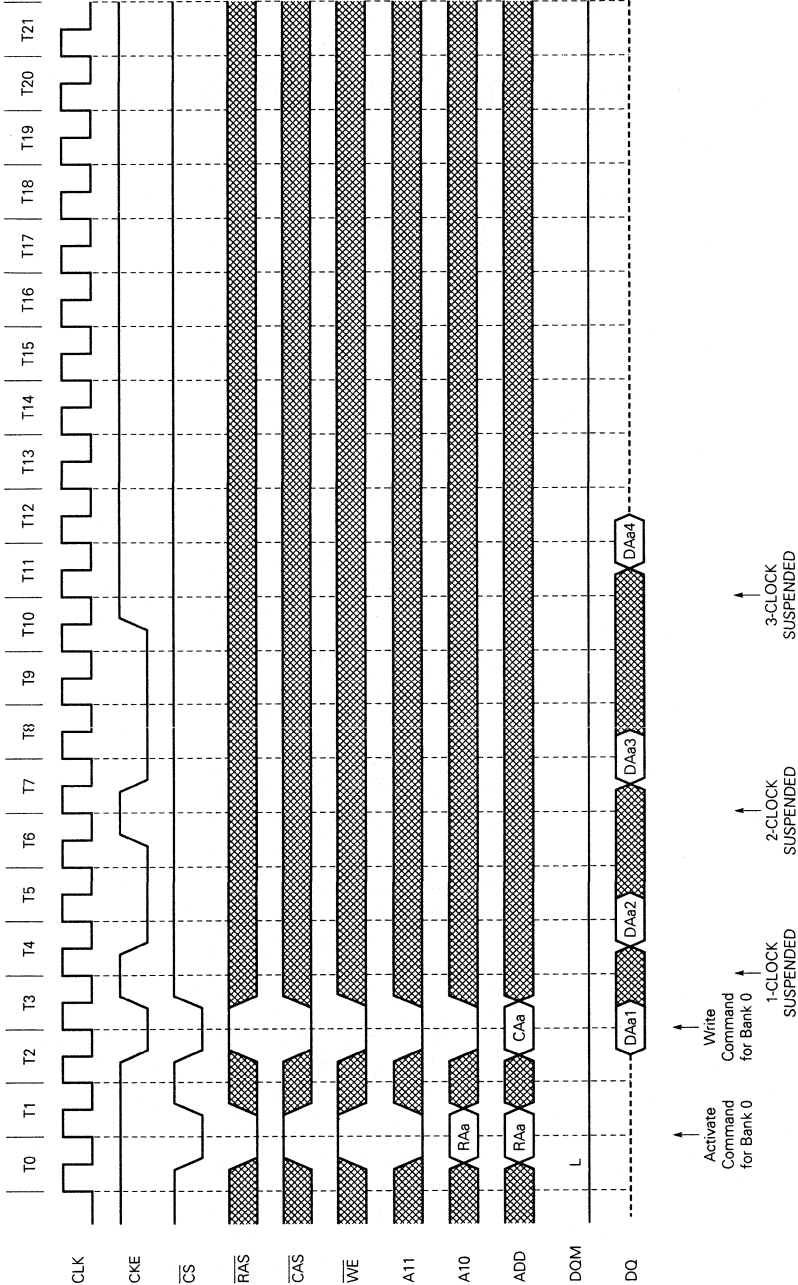
12.8 Clock Suspension during Burst Write (using CKE Function) (1/3)

Burst length = 4 CAS latency = 1

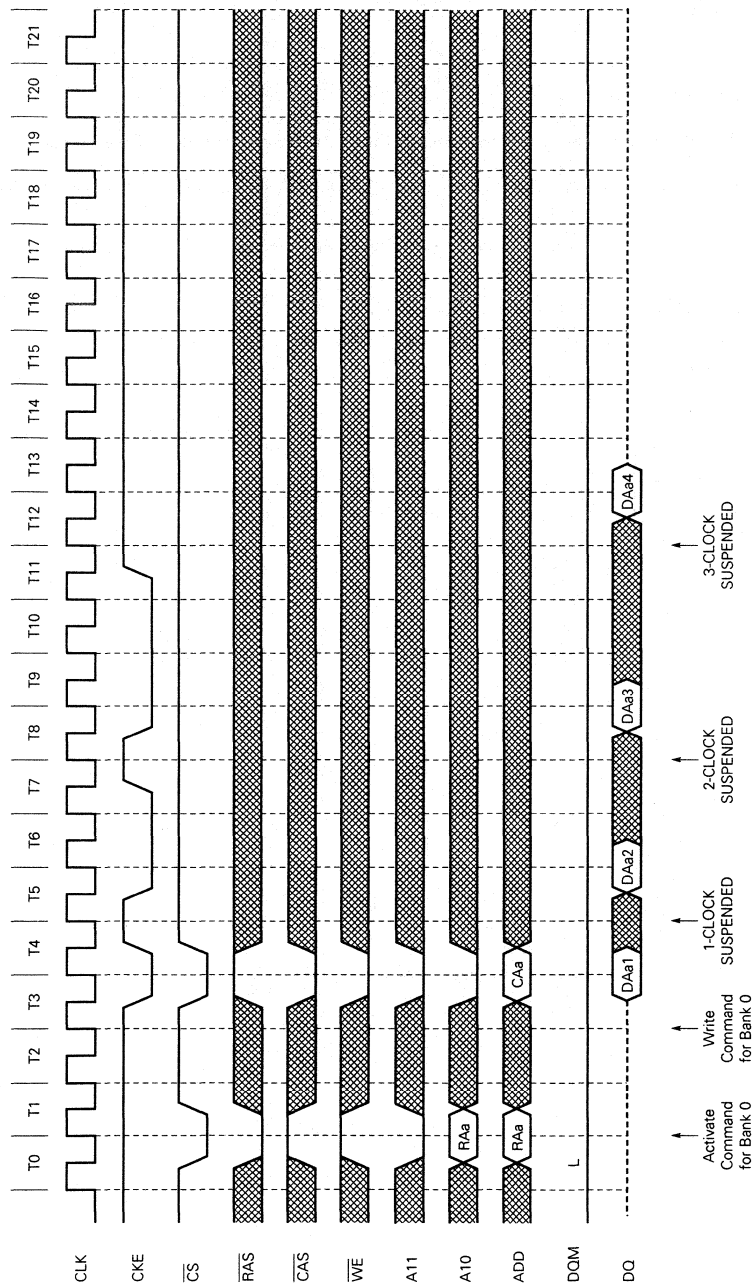


Clock Suspension during Burst Write (using CKE Function) (2/3)

Burst length = 4 CAS latency = 2

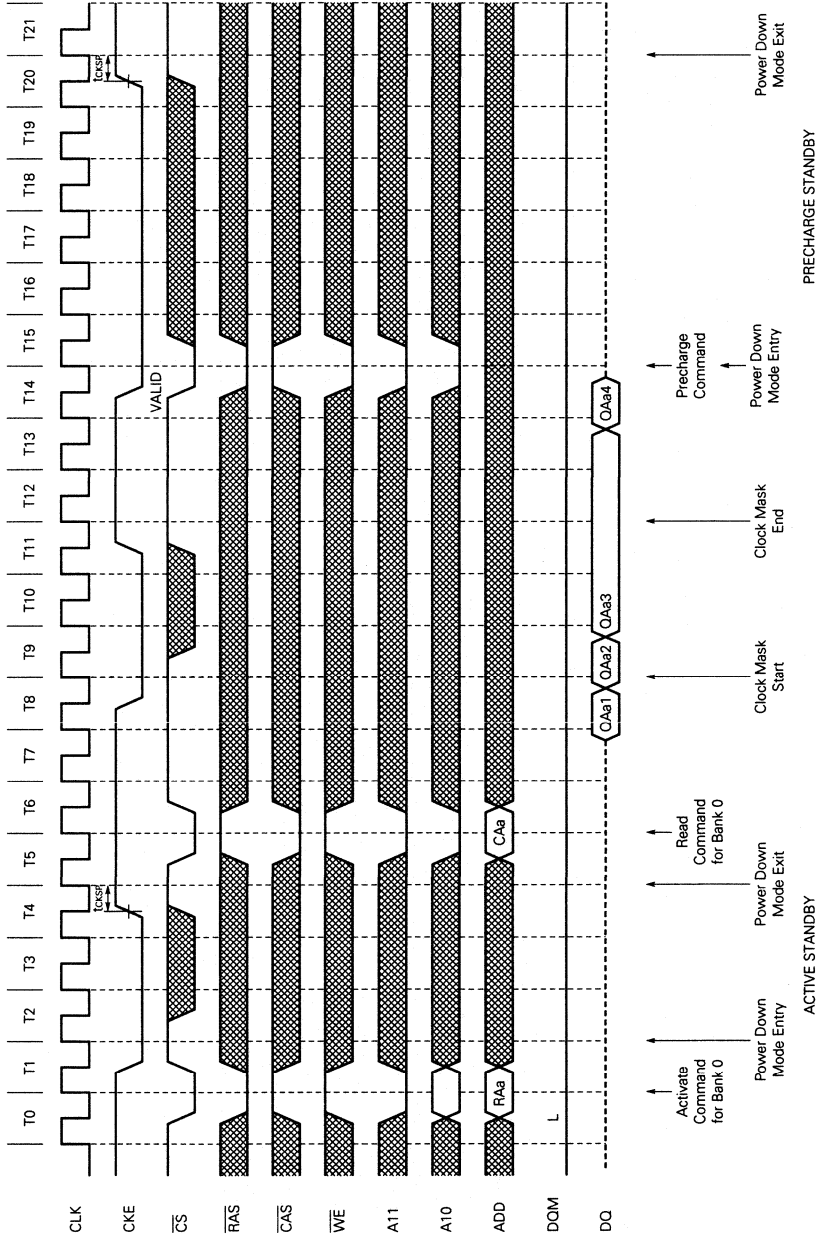


Burst length = 4 CAS latency = 3

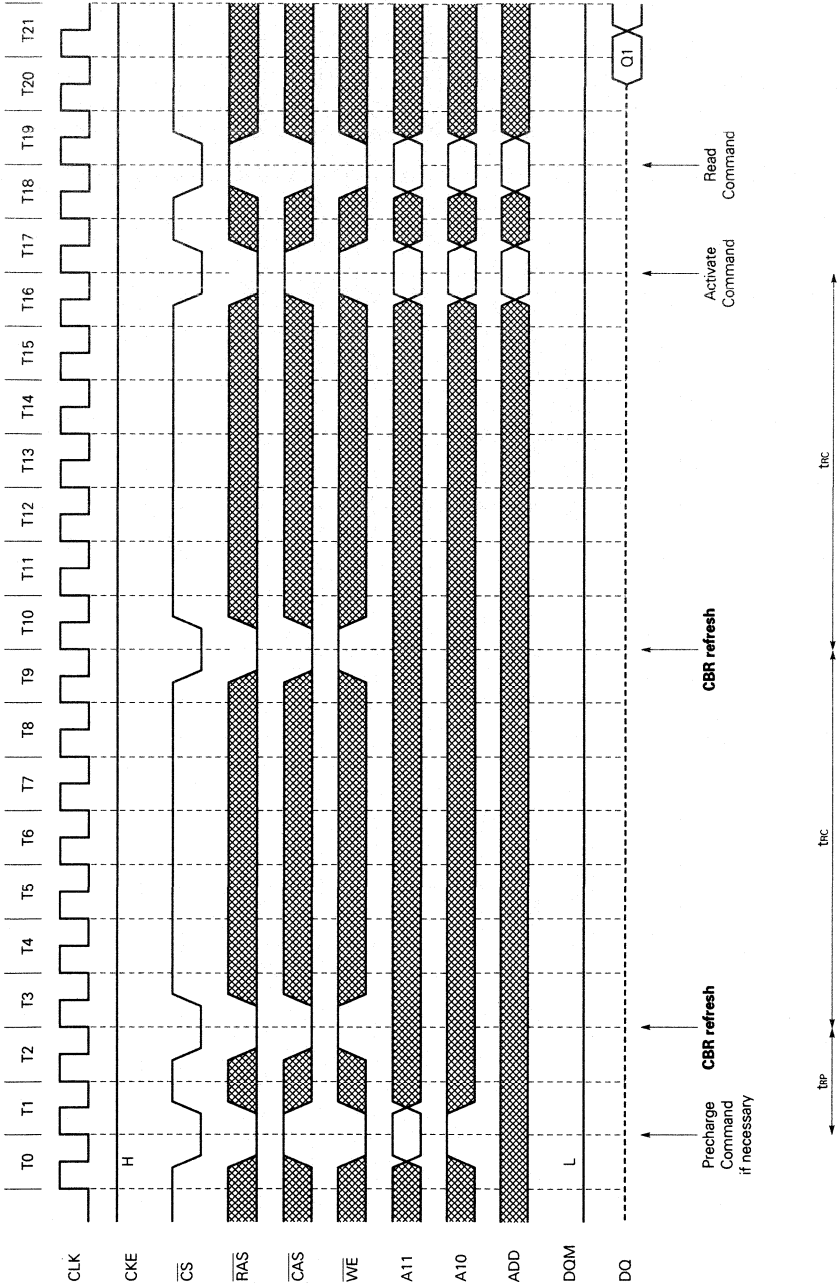


★ 12.9 Power Down Mode and Clock Mask

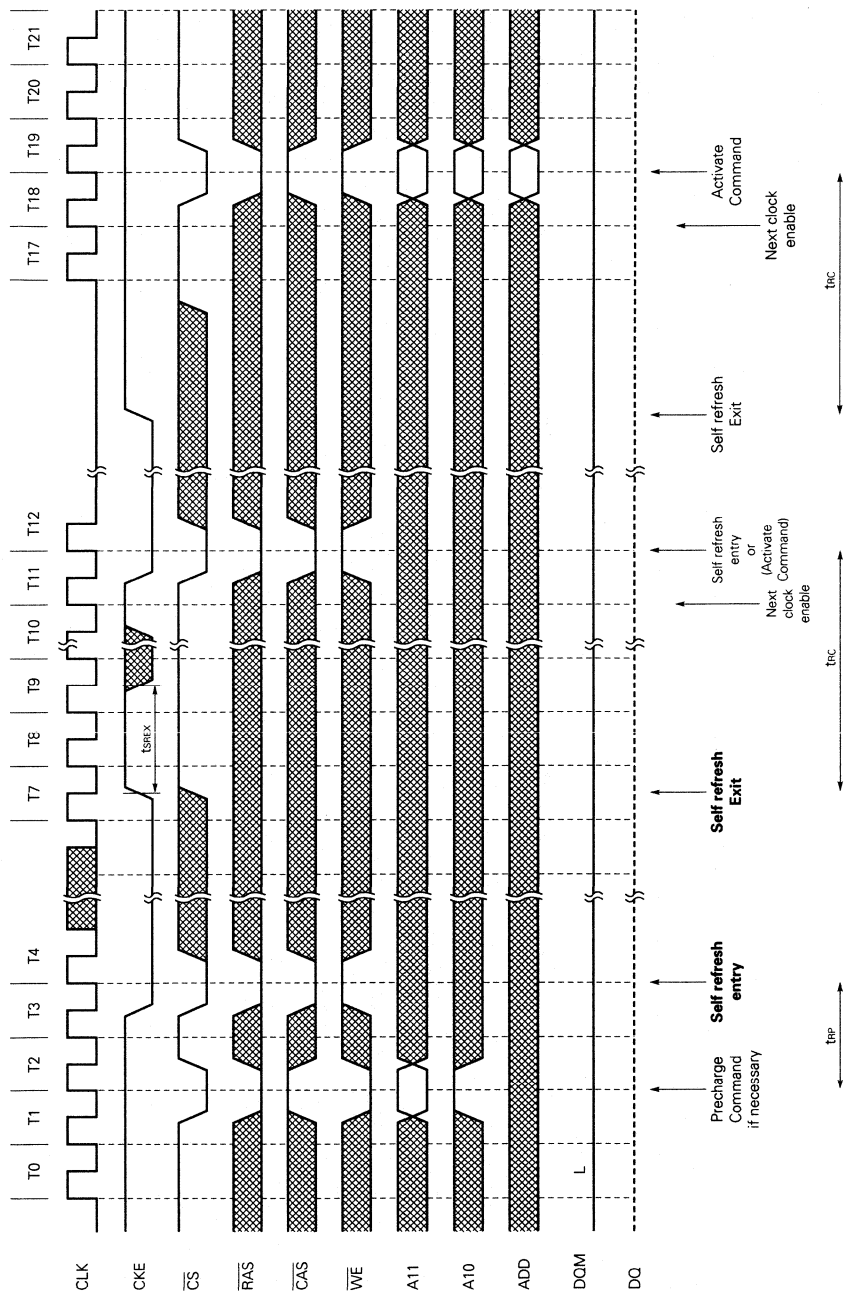
Burst length = 4 CAS latency = 2



12.10 CBR Refresh

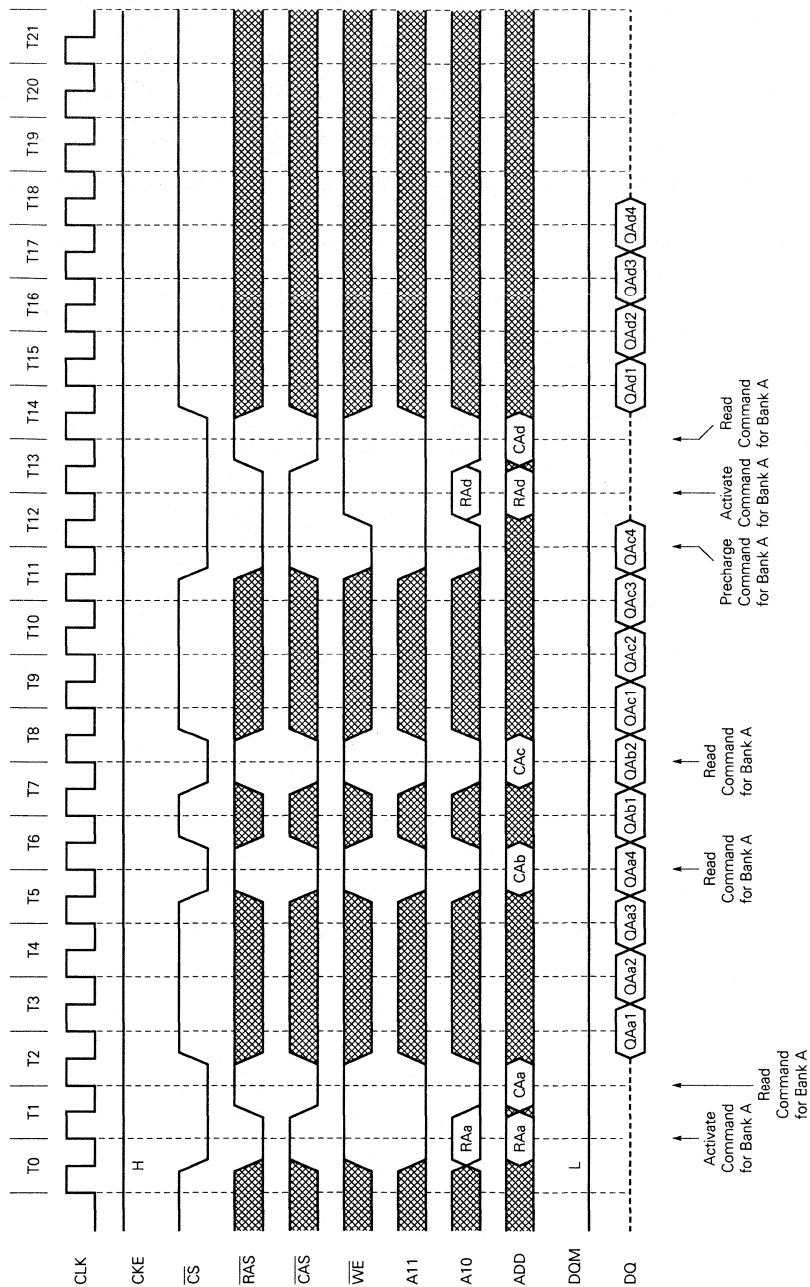


12.11 Self Refresh (entry and exit)



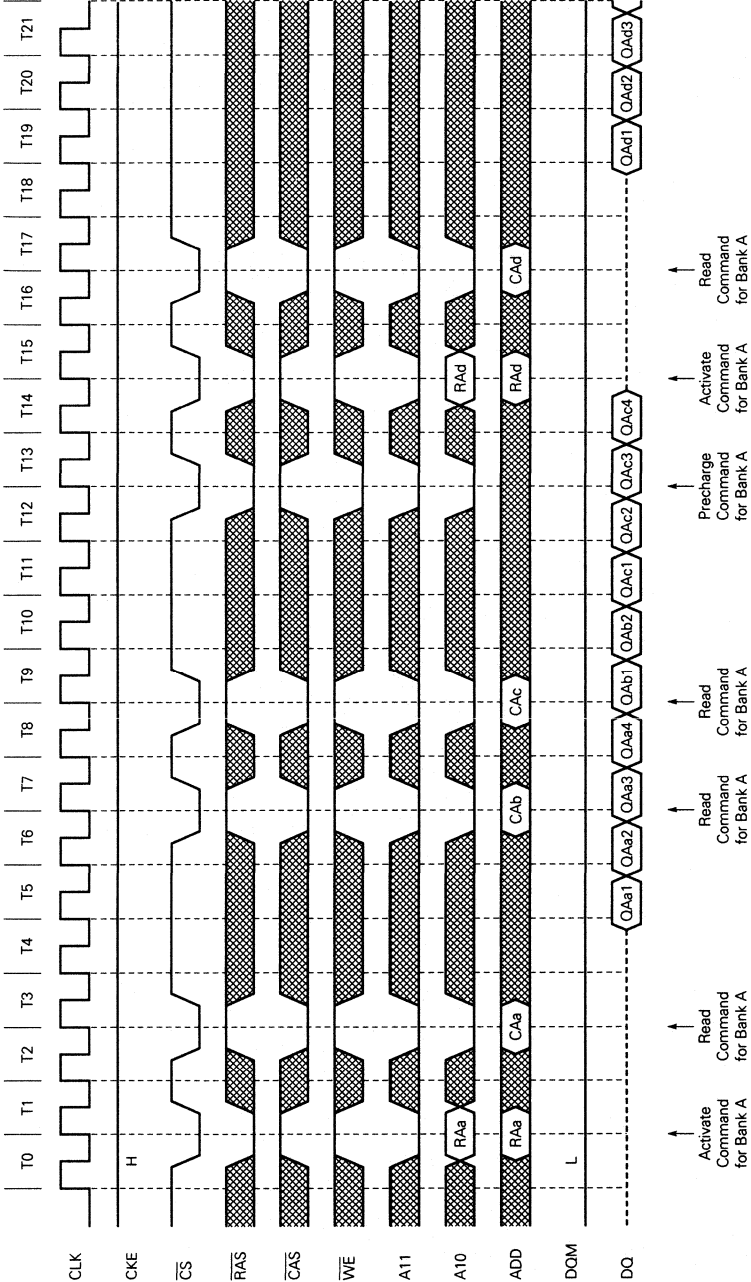
12.12 Random Column Read (Page with same bank) (1/3)

Burst length = 4 CAS latency = 1



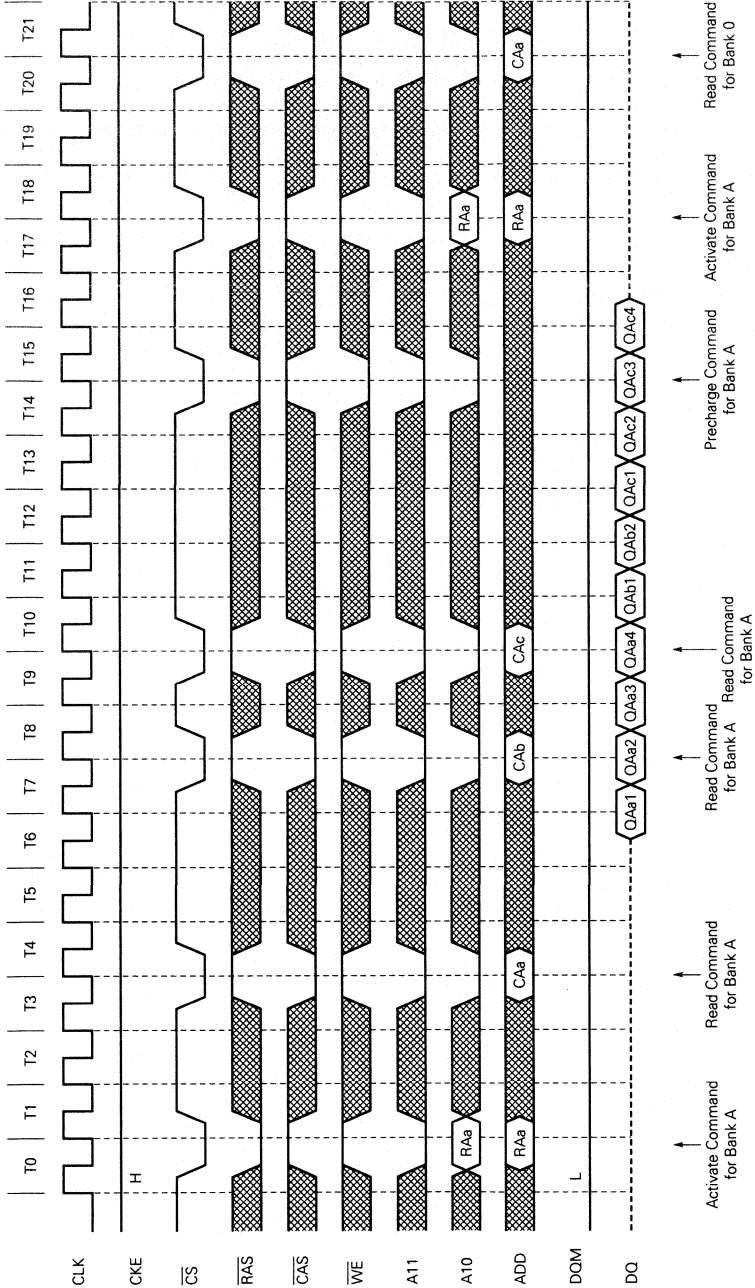
Random Column Read (Page with same bank) (2/3)

Burst length = 4 CAS latency = 2



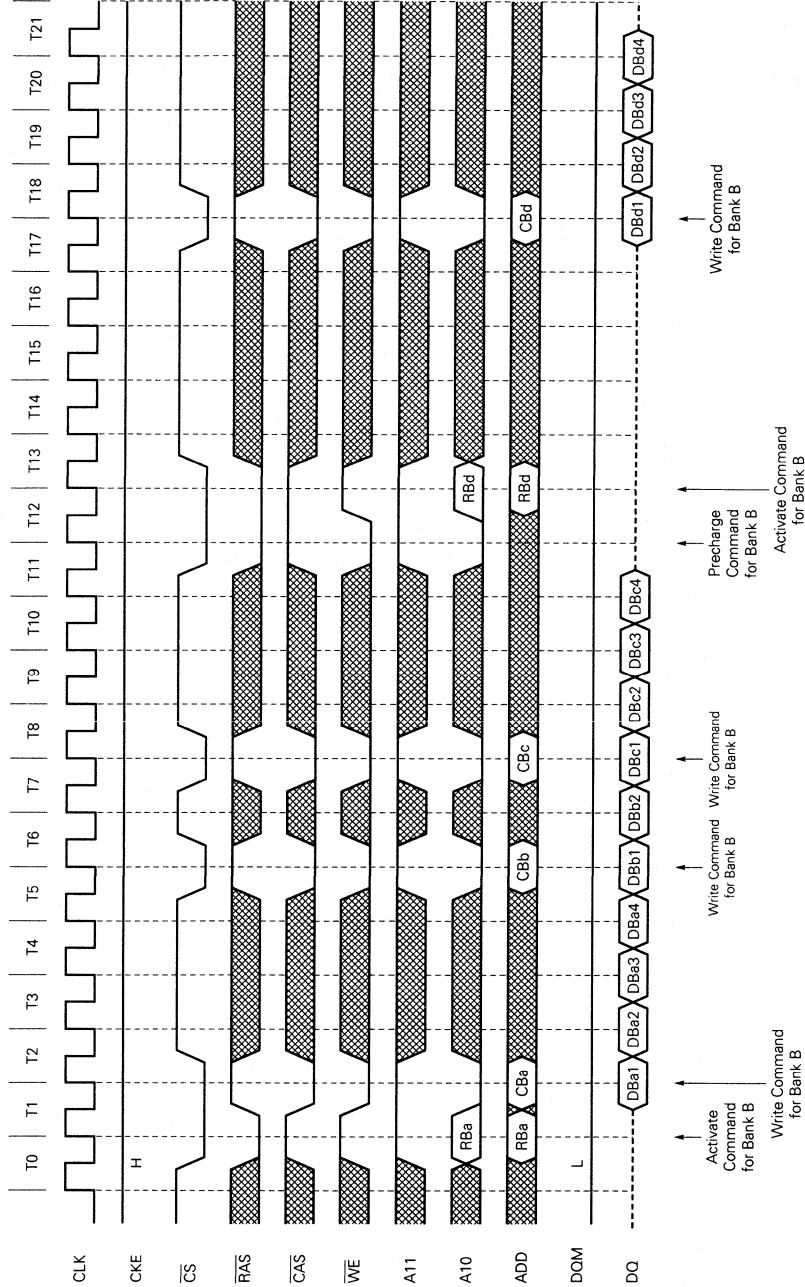
Random Column Read (Page with same bank) (3/3)

Burst length = 4 CAS latency = 3



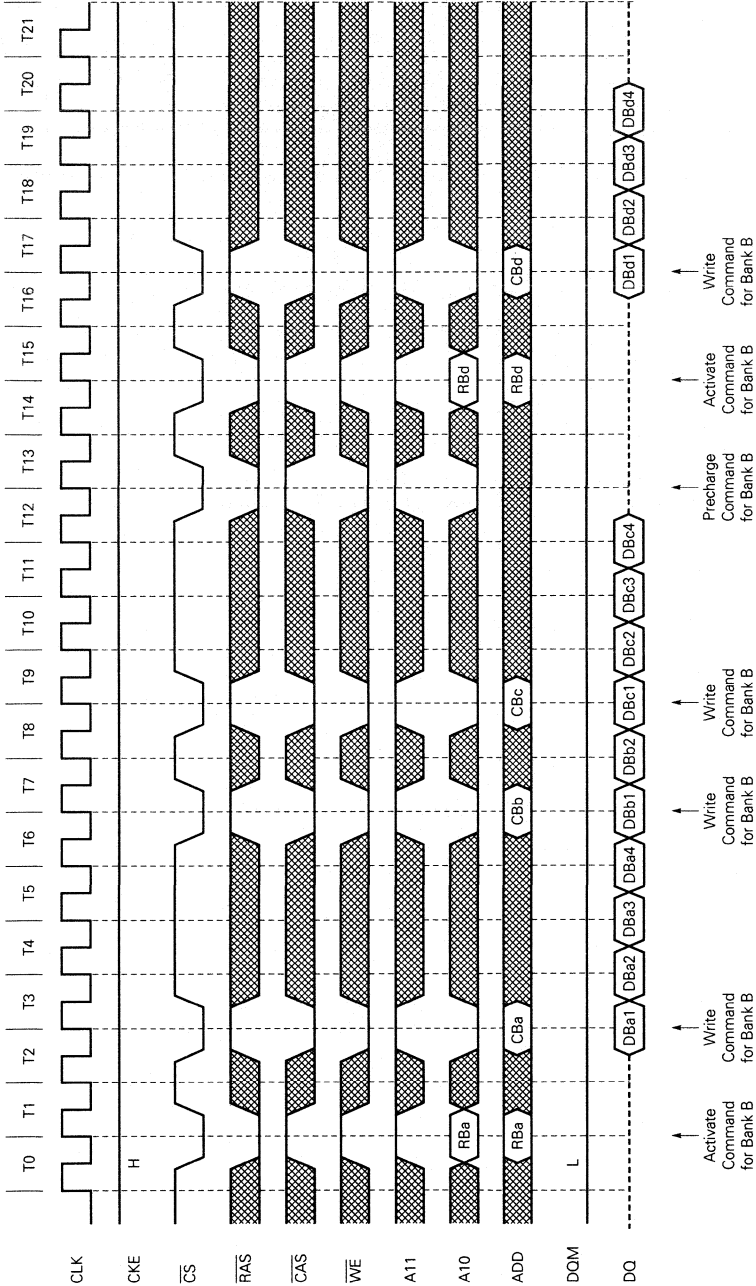
12.13 Random Column Write (Page with same bank) (1/3)

Burst length = 4 CAS latency = 1



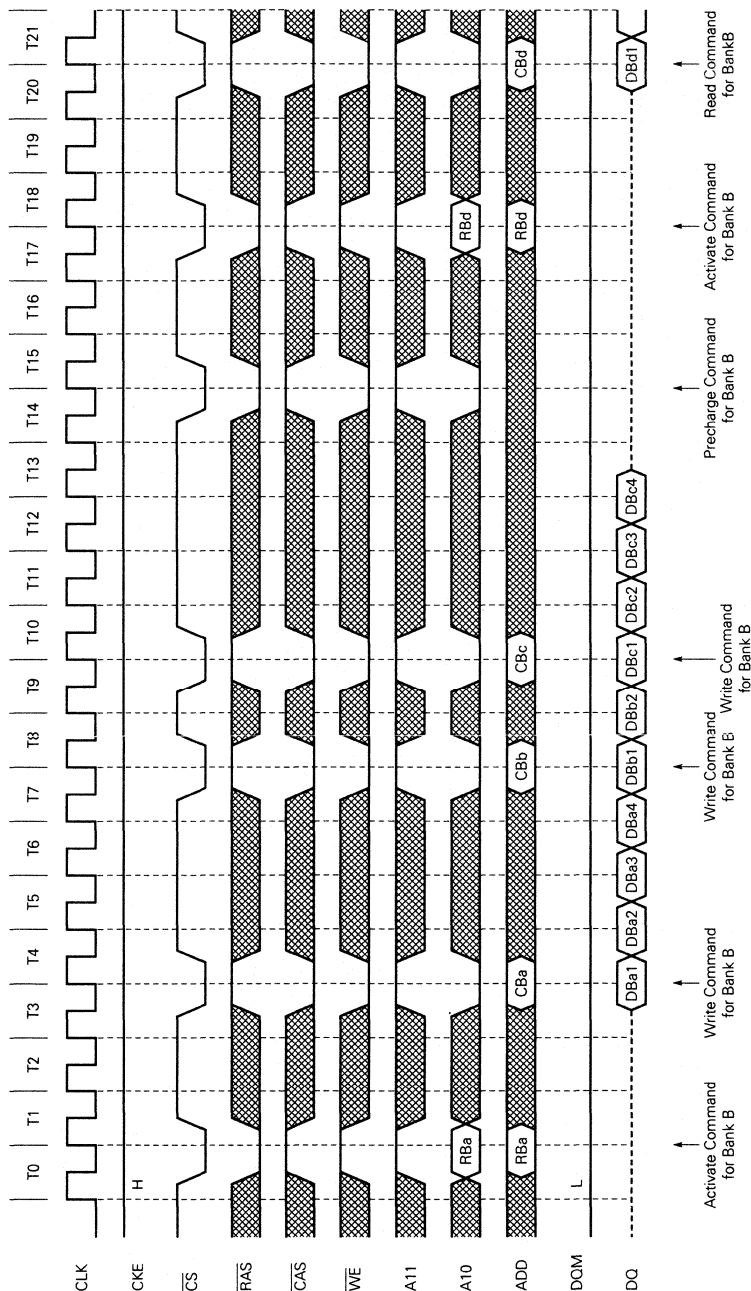
★ Random Column Write (Page with same bank) (2/3)

Burst length = 4 CAS latency = 2



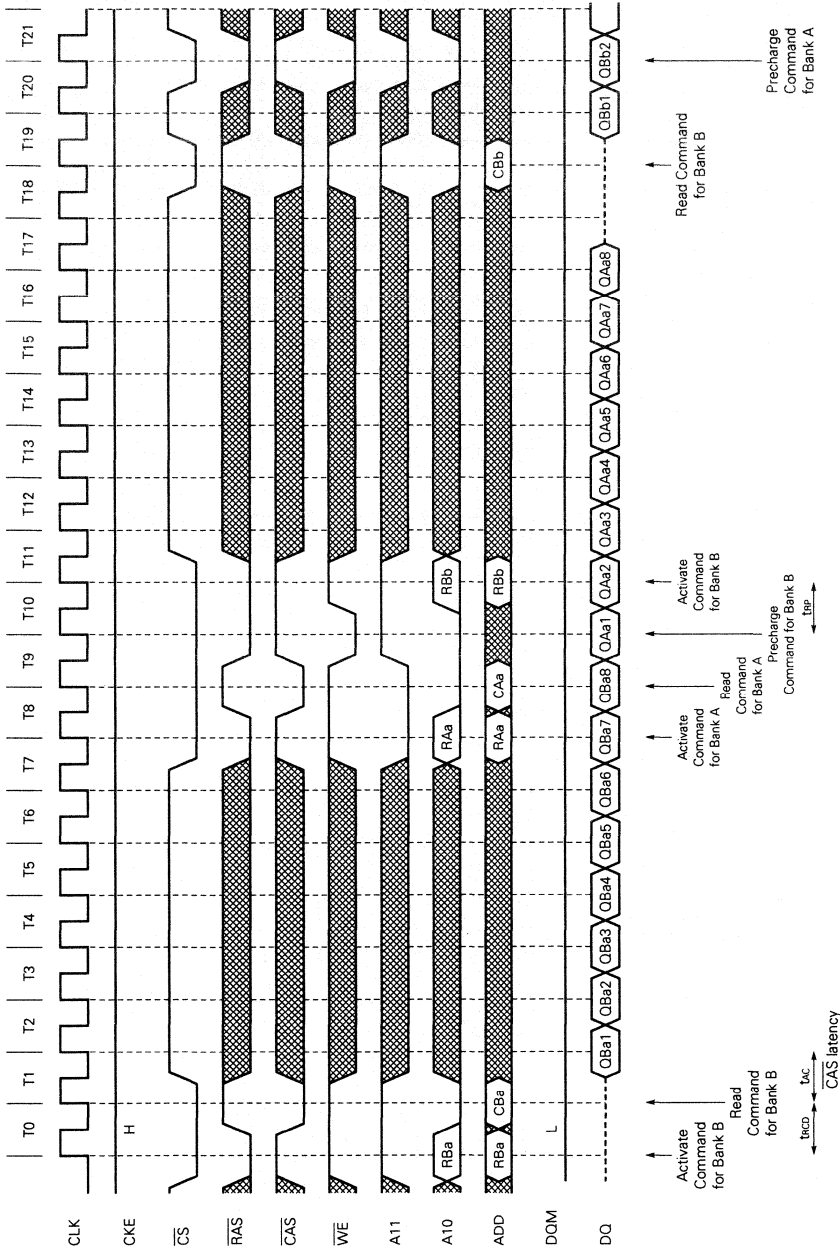
★ Random Column Write (Page with same bank) (3/3)

Burst length = 4 CAS latency = 3



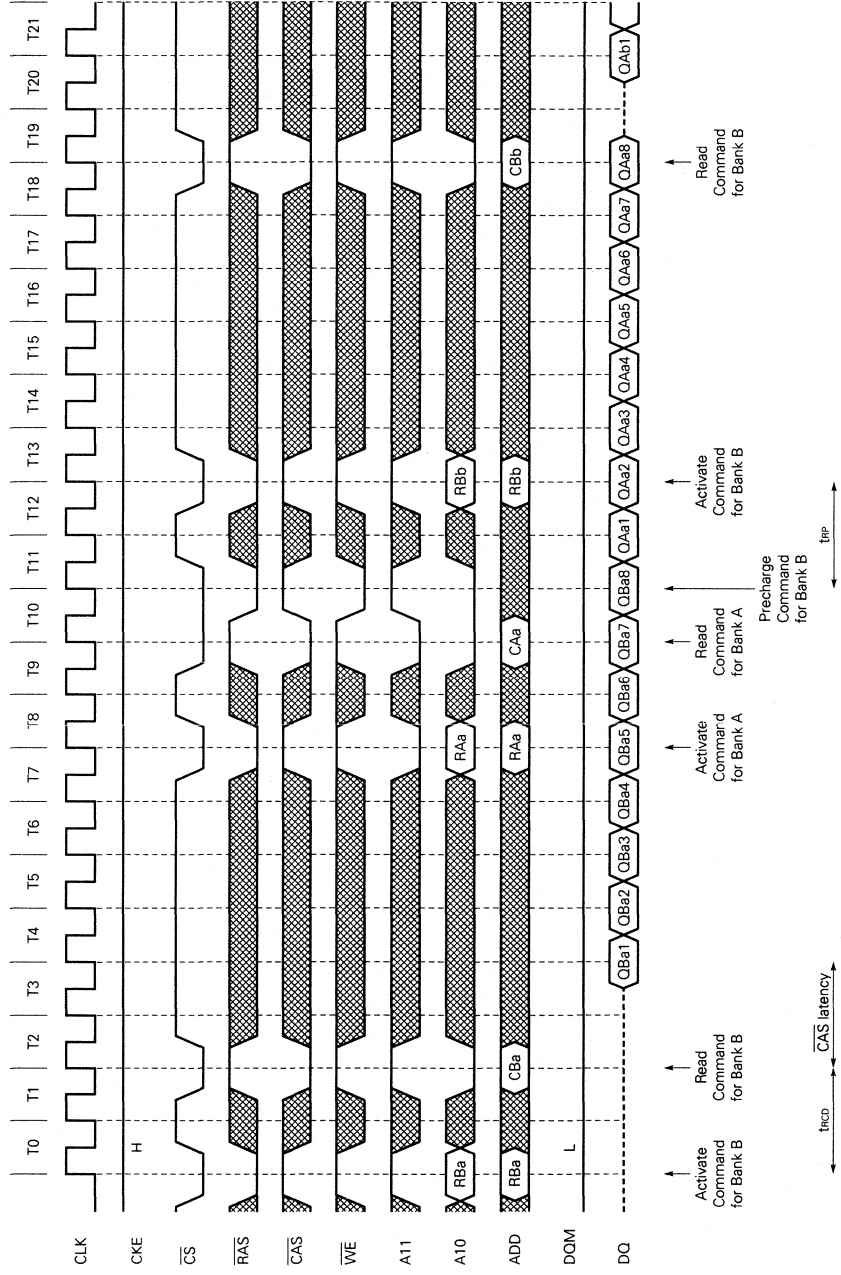
12.14 Random Row READ (Pingpong banks) (1/3)

Burst length = 8 $\overline{\text{CAS}}$ latency = 1



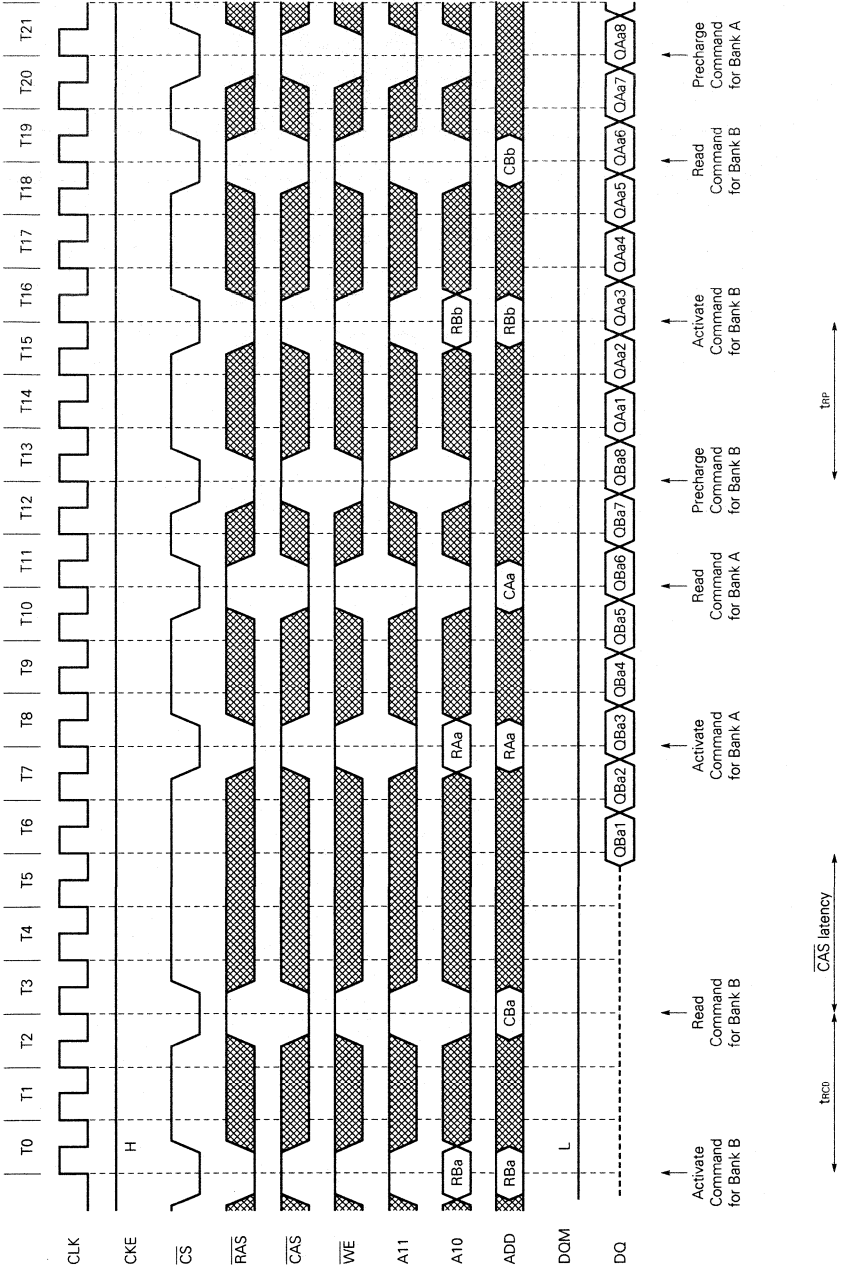
Random Row READ (Pingpong banks) (2/3)

Burst length = 8 CAS latency = 2



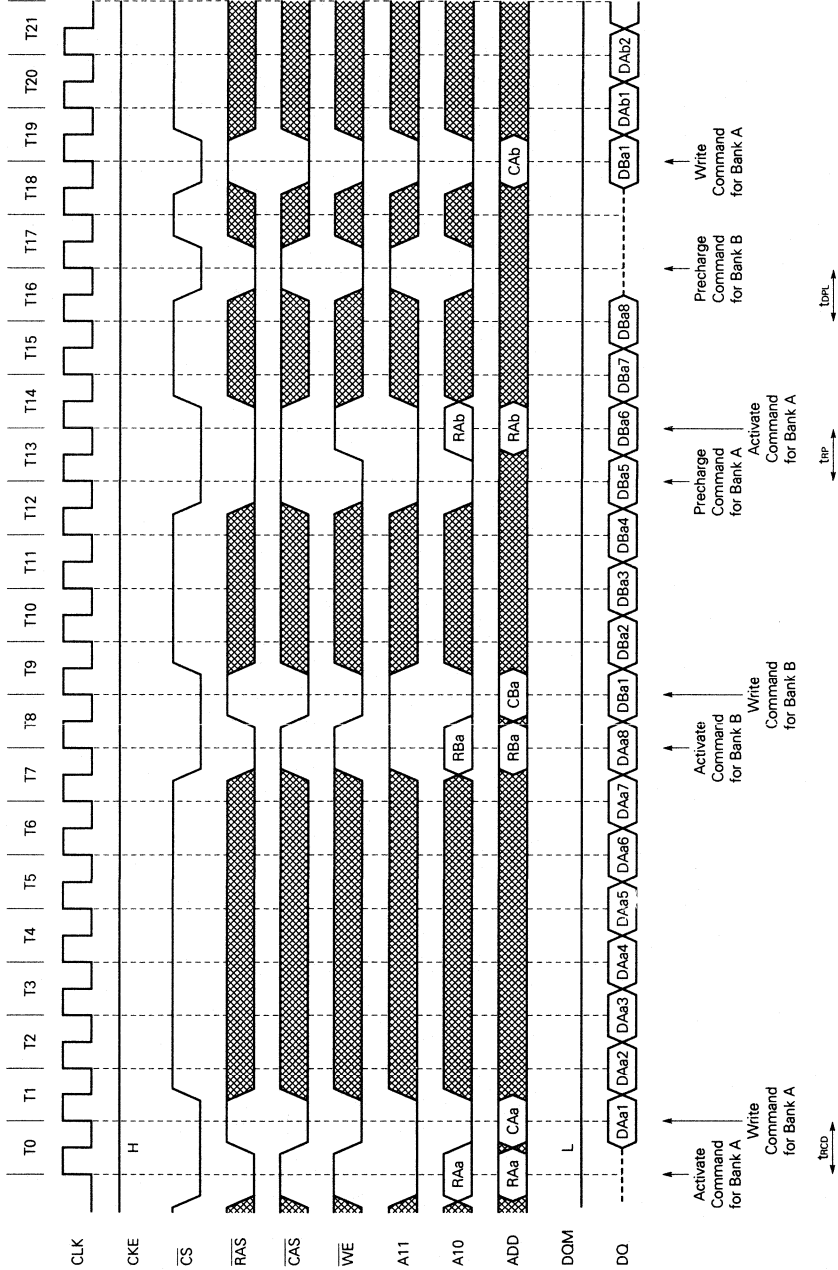
Random Row READ (Pingpong banks) (3/3)

Burst length = 8 CAS latency = 3



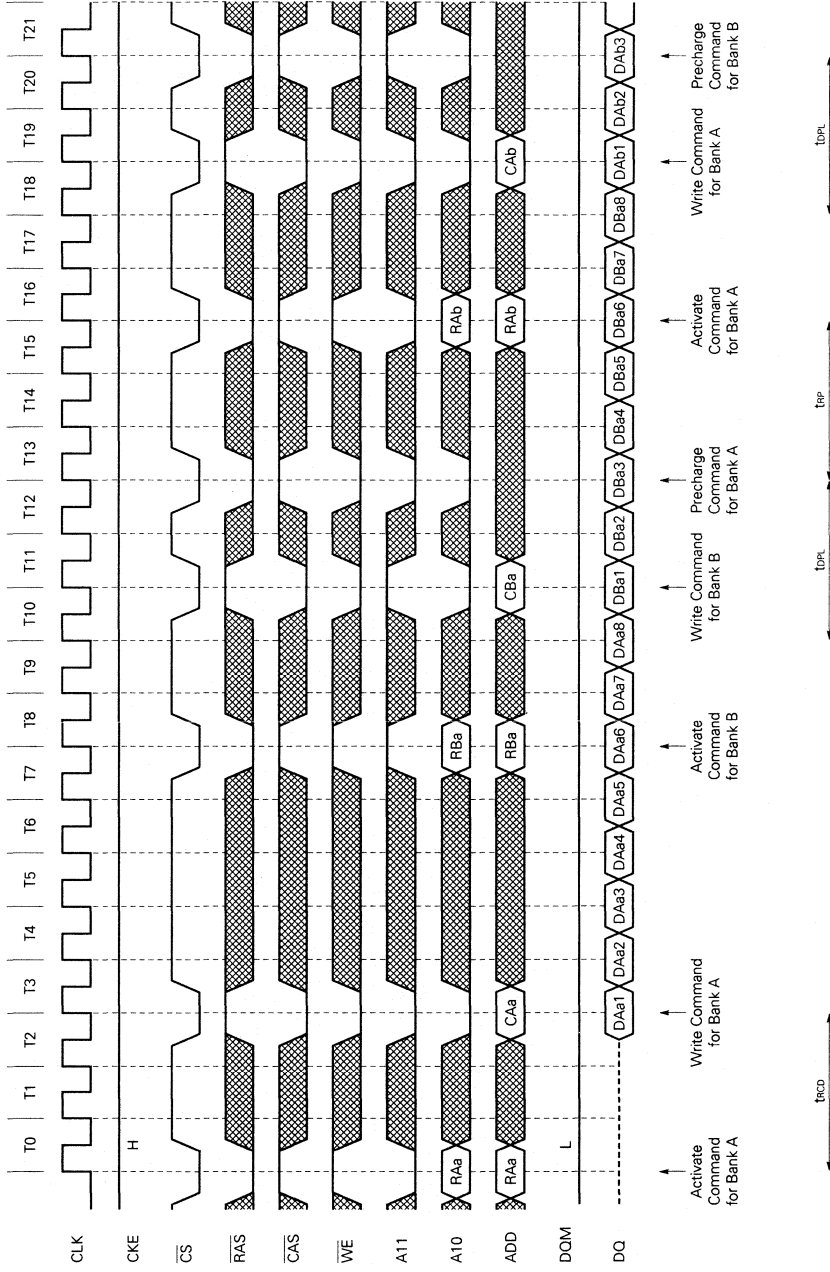
12.15 Random Row Write (Pingpong banks) (1/3)

Burst length = 8 CAS latency = 1



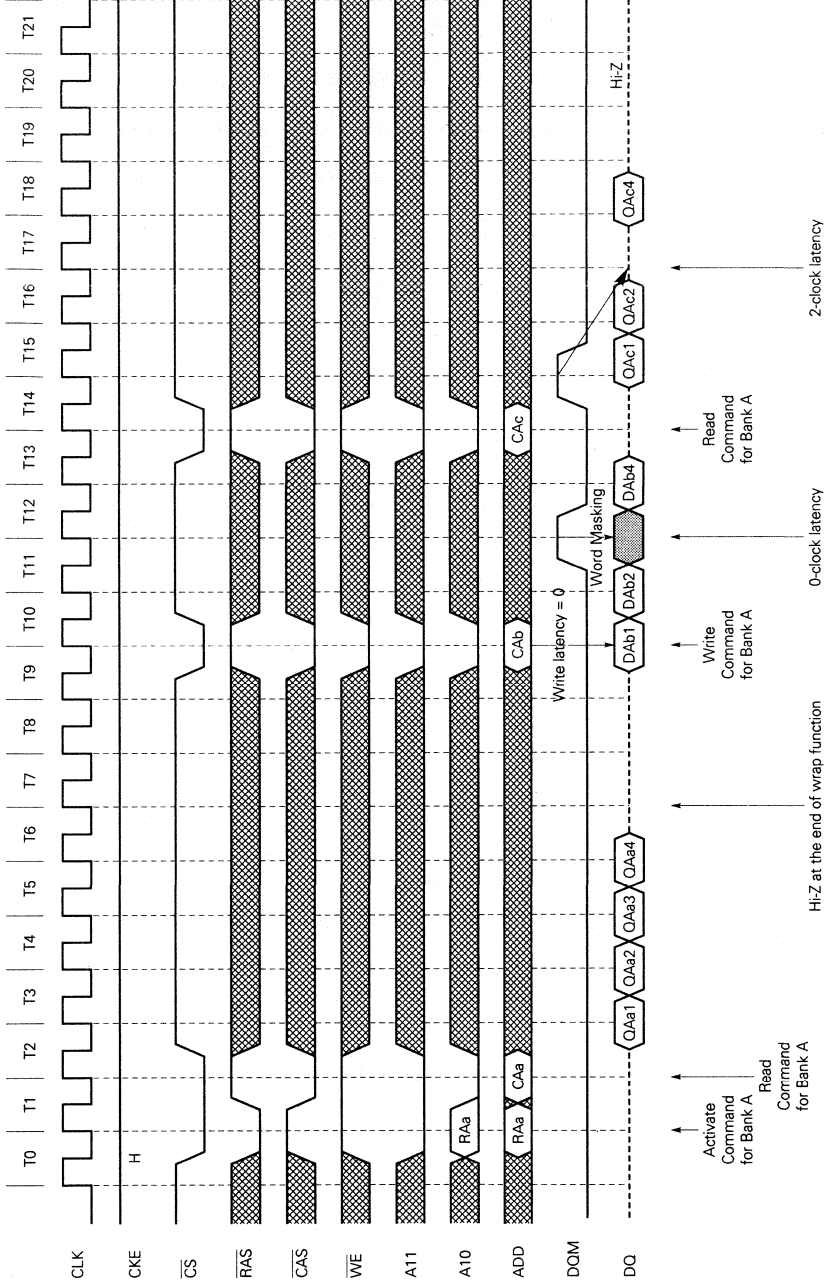
Random Row Write (Pingpong banks) (3/3)

Burst length = 8 CAS latency = 3



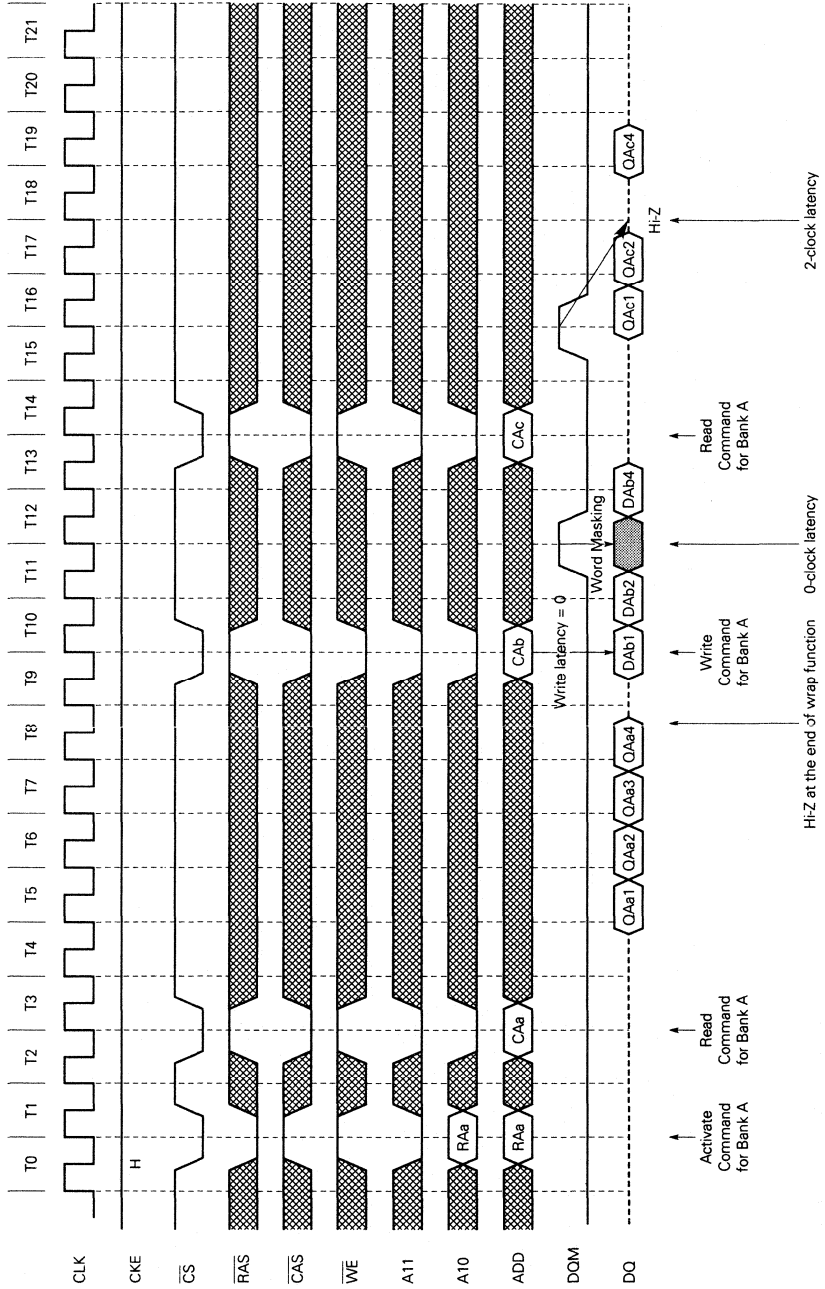
12.16 READ and WRITE (1/3)

Burst length = 4 CAS latency = 1



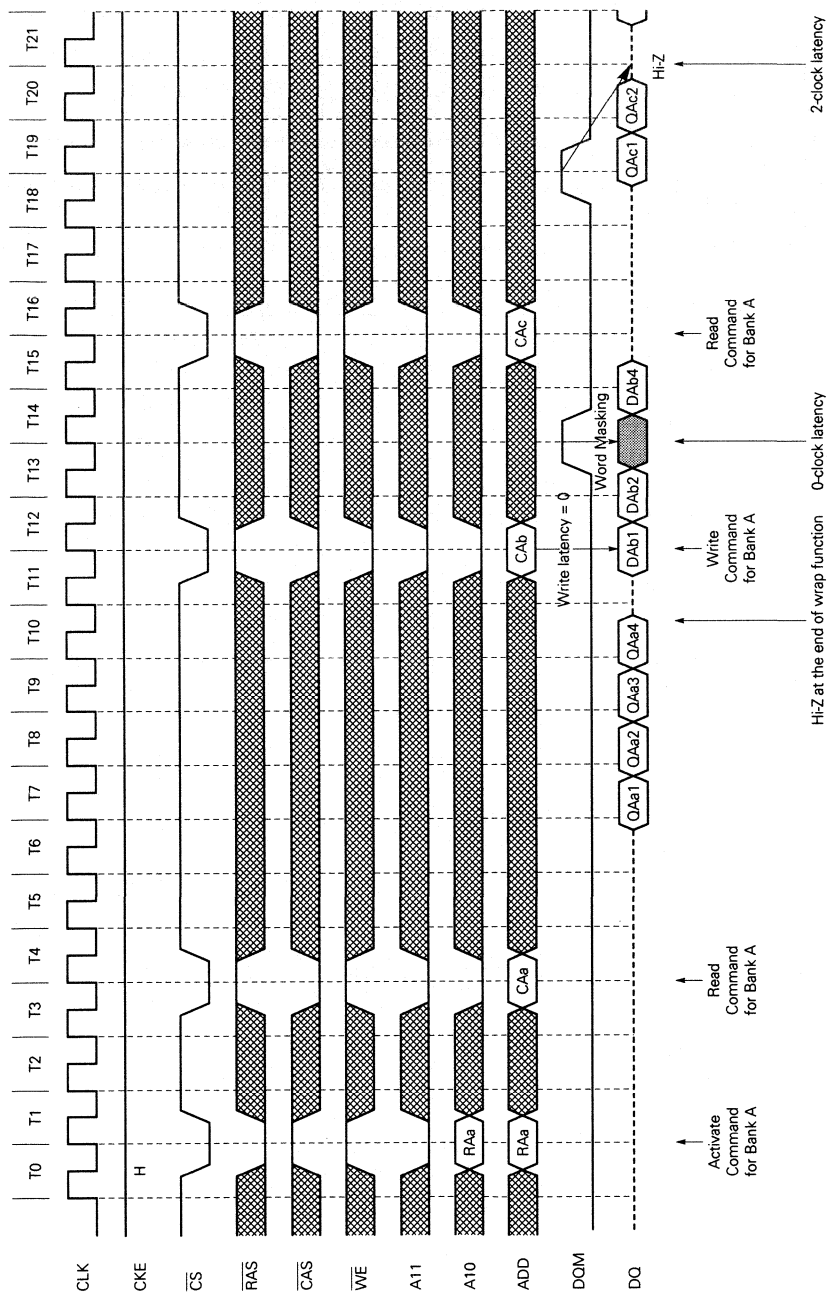
READ and WRITE (2/3)

Burst length = 4 CAS latency = 2



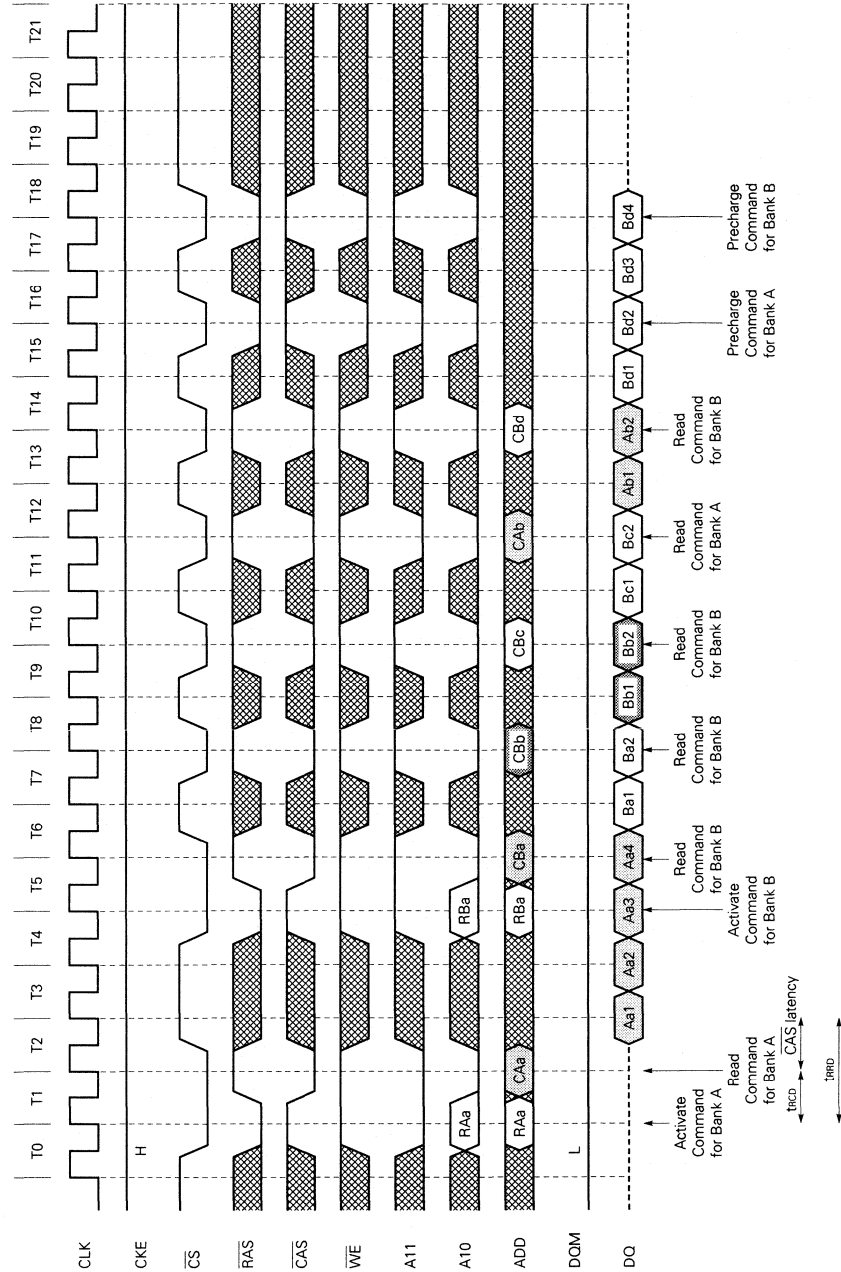
READ and WRITE (3/3)

Burst length = 4 CAS latency = 3



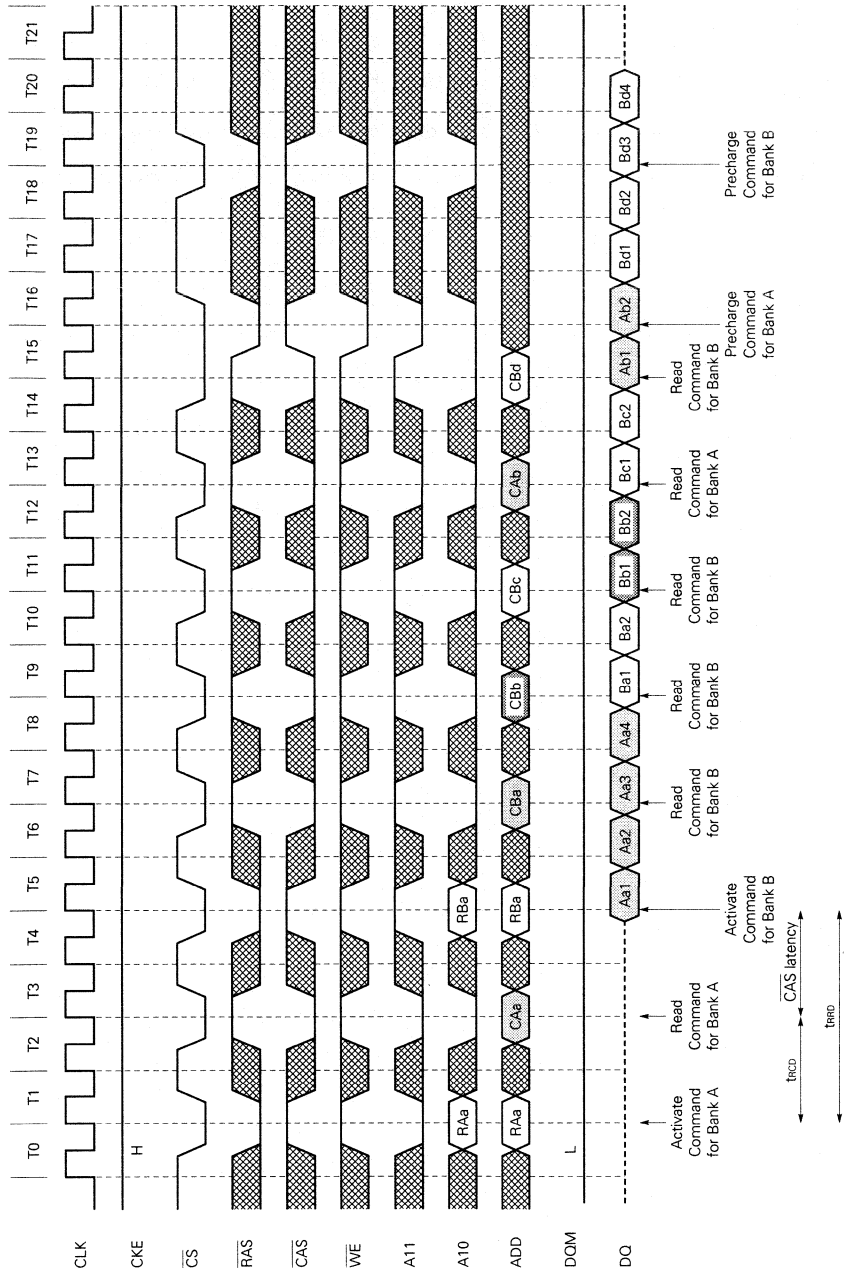
12.17 Interleaved Column READ Cycle (1/3)

Burst length = 4 CAS latency = 1

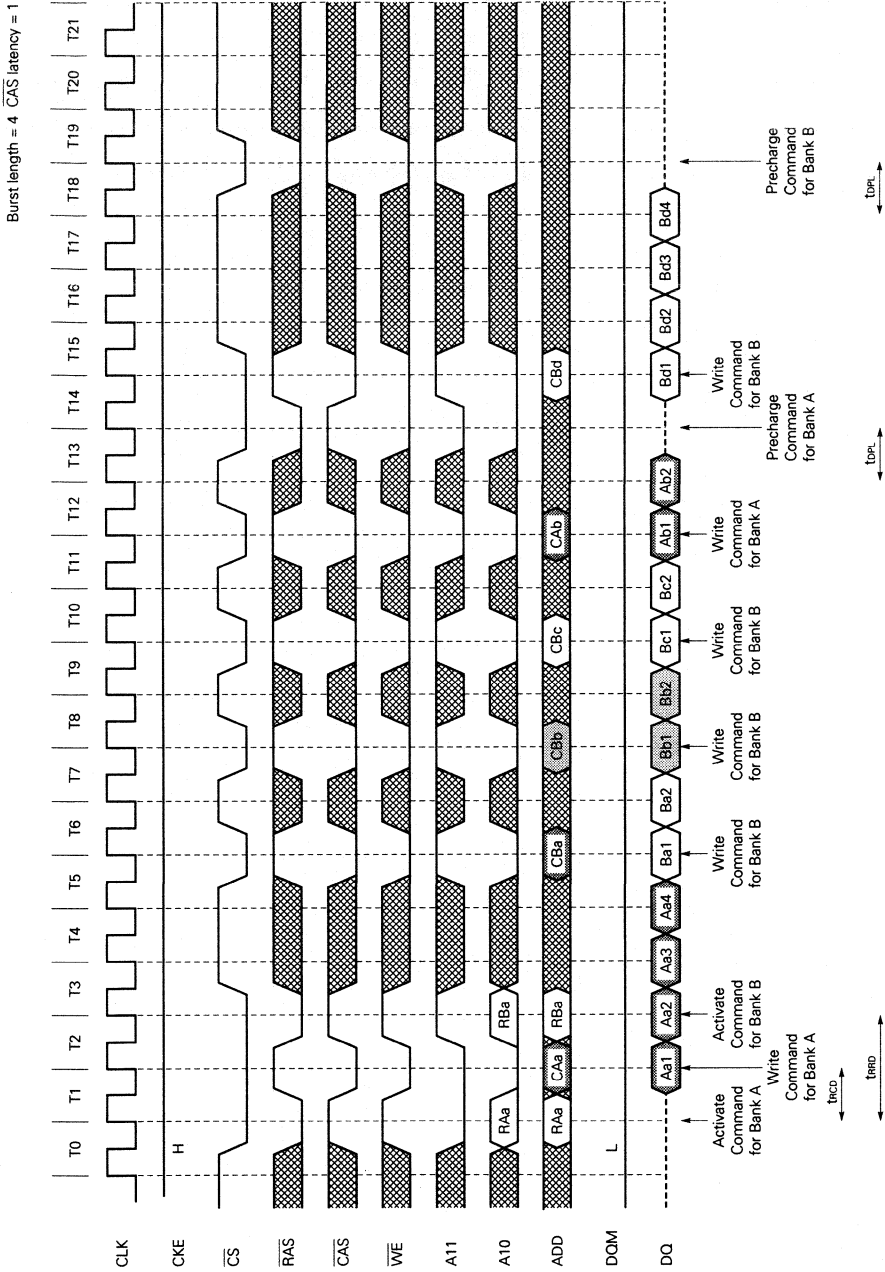


Interleaved Column READ Cycle (2/3)

Burst length = 4 CAS latency = 2

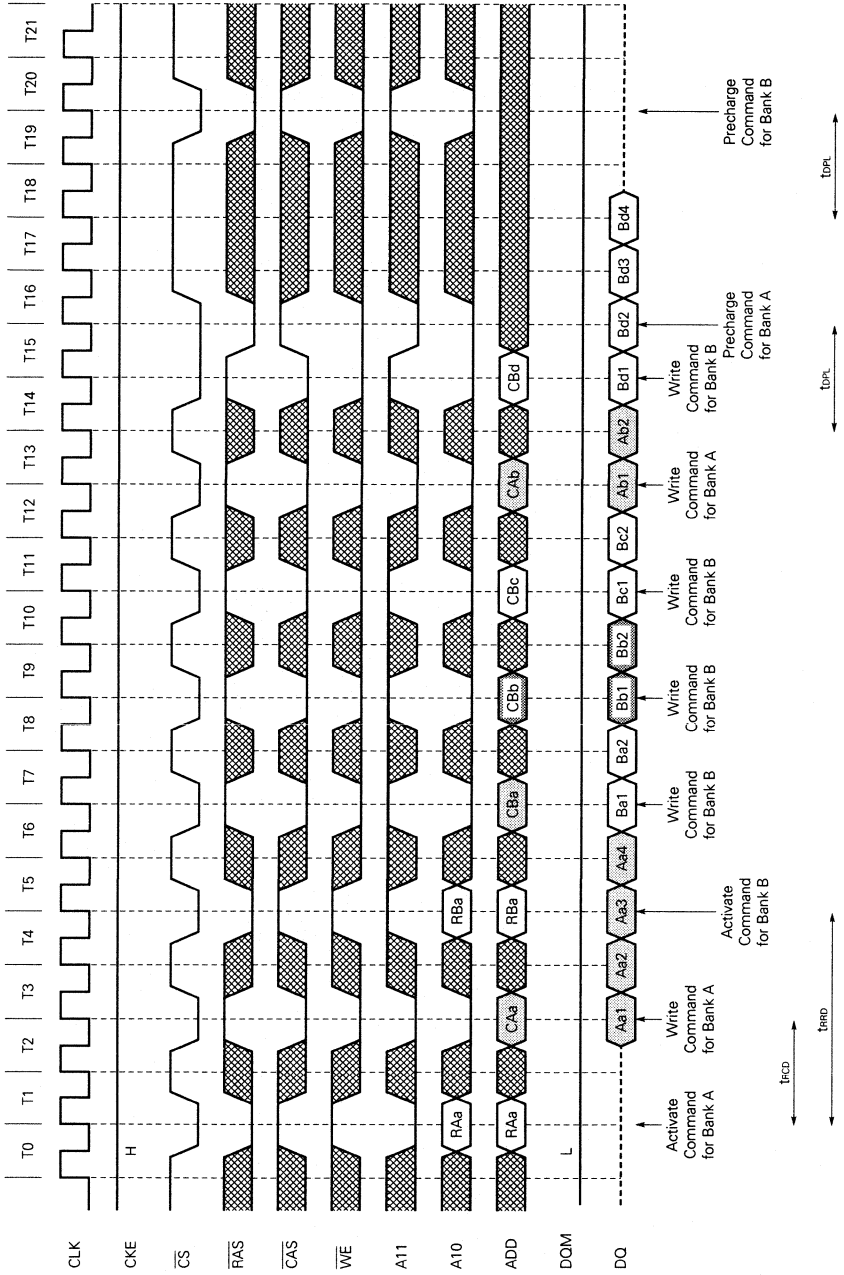


12.18 Interleaved Column WRITE Cycle (1/3)



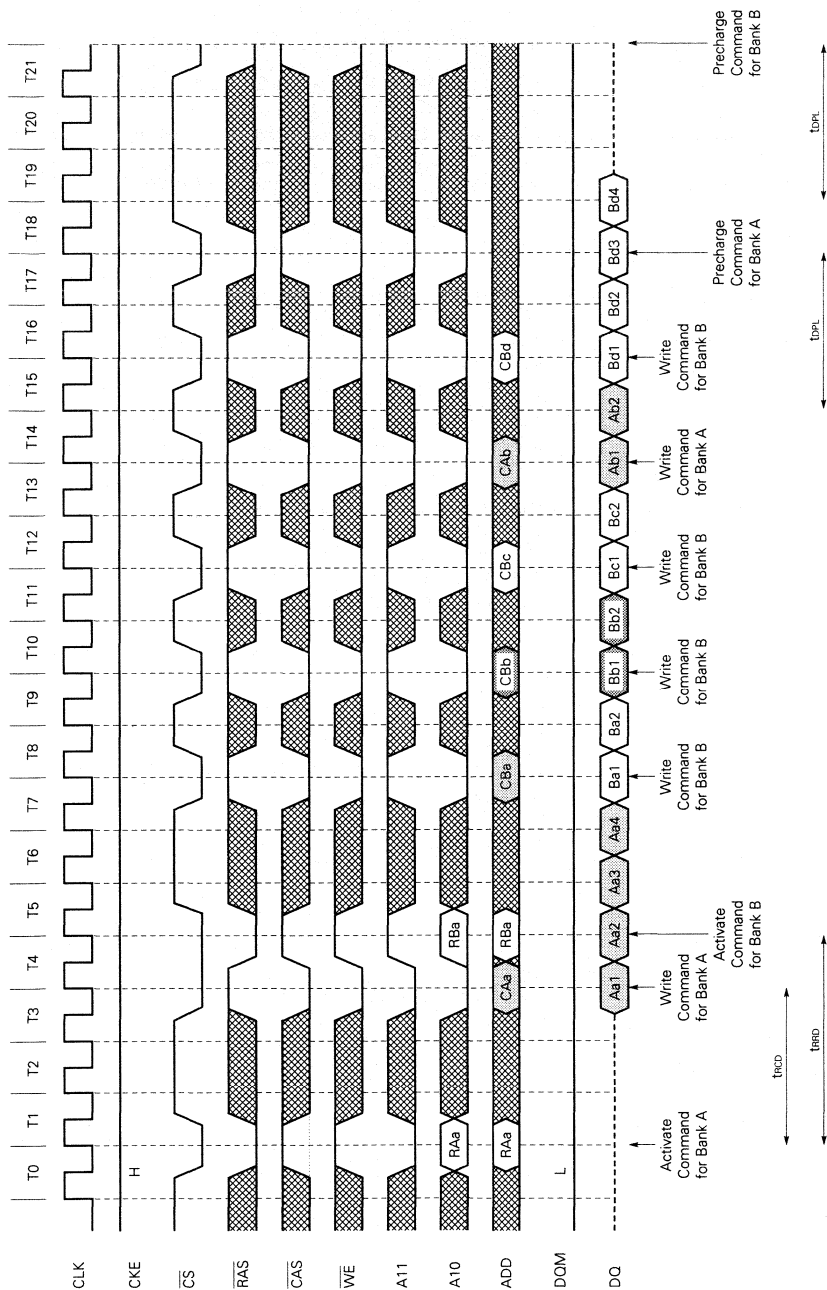
Interleaved Column WRITE Cycle (2/3)

Burst length = 4 CAS latency = 2



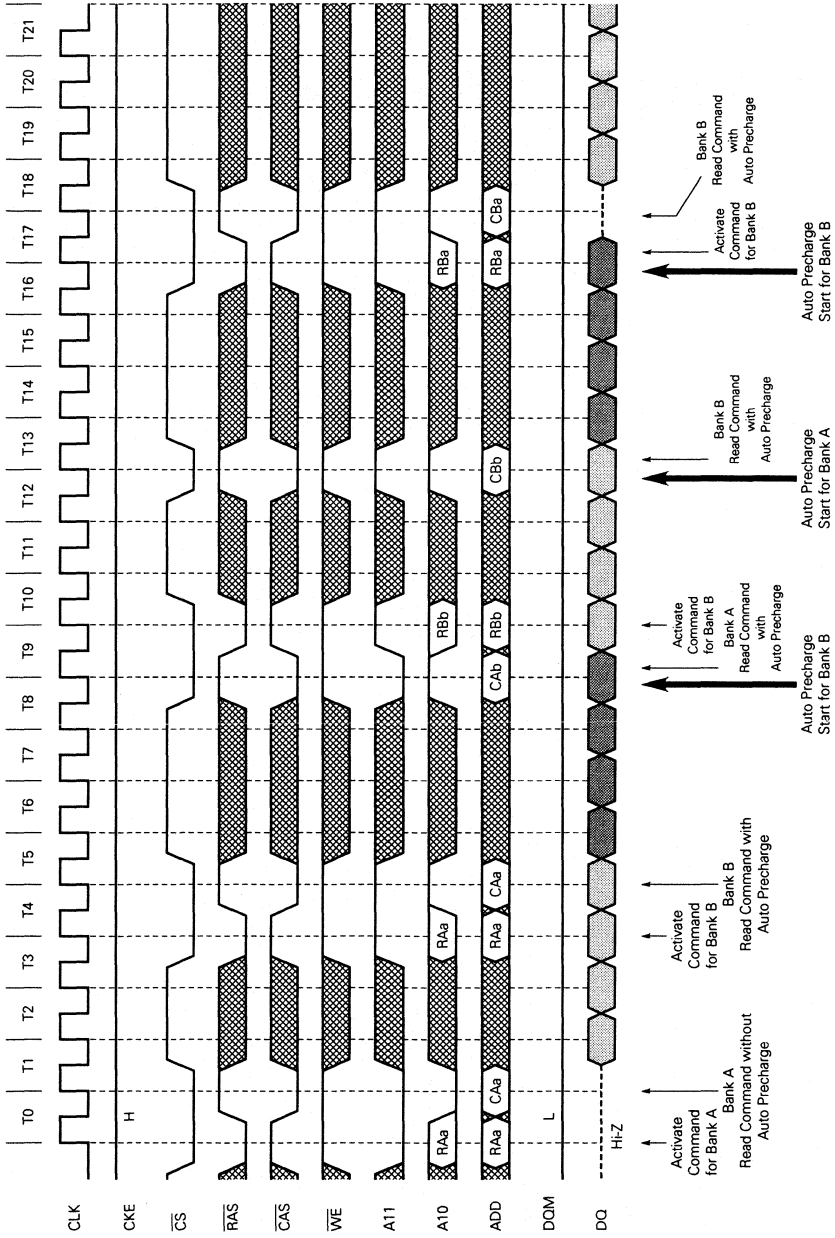
Interleaved Column WRITE Cycle (3/3)

Burst length = 4 CAS latency = 3



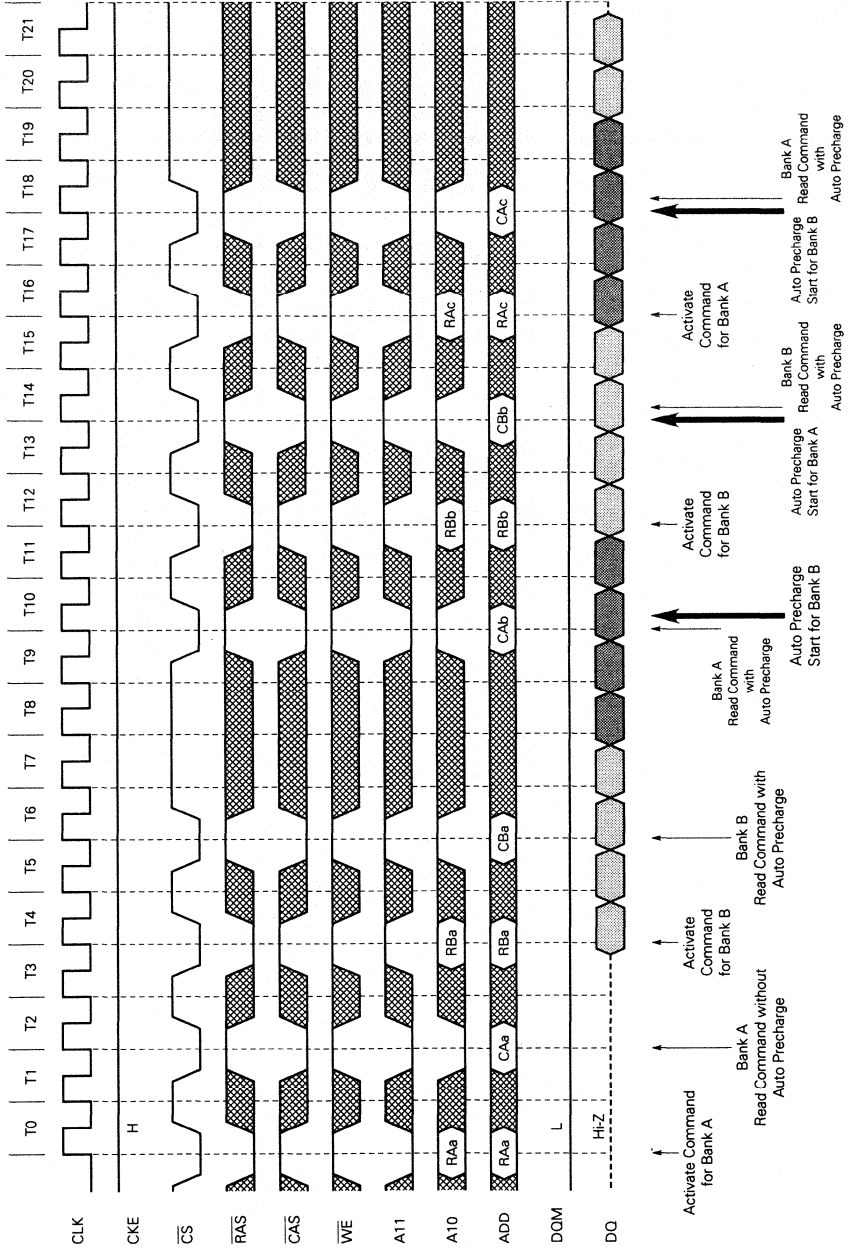
12.19 Auto Precharge after Read Burst (1/3)

Burst length = 4 CAS latency = 1



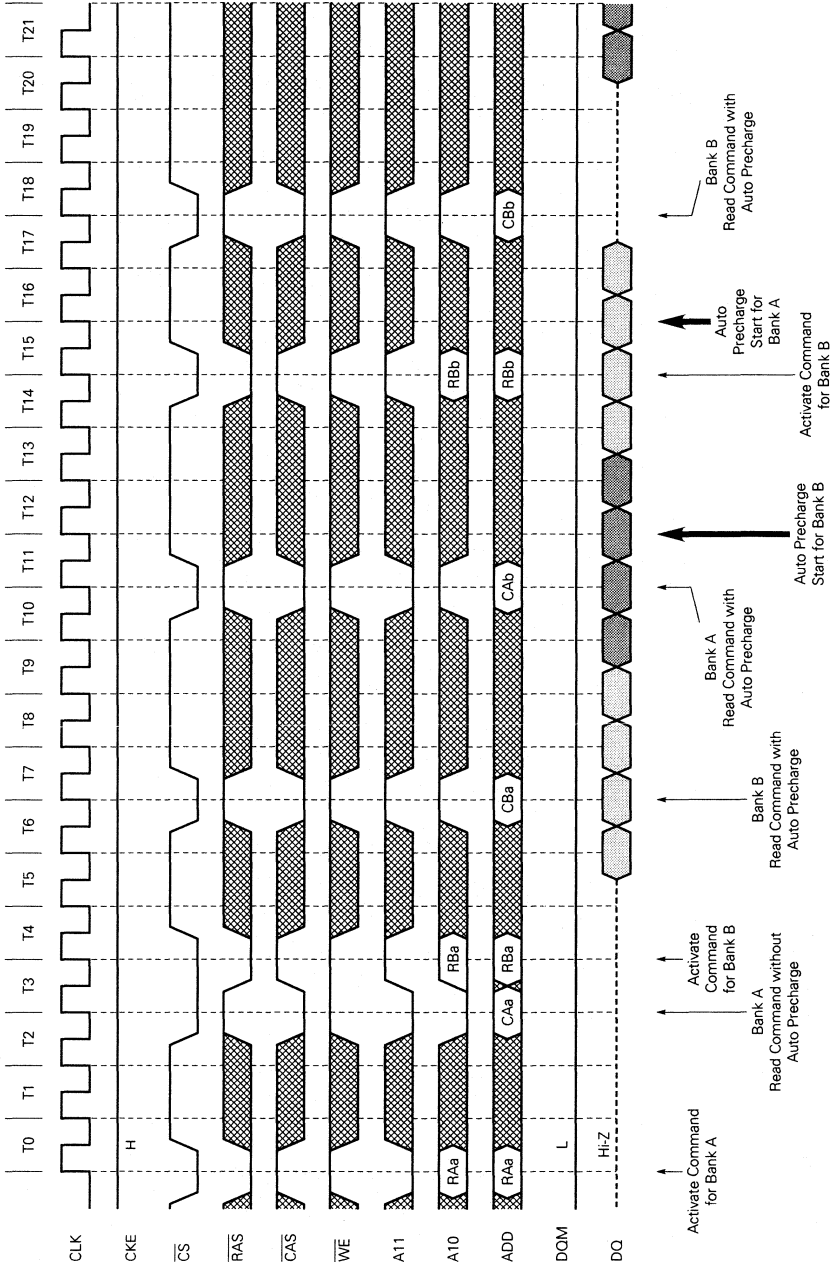
Auto Precharge after Read Burst (2/3)

Burst length = 4 CAS latency = 2

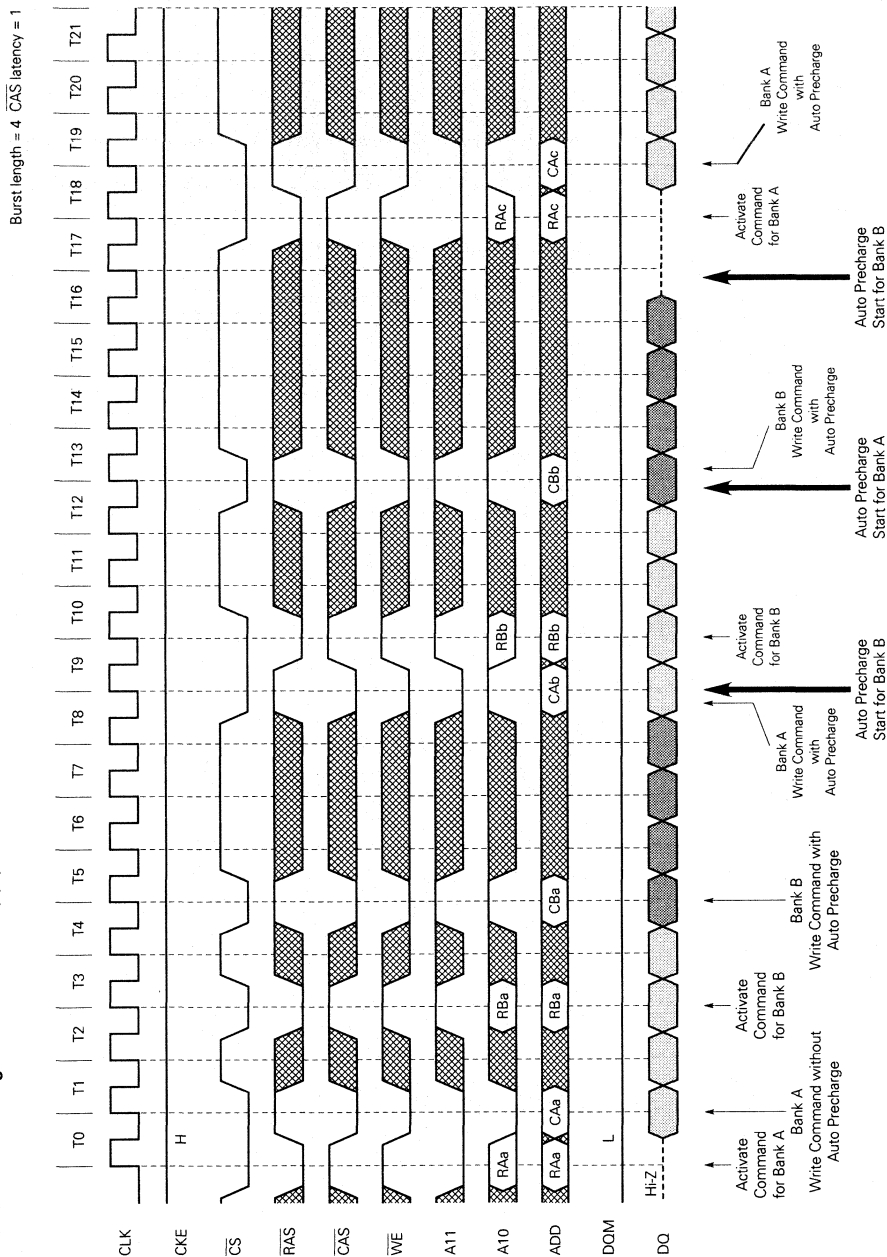


Auto Precharge after Read Burst (3/3)

Burst length = 4 CAS latency = 3

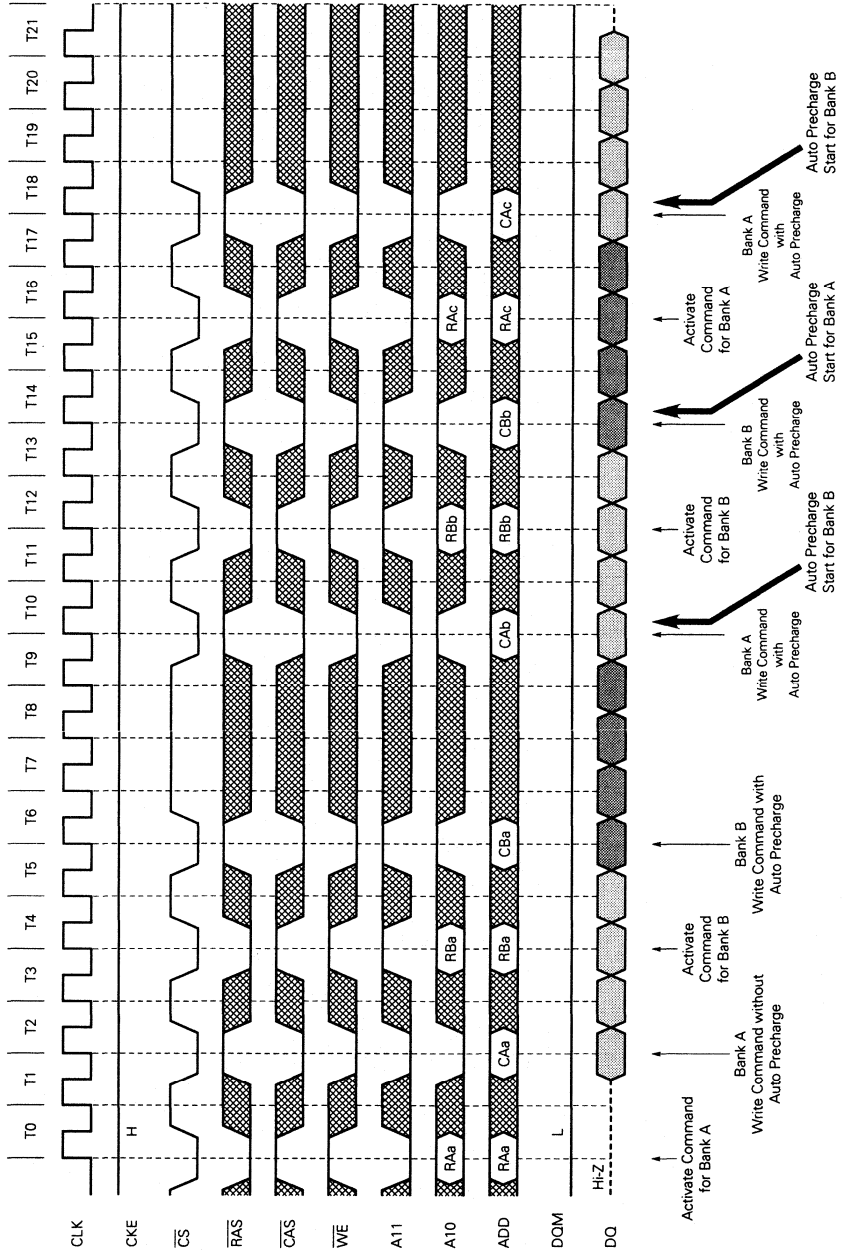


12.20 Auto Precharge after Write Burst (1/3)



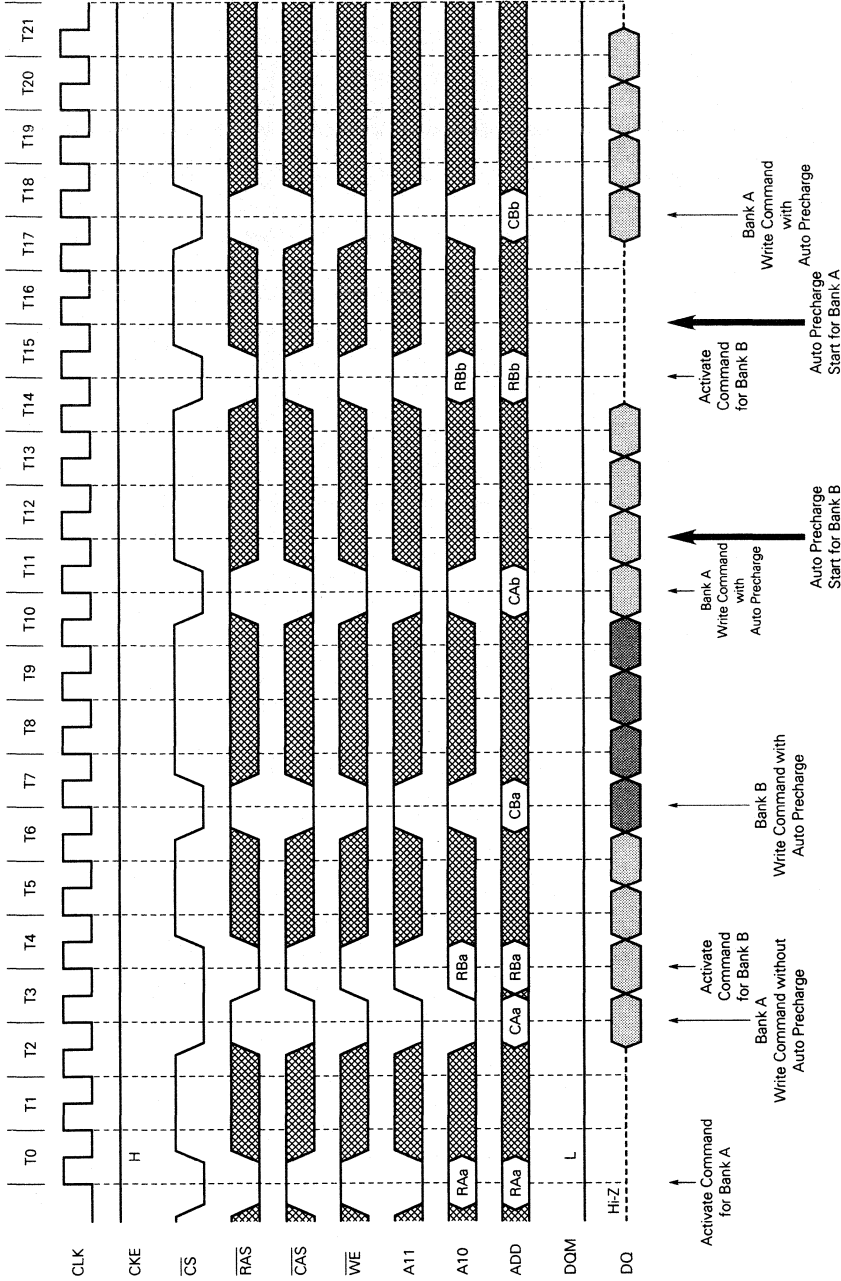
Auto Precharge after Write Burst (2/3)

Burst length = 4 CAS latency = 2



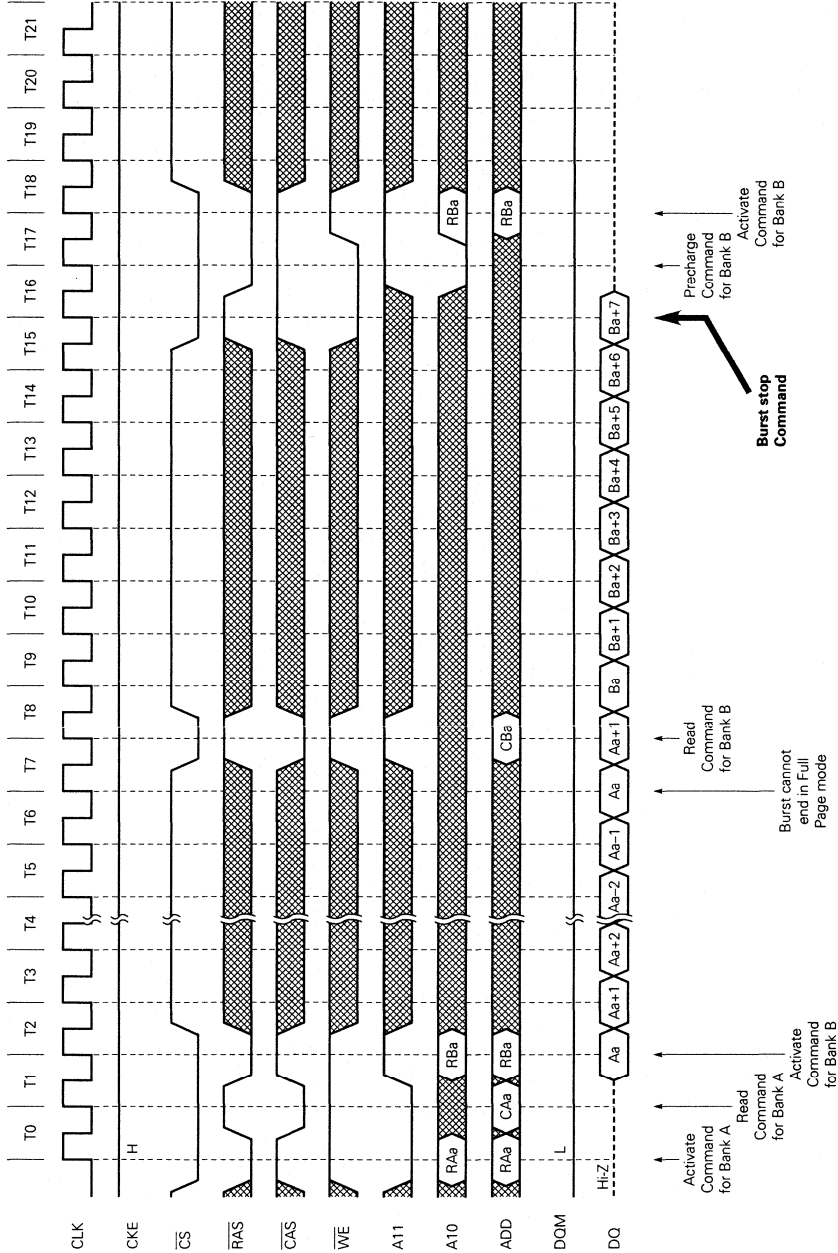
Auto Precharge after Write Burst (3/3)

Burst length = 4 CAS latency = 3



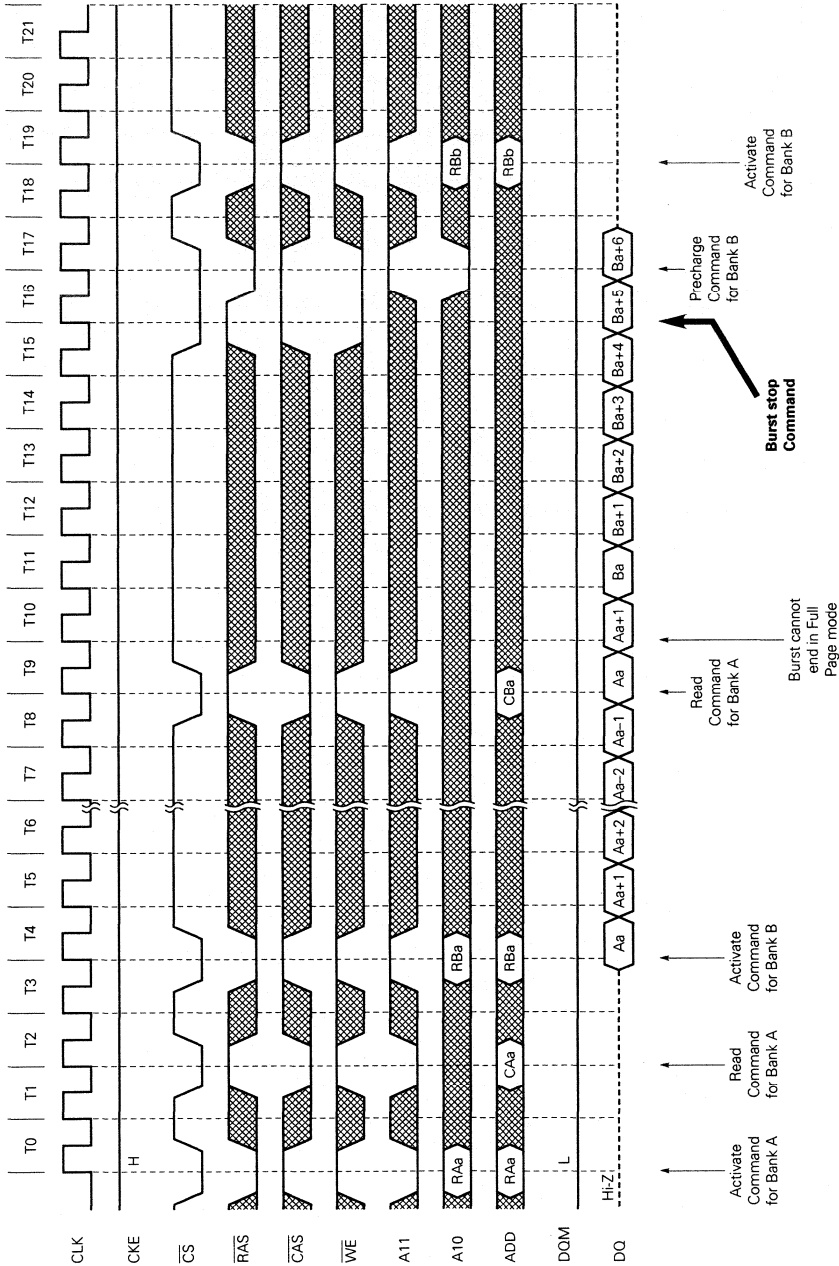
12.21 Full Page READ Cycle (1/3)

CAS latency = 1



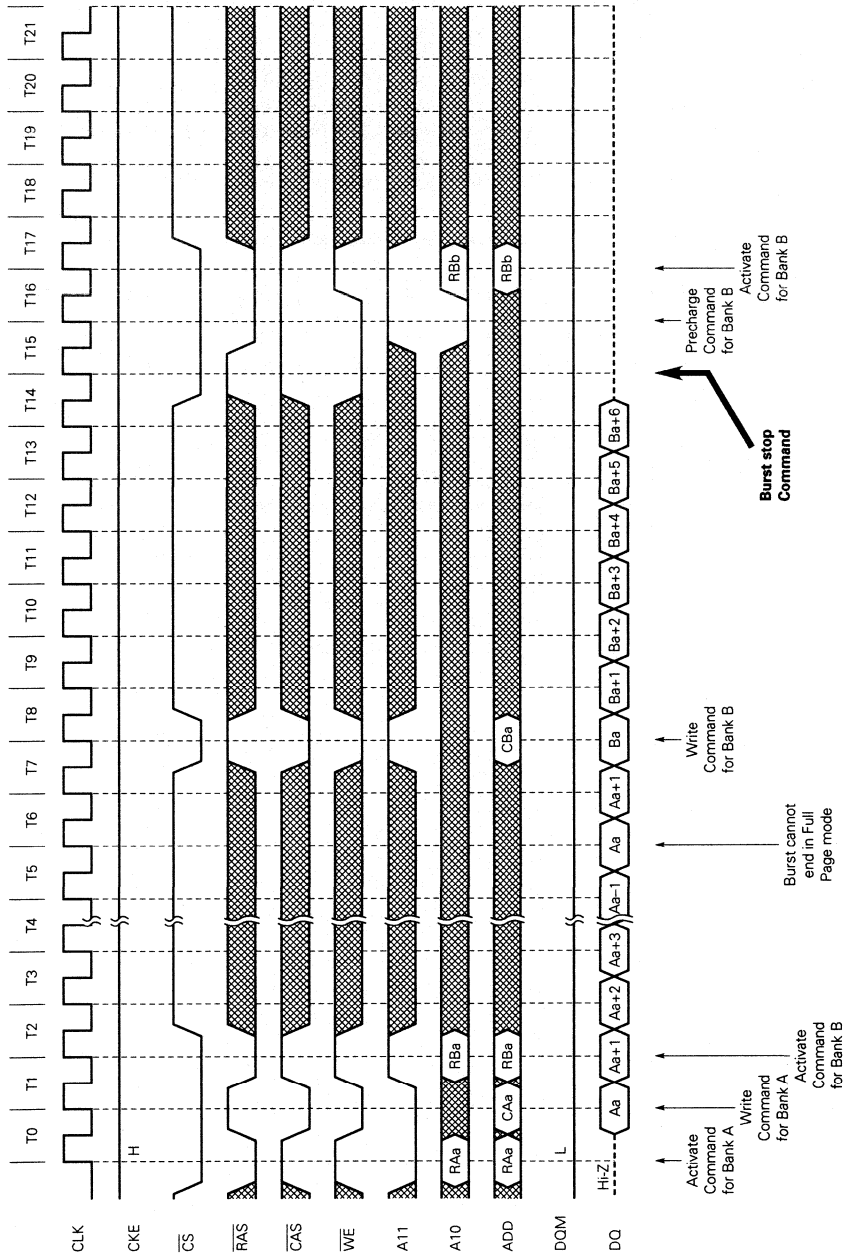
Full Page READ Cycle (2/3)

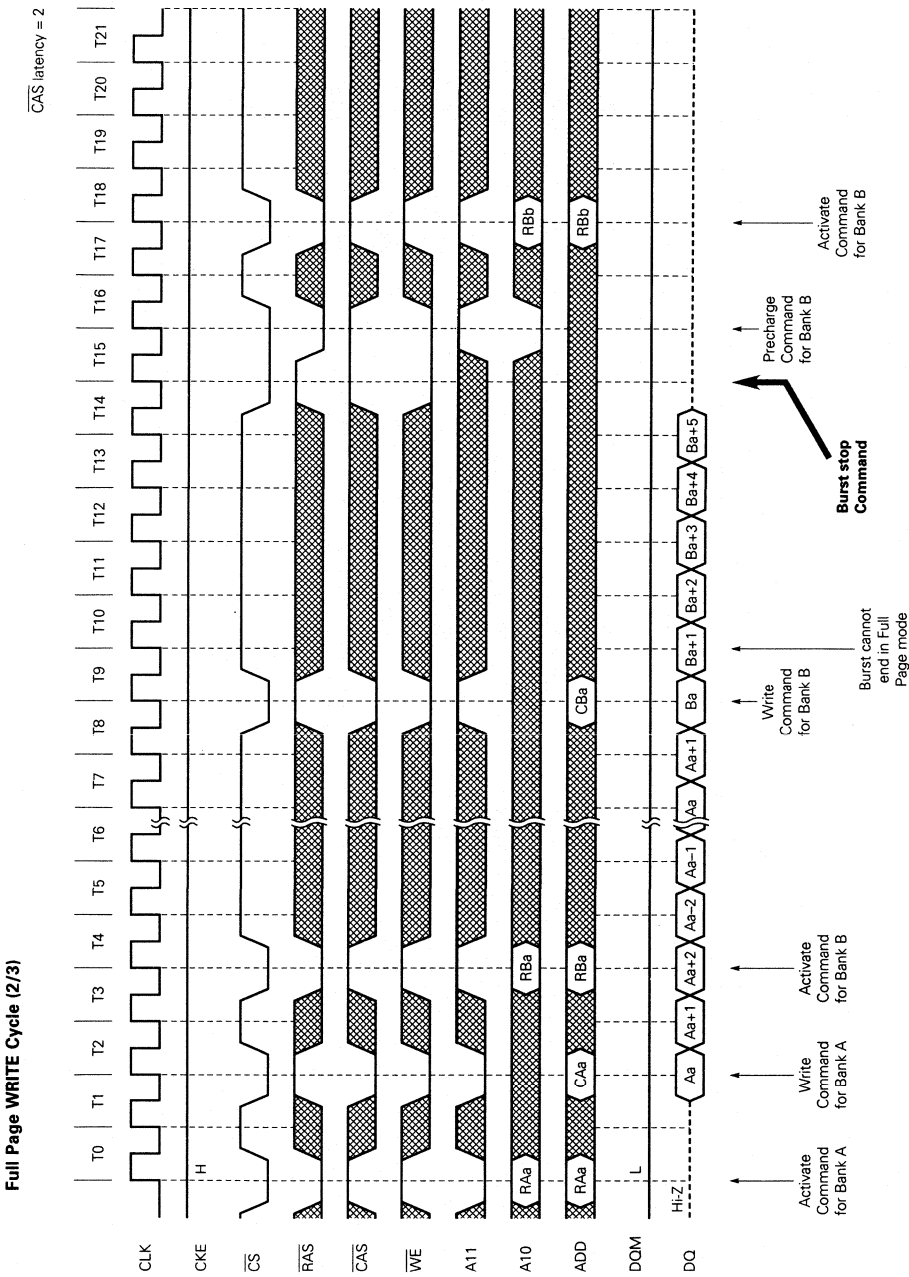
CAS latency = 2



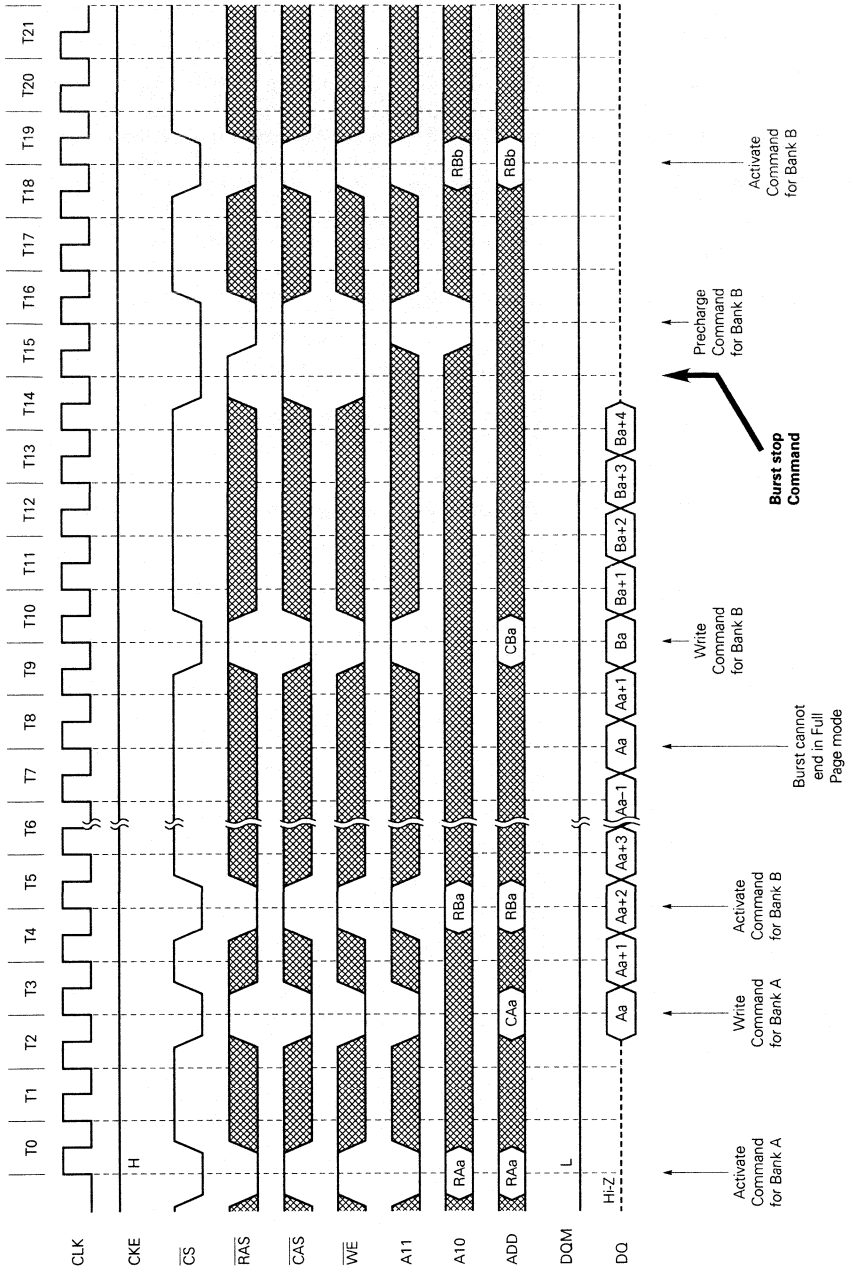
12.22 Full Page WRITE Cycle (1/3)

CAS latency = 1



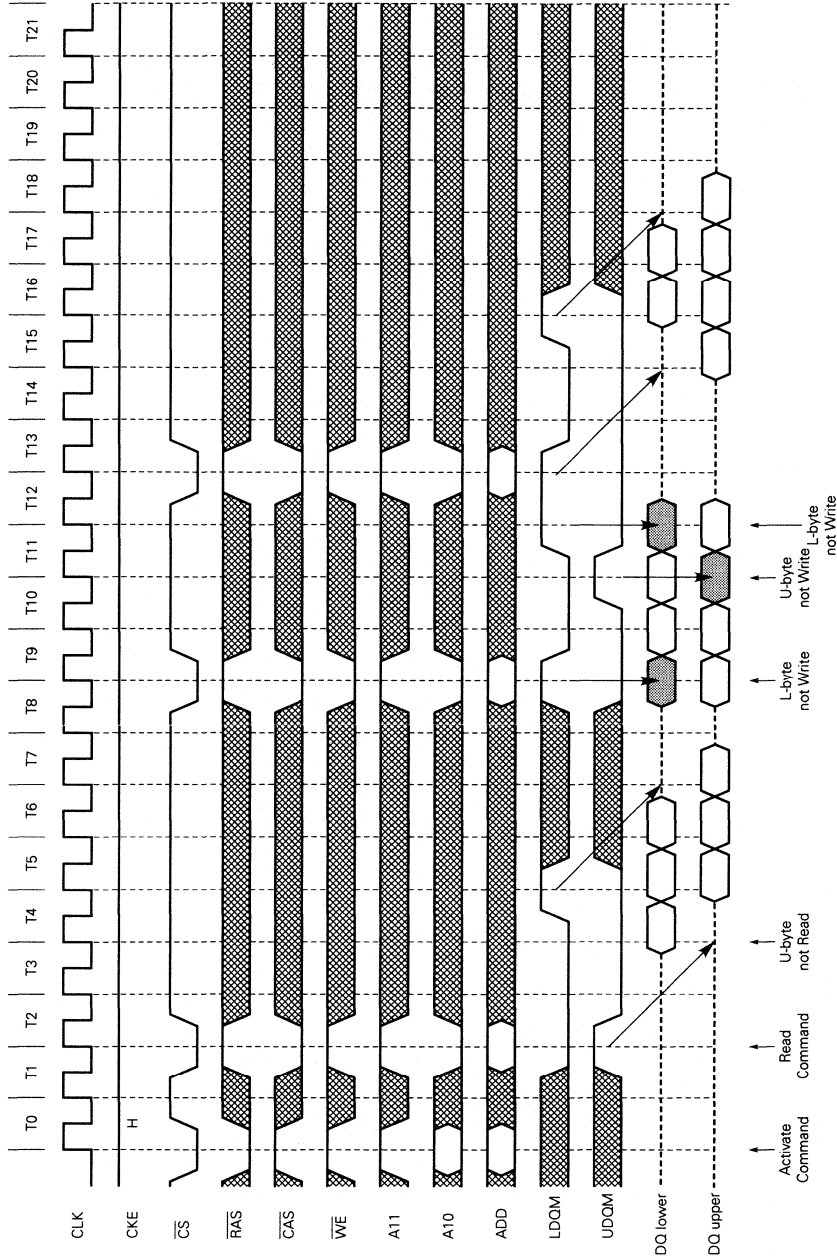


CAS latency = 3

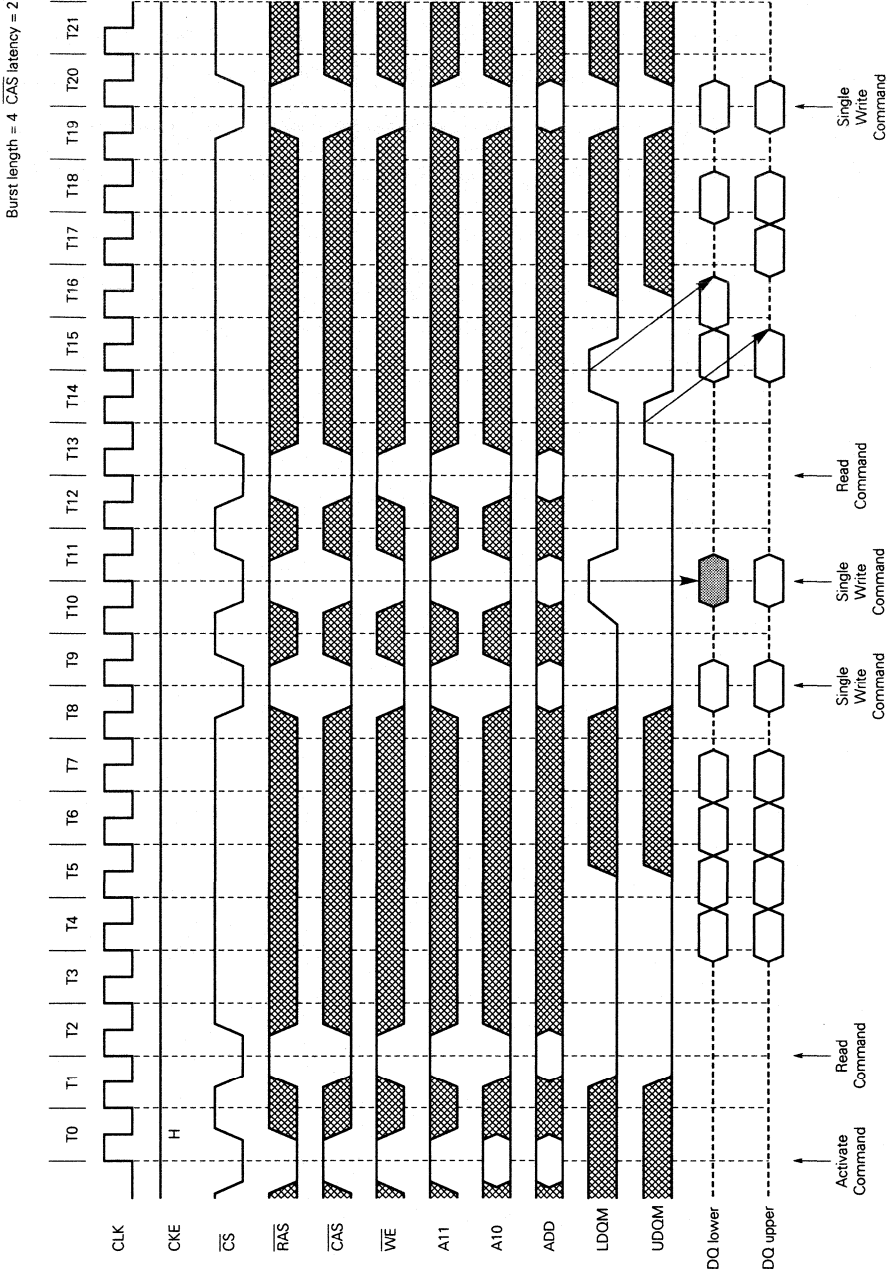


12.23 Byte Write Operation

Burst length = 4 CAS latency = 2

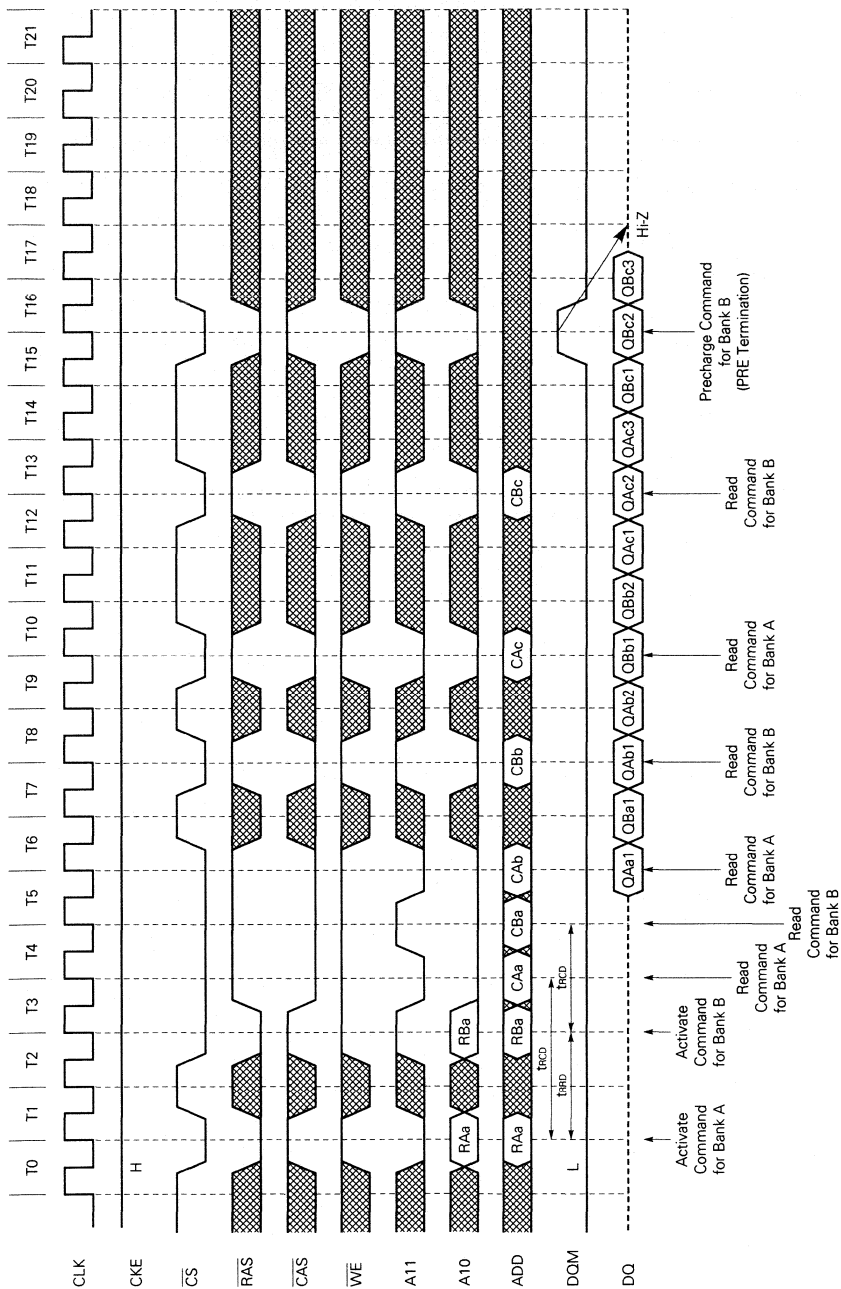


12.24 Burst Read and Single Write (Option)



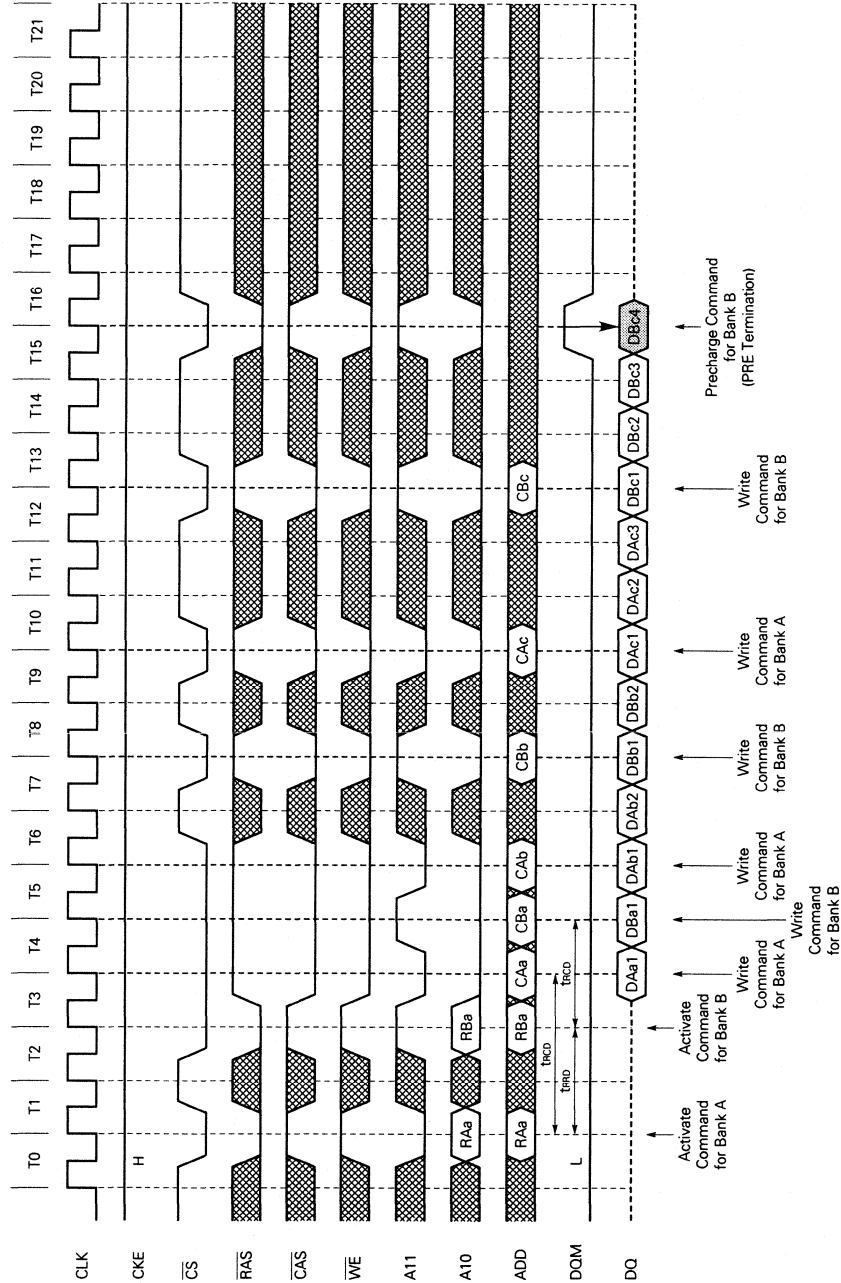
12.26 Full Page Random Column Read

Burst length = Full Page CAS latency = 2



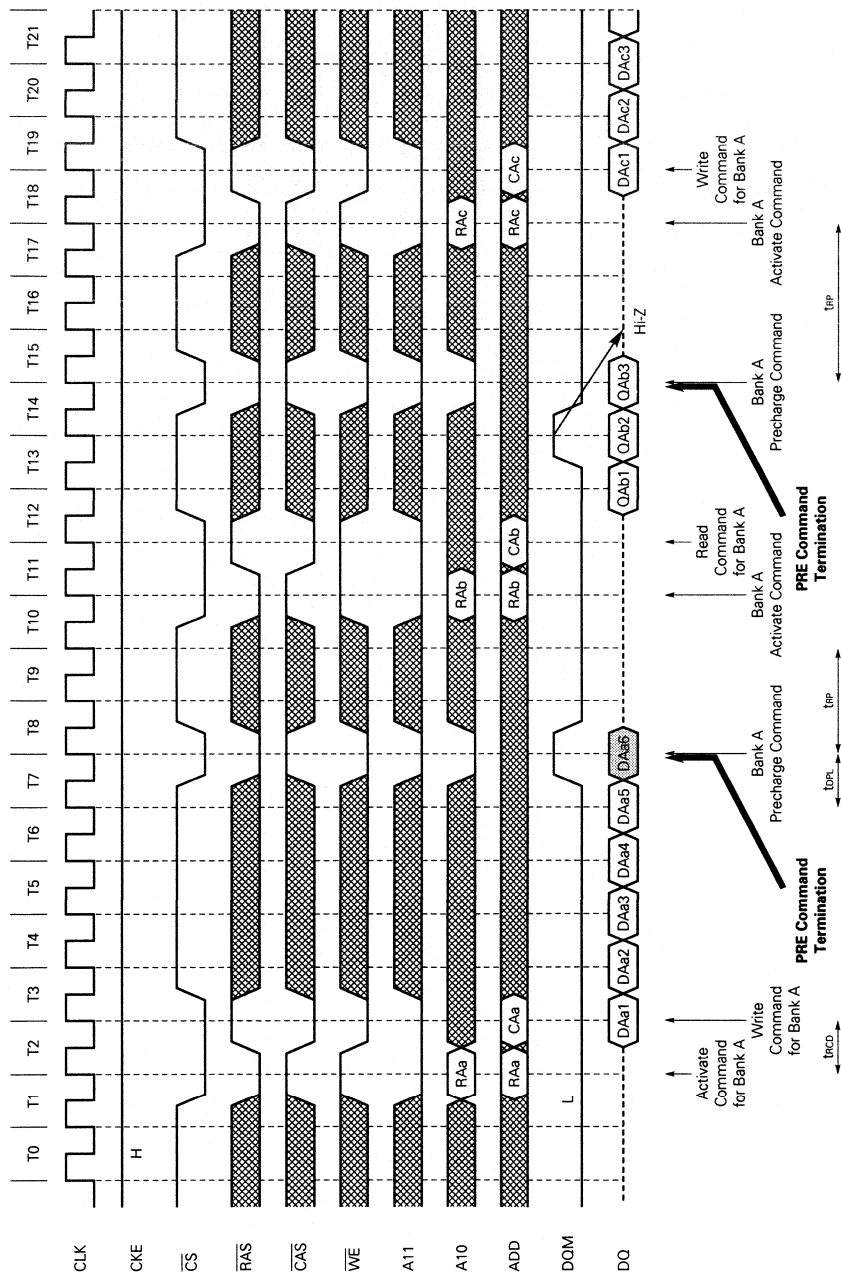
12.27 Full Page Random Column Write

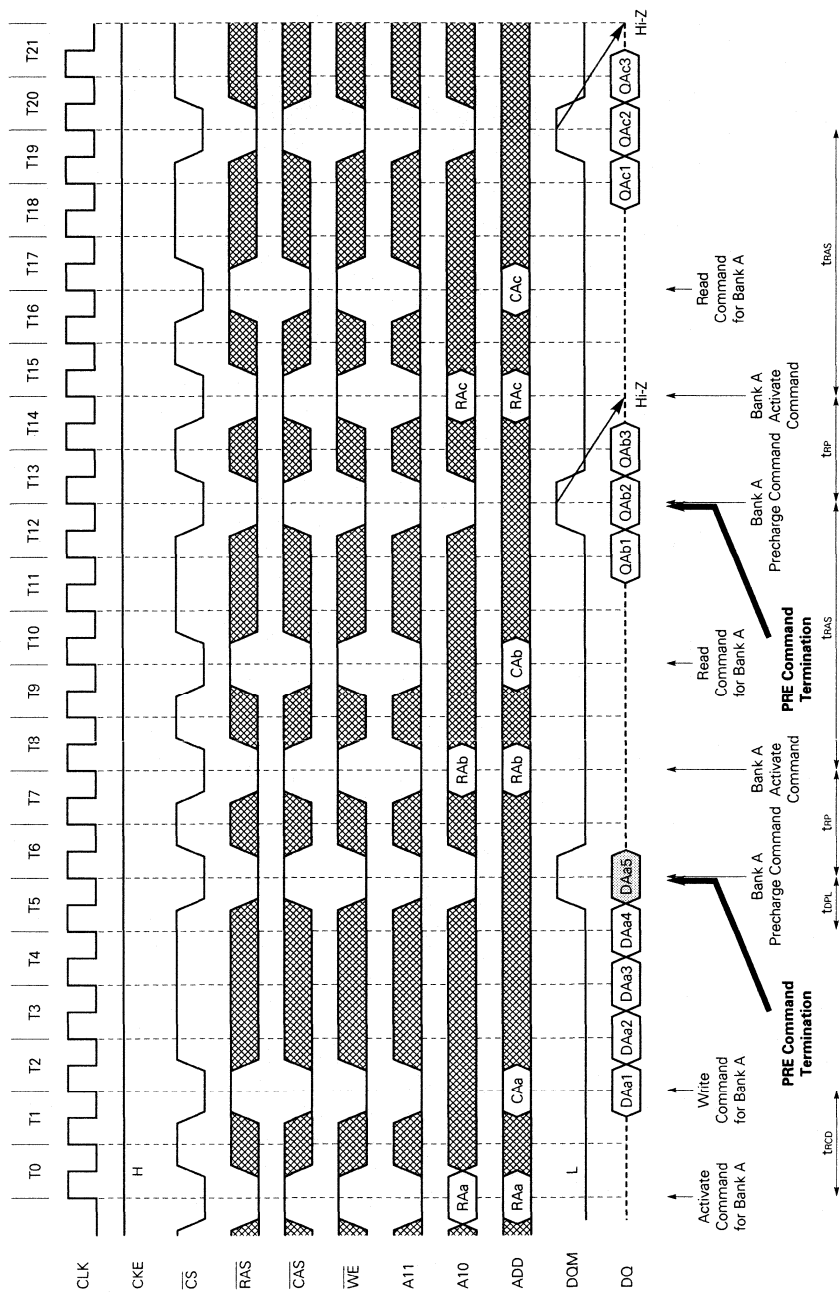
Burst length = Full Page CAS latency = 2



12.28 PRE(Precharge) Termination of Burst (1/3)

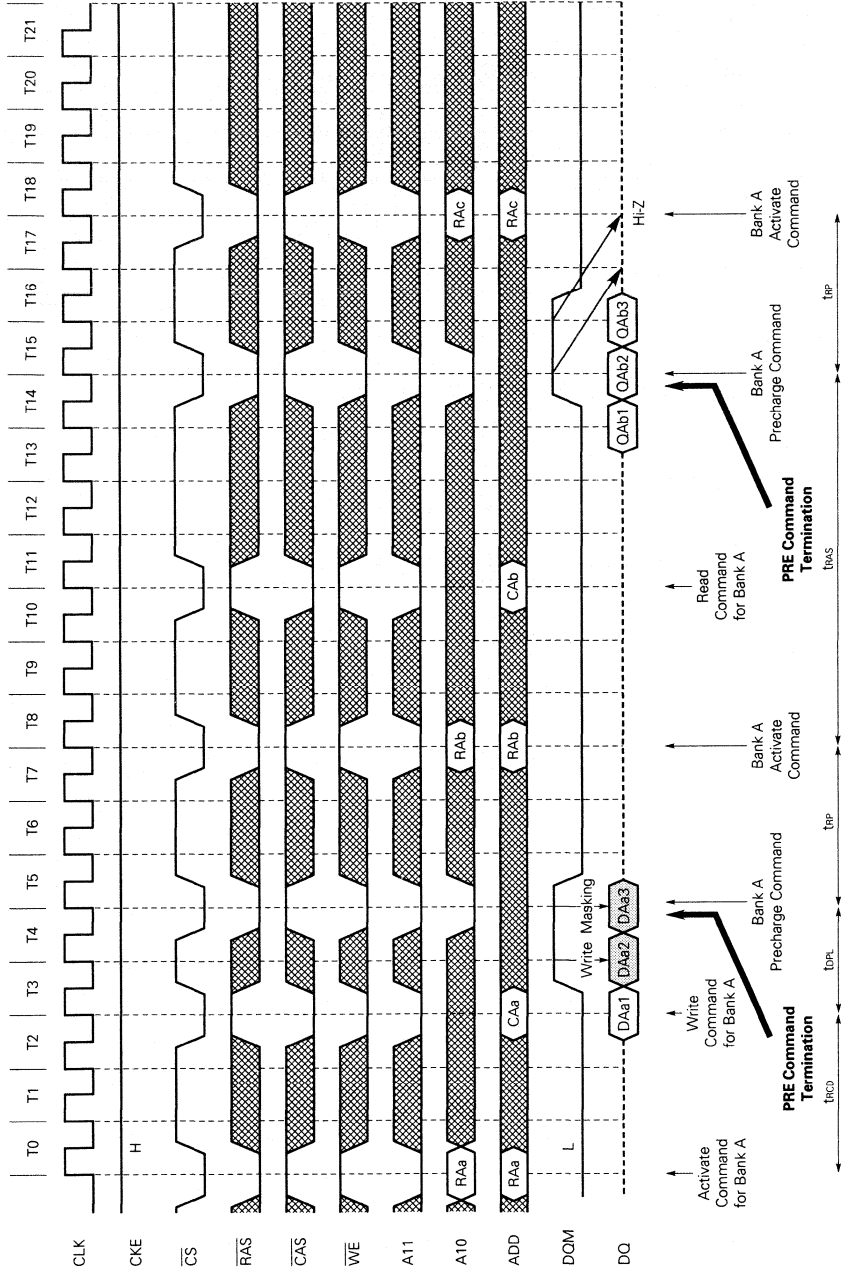
Burst length = 2,4,8,FULL CAS latency = 1



Burst length = 2,4,8,FULL CAS latency = 2

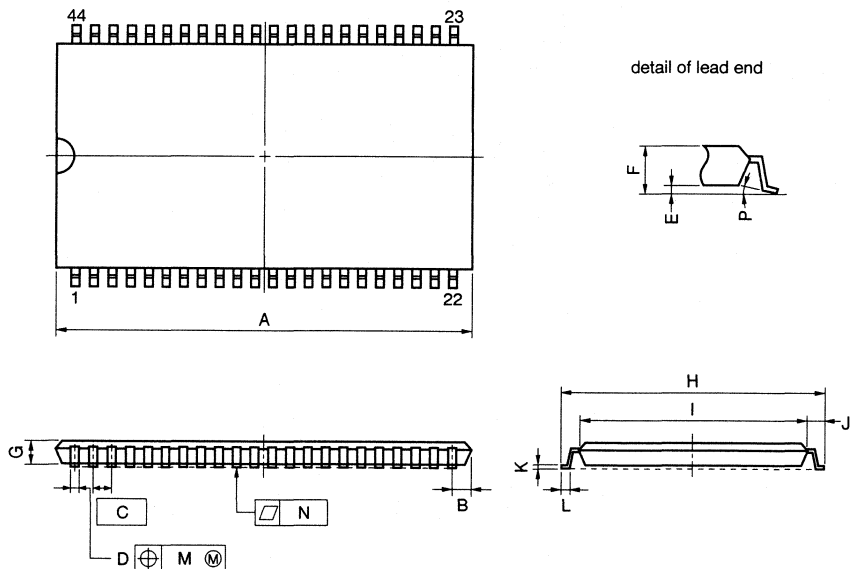
PRE(Precharge)Termination of Burst (3/3)

Burst length = 2.4.8, FULL CAS latency = 3



13. Package Drawings

44PIN PLASTIC TSOP(II) (400 mil)



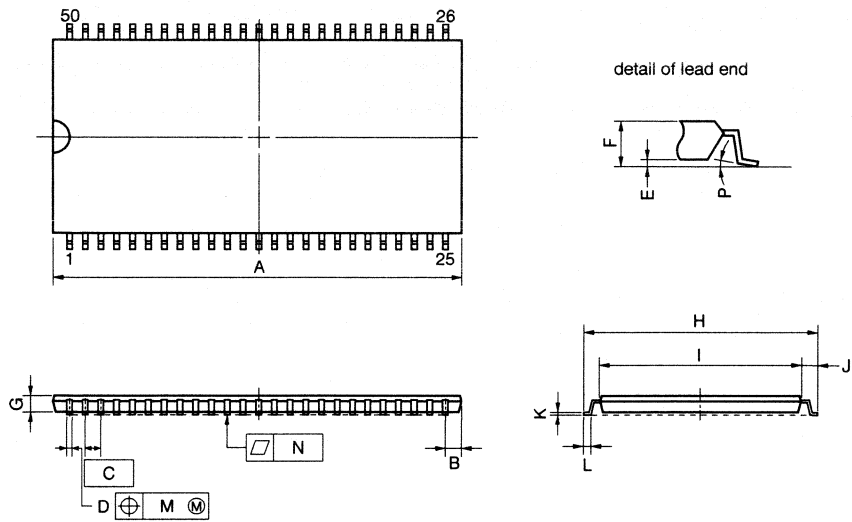
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 ^{+0.08} _{-0.07}	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S44G5-80-7JF3

50PIN PLASTIC TSOP(II) (400 mil)



NOTE
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 ^{+0.08} _{-0.07}	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S50G5-80-7JF3

14. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD4516421, 4516821, 4516161.

Types of Surface Mount Device

μ PD4516421G5-7JF, 4516821G5-7JF: 44-pin Plastic TSOP (II) (400 mil)

μ PD4516161G5-7JF: 50-pin Plastic TSOP (II) (400 mil)

Rambus DRAM



18M bit Rambus DRAM (1Mword x 9bit x 2bank)

Description

The 18-Megabit Rambus™ DRAM (RDRAM™) is an extremely-high-speed CMOS DRAM organized as 2M words by 9 bits and capable of bursting up to 256 bytes of data at 2 ns per byte. The use of Rambus Signaling Logic (RSL) technology makes this 500 MHz transfer rate achievable while using conventional system and board design methodologies. Low latency is attained by using the RDRAM's large internal sense amplifier arrays as high speed caches.

RDRAMs are general purpose high-performance memory devices suitable for use in a broad range of applications including main memory, graphics, video, and any other application where high-performance and low cost are required.

Features

- Rambus Interface:
- 500 MB/sec peak transfer rate per RDRAM
- RSL interface
- Synchronous protocol for fast block-oriented transfers
- Direct connection to Rambus ASICs, MPUs, and Peripherals
- 40 ns from start of read request to first byte, 2 ns per byte thereafter
- Features for graphics include random-access mode, write-per-bit and mask-per-bit operations
- Dual 2KByte sense amplifiers act as caches for low latency accesses
- Control and refresh logic entirely self-contained
- Multiple power-saving modes
- EIAJ standard plastic vertical surface mount package (SVP)
- On-chip registers for flexible addressing and timing
- Low pincount — only 15 active signals

Standardized pinout across multiple generations of RDRAMs

3.3 volt operation

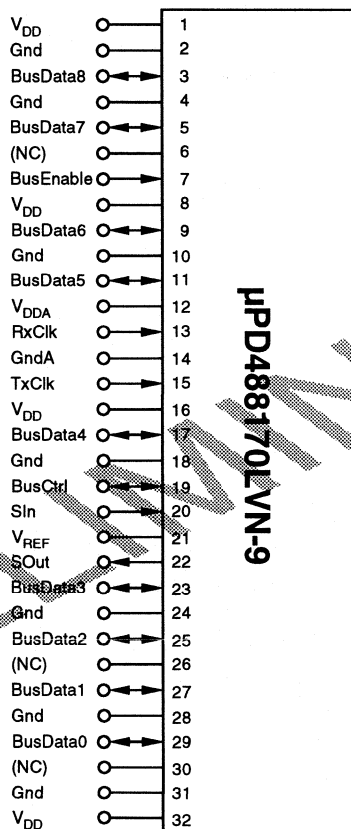
Ordering information

Part Number	Clock Frequency	Operation Voltage	PACKAGE
μPD488170LVN-A50-9	250MHz	3.3±0.15V	32pin plastic SVP
μPD488170LVN-A40-9	200MHz	3.3±0.15V	32pin plastic SVP

Rambus™ and RDRAM™ are trademarks of Rambus Inc.

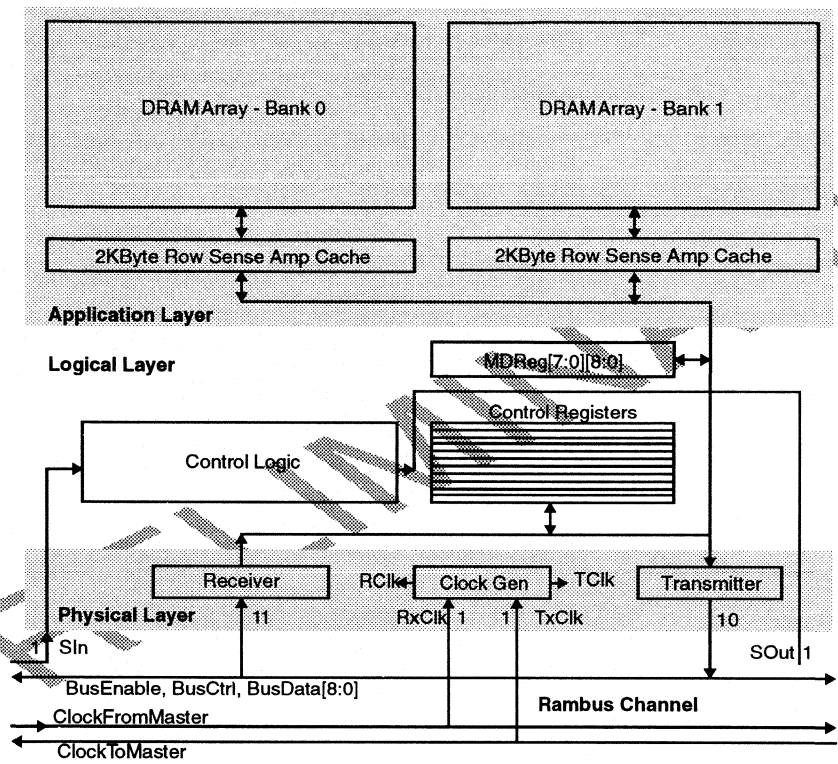
The information in this document is subject to change without notice

Pin configuration



BusData 0 - 8	:	Bus Data (Input/Output)
RxCk	:	Receive Clock (Input)
TxCk	:	Transmit Clock (Input)
Vref	:	Logic Threshold Voltage (Input)
BusCtrl	:	BusCtrl (Input/Output)
BusEnable	:	BusEnable (Input)
Vdd, VddA	:	Power Supply
Gnd, GndA	:	Ground
SIn	:	Serial Input (Input)
SOut	:	Serial Output (Output)

Block Diagram



Pin Function

Signal	I/O	Description
BusData[8-0]	I/O	Signal lines for request, write data, and read data packets. The request packet contains the address, operation codes, and the count of the bytes to be transferred. This is a low-swing, active-low signal referenced to Vref.
RxCk	I	Receive clock. Incoming request and write data packets are aligned to this clock. This is a low-swing, active-low signal referenced to Vref.
TxCk	I	Transmit clock. Outgoing acknowledge and read packets are aligned with this clock. This is a low-swing, active-low signal referenced to Vref.
Vref	I	Logic threshold voltage for low swing signals.
BusCtrl	I/O	Control signal to frame packets, to transmit part of the operation code, and to acknowledge requests. Low-swing, active-low signal referenced to Vref.
BusEnable	I	Control signal to enable the bus. Long assertions of this signal will reset all devices on the Channel. This is a low-swing, active-low signal referenced to Vref.
Vdd, VddA		+3.3V power supply. VddA is a separate analog supply.
Gnd, GndA		Circuit ground. GndA is a separate analog ground.
SI _{in}	I	Initialization daisy chain input. TTL levels. Active high.
SO _{ut}	O	Initialization daisy chain output. TTL levels. Active high.

Rambus System Overview

A typical Rambus memory system has three main elements: the Rambus Channel, the RDRAMs, and a Rambus Interface on a controller. The logical representation of this is shown in the fig.1 below.

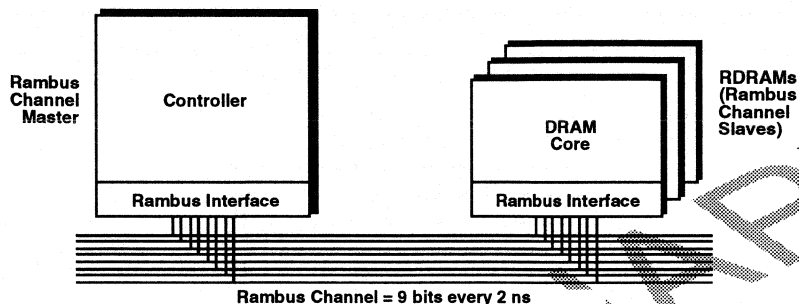


Fig. 1 Logical representation

The Rambus Channel is a synchronous, high-speed, byte-wide bus that is used to directly connect Rambus devices together. Using only 13 high-speed signals, the Channel carries all address, data, and control information to and from devices through the use of a high level block-oriented protocol.

The Rambus Interface is implemented on both master and slave devices. Rambus masters are the only devices capable of generating transaction requests and can be ASIC devices, memory controllers, graphics engines, peripheral chips, or microprocessors. RDRAMs are slave devices and only respond to requests from master devices.

The following fig.2 shows a typical physical implementation of a Rambus system. It includes a controller ASIC that acts as the Channel master and a base set of RDRAMs soldered directly to the board. An RSocket™ is included on the Channel for memory upgrade using RModule™ expansion cards.

(RSocket™ and RModule™ are trademarks of Rambus Inc.)

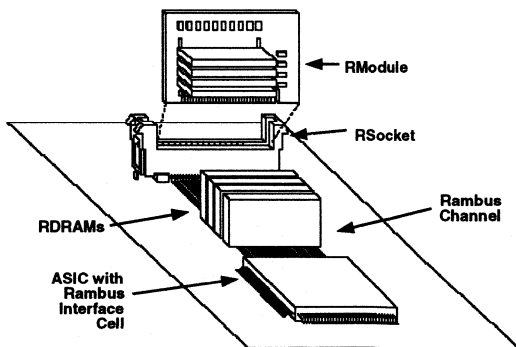


Fig.2 A Rambus System Example

Rambus Signaling Logic

RSL technology is the key to attaining the high data rates available in Rambus systems. By employing high quality transmission lines, current-mode drivers, low capacitive loading, low-voltage signaling, and precise clocking, systems reliably transfer data at 2 nanosecond intervals on a Rambus Channel with signal quality that is superior to TTL or GTL-based interfaces.

All Rambus Interfaces incorporate special logic to convert signals from RSL to CMOS levels for internal use. In addition, these interfaces convert the Channel data rate of one byte every 2 nanoseconds to an internal data rate of 8 bytes every 16 nanoseconds as shown in the fig.3 below. Although the bandwidth remains the same, the use of a wide internal bus eases internal timing requirements for chip designers.

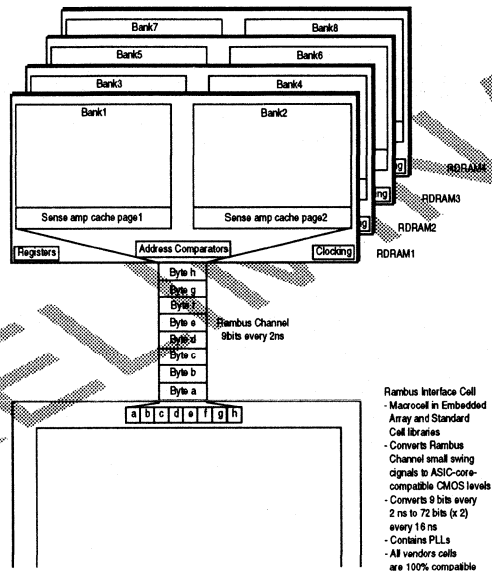


Fig.3 Converting the Channel data rate

Protocol

The high-level transaction protocol used in Rambus systems is built from several types of information packets. These include the request, acknowledge, serial mode, and data packets. A master device initiates a transaction by generating a six byte request packet containing address, control, and byte count information as shown in the fig.4 below.

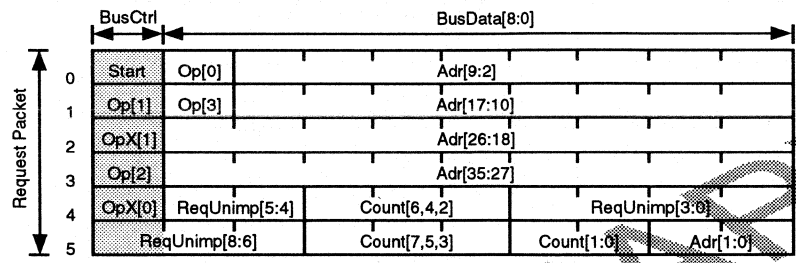


Fig.4 Request Packet Format

All slave devices constantly monitor the Channel for a request to access their assigned memory range. The device matching the address range requested then drives an acknowledge packet back to the master. The RDRAM also drives a data packet back to the master in the case of a read, or accepts a data packet from the master in the case of a write. The figure below shows example 16 byte read and write transactions. The actual timing from the end of a request packet to data and acknowledge packets is adjustable through RDRAM register settings.

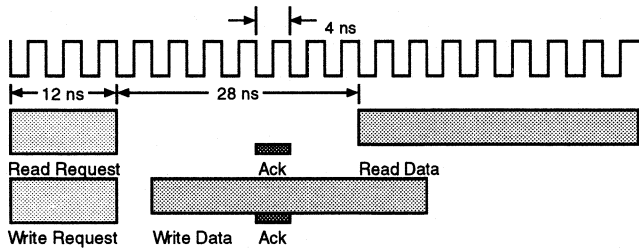


Fig.5 Sample 16-Byte Read and Write Transactions

RDRAM Commands

The request packet generated by the master device contains an Op and OpX field used to specify the type of operation to be performed on the RDRAM being accessed. The following table describes the types of operations supported in the 16-Megabit RDRAM.

Table 1 Types of operations

Op[3:0]	OpX[1:0]	Name	Description
0000	00	Rseq	Read sequential data from memory space.
0000	01	Rnsq	Read non-sequential data from memory space.
0100	00	WseqNpb	Write sequential data to memory space with no per-bit mask application.
0100	01	WseqDpb	Write sequential data to memory space with data-per-bit masking. Static bit masks are supplied by the MDReg while write data is supplied in the data packets.
0100	10	WseqBpb	Write sequential data to memory space with mask-per-bit masking. Both write data and dynamic bit masks are supplied in the data packets.
0100	11	WseqMpb	Write sequential data to memory space with mask-per-bit masking. Static write data is supplied by the MDReg while dynamic bit masks are supplied in the data packets.
0110	00	Rreg	Read data from register space.
0111	00	Wreg	Write data to register space.
1000	00	WnsqNpb	Write non-sequential data to memory space with no per-bit mask application.
1000	01	WnsqDpb	Write non-sequential data to memory space with data-per-bit masking. Static bit masks are supplied by the MDReg while write data is supplied in the data packets.
1000	10	WnsqBpb	Write non-sequential data to memory space with mask-per-bit masking. Both write data and dynamic bit masks are supplied in the data packets.
1000	11	WnsqMpb	Write non-sequential data to memory space with mask-per-bit masking. Static write data is supplied by the MDReg while dynamic bit masks are supplied in the data packets.
1100	00	WbnsNpb	Write non-sequential data to memory space with byte masking and no per-bit mask application. Both byte masks and write data are supplied in the data packets.
1100	01	WbnsDpb	Write non-sequential data to memory space with byte masking and data-per-bit masking. Static bit masks are supplied by the MDReg while byte masks and write data are supplied in the data packets.
1100	11	WbnsMpb	Write non-sequential data to memory space with byte masking and mask-per-bit masking. Static write data is supplied by the MDReg while byte masks and dynamic bit masks are supplied in the data packets.
1111		WregB	Broadcast write to register space of all responding devices with no acknowledge permitted.

Random Access Mode

Non-contiguous blocks of memory can be accessed through the use of the read and write non-sequential operations. With these commands, multiple eight-byte blocks (octbytes) of data within a cache line can be accessed in a non-sequential fashion. To do this, the master device sends a request packet specifying a non-sequential operation along with the address of the first octbyte to be accessed. The master device also generates a serial address packet on the BusEnable signal that specifies the address of the next octbyte. Successive serial address packets continue to specify new addresses within the cache line while data is continuously transferred until the access is complete.

Bit Masking

Three forms of bit masking are available for write operations. These operations are referred to as data-per-bit (Dpb), mask-per-bit (Mpb), and both-per-bit (Bpb) masking. An eight-byte register within the RDRAM (MDReg) is used to hold either mask or data information for these operations.

With the Dpb operation, the MDReg is used to hold a static mask that is applied to all octbytes of data written to the RDRAM core. With the Mpb operation, the MDReg is used to hold an octbyte of static data that is masked by dynamic bit masks supplied in the data packets before being written to the RDRAM core.

The Bpb operation requires data packets to alternate between mask and data octbytes. The even data packets (starting with data packet 0) carry bit masking information which is placed in the MDReg while the odd data packets carry the data to be masked by the latest contents on the MDReg. This type of operation is also used to set the MDReg for later use in Dpb and Mpb operations.

Byte Masking

This device supports non-sequential byte masked writes that may include Dpb or Mpb bit masking as an option. Bpb bit masking is not supported in conjunction with byte masking.

In this operation, the first data packet, and every ninth thereafter, contain byte masking information that is applied to the eight data packets that follow. This means data packet 0, 9, 18, and 27 are not written to memory, but are instead used as byte masks for the eight octbytes of data that follow.

RDRAM Overview

Conceptually, the RDRAM can be divided into three sections referred to as the physical, logical and application layers. These are shown in the fig.6 below.

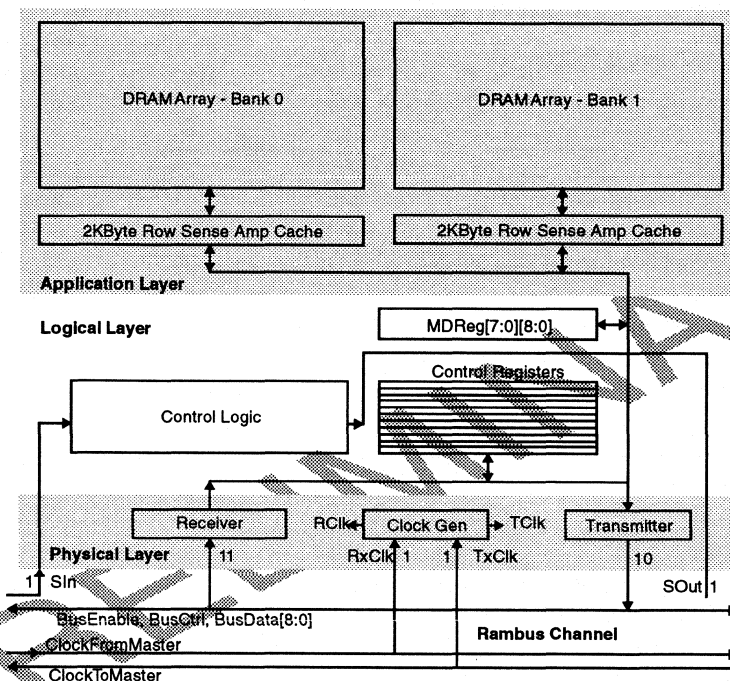


Fig. 6 Block diagram

The physical layer consists of a clock generator, a receiver, and a transmitter. The clock generator uses the external clock signals RxClk and TxClk (tapped off the Channel traces ClockFromMaster and ClockToMaster) and creates the internal signals RClk and TClk. These are used by the receiver and transmitter, respectively, to transfer a bit every 2 nanoseconds on each wire between the RDRAM and the master device. The receiver and transmitter blocks also contain multiplexing and storage hardware to permit the internal RDRAM data paths to operate at the slower clock rate (but equivalent bandwidth) of eight bytes transferred every 16 nanoseconds.

The logical layer consists of control logic and configuration registers. The registers are read and written using special register space commands and control the following aspects of RDRAM operation:

Table 2 Special register

Register	Description
DeviceType	Readable register that defines the type and size of the device along with part version information.
DeviceId	Used to define the base address for the RDRAM.
Delay	Used to specify programmable CAS-type delay values.
Mode	Used to enable device, control refresh mode, and adjust current control settings.
RefInterval	Used to define the refresh interval for self-refresh.
RefRow	Contains the current refresh row and bank information.
RasInterval	Used to define RAS timing parameters.
MinInterval	Readable register defining minimum timings for Delay register parameters.
AddressSelect	Used to define address bit swapping to alter RDRAM address mapping.
DeviceManufacture	Readable register containing a manufacturer code and a manufacturer specific part type code.
Row	Readable register containing the row numbers for the currently sensed rows in each bank.
MDReg	Used in performing write-per-bit and mask-per-bit operations.

The application layer consists of a standard DRAM memory core and row sense amplifier caches.

Caches

Each RDRAM is broken down into two independent banks of memory. Each of these banks has a 2KByte cache line associated with it that is built out of large sense amplifier arrays. These caches work by holding the last accessed row of their associated bank in the sense amplifiers allowing further accesses to the same row of memory to result in cache hits. With the row already stored in the cache, data can be accessed with very low latency. Each RDRAM added to a system adds two cache lines to the memory system helping increase cache hit rates.

A cache miss results when a row is accessed that is not currently stored in one of the cache lines. When this happens, the requesting master is sent a NACK Acknowledge packet indicating the requested row is not yet available. The RDRAM then loads the requested row into the cache line and waits for the master to submit a retry of the previous request. The figure below shows an example of a read miss followed by a read hit for a 32 byte memory read operation.

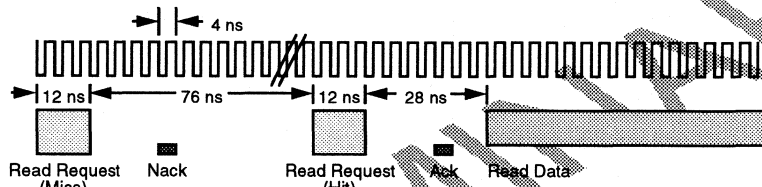


Fig. 7 Sample 32-Byte Read Miss and Read Hit Transactions

Address Mapping

Address mapping hardware is provided to increase cache hit rates by allowing system designers to easily perform n-way RDRAM interleaving. In a non-interleaved memory system, contiguous blocks of addresses follow each other in sequence in one RDRAM which is then followed by the next RDRAM. By using address mapping, contiguous blocks of addresses are split across several RDRAMs, and therefore across several cache lines. In a typical system containing, for example, eight RDRAMs, miss rates could be expected to be as low as 5%. Address mapping is easily adjusted by writing a control register in each RDRAM.

Automatic Refresh

RDRAMs have been designed with built-in self-refresh circuitry to ease system design requirements. Registers are provided to enable and adjust self-refresh operation. If automatic refresh is disabled, refresh must be accomplished through standard memory reads and writes. When automatic refresh is enabled, refresh operations are done in bursts refreshing 4 rows of an individual bank at a time with banks being alternated each refresh cycle. The entire RDRAM is refreshed every 16 milliseconds with 128 burst refresh cycles.

Standby Mode

The RDRAM's normal state while not being accessed is standby mode. While in this low power state, each RDRAM monitors the BusEnable signal for a serial mode packet while ignoring most other activity on the remaining Channel signals. The serial mode packet is used by a master device to bring all RDRAMs temporarily out of standby and into active mode so they can respond to a request packet. Once a request packet is acknowledged, all RDRAMs return to standby mode with the exception of the one responding to the request. This device will return to standby mode once the read or write operation is completed.

Unlike conventional DRAM memory systems where each device in an entire bank of memory must be kept active and consuming power through an entire access, Rambus memory systems allow only one active device while all others remain in a low power state.

PowerDown Mode

Power may be greatly reduced by using the powerdown mode. This mode is manually entered by setting a register bit in the RDRAM which causes the device to write back and precharge both cache lines, disable the internal clock generator, and disable most DC current sources. The BusEnable receiver is kept active to detect serial mode packets used to exit powerdown mode. Once in this mode, the only significant power consumption is due to refresh.

Since the RDRAM's internal clocks are disabled while in powerdown mode, automatic refresh is not available. Because of this, refresh must be maintained manually by the master device. This is done by supplying a low frequency square wave on the SIn TTL signal. This propagates through each RDRAM and is used to initiate asynchronous refresh operations in each device.

Each RDRAM may be placed in either low or high threshold powerdown mode. This refers to the number of serial mode packets required to wake up the RDRAM. Low threshold requires relatively few serial mode packets while high threshold requires a larger number. Actual power dissipation is identical in both modes.

An example of how these mode can be used might be a portable application where a sleep mode is implemented by placing a majority of the RDRAMs in high threshold powerdown while one or two containing the frame buffer are placed in low threshold powerdown. This would permit screen refresh to take place without powering up the entire memory system.

Transaction Concurrency

Concurrent transactions can be used to optimize RDRAM utilization in high performance applications by taking advantage of available Channel bandwidth during cache miss latency periods. When a miss in one RDRAM takes place, that device will be busy loading a new row into one of its cache lines. Other than that, the Channel and all other RDRAMs will still be available for use. Instead of waiting for the first RDRAM to finish loading its cache, a transaction to another RDRAM can be initiated.

This can be used in various ways. In systems where memory accesses can be queued, a transaction can take place for any pending access residing in a different RDRAM. When that transaction is complete, the first transaction can be retried.

Pretouching can be used in systems where memory accesses are predictable, such as video applications. This is done when an application is finished with a particular RDRAM and about to access a different one. If the next access to the original RDRAM is known in advance, a dummy transaction can be first generated to cause a row miss and prepare it for its next access. Transactions to other devices can then take place while a cache fill is taking place. When the original device is next accessed, the required row of data will already be loaded in the cache line and a cache hit will take place.

Absolute Maximum Ratings

The following table represents stress ratings only, and functional operation at the maximums is not guaranteed. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although devices contain protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL pin with respect to Gnd	- 0.5	$V_{DD}+0.5$	V
$V_{I,TTL,ABS}$	Voltage applied to any TTL pin with respect to Gnd	- 0.5	$V_{DD}+0.5$	V
$V_{DD,ABS}$	Voltage on V_{DD} with respect to Gnd	- 0.5	$V_{DD,MAX}+1.0$	V
$T_{J,ABS}$	Junction temperature under bias	- 55	125	°C
T_{STORE}	Storage temperature	- 55	125	°C

Thermal Parameters

Symbol	Parameter and Conditions	Min	Max	Unit
T_J	Junction operating temperature	0	100	°C
Θ_{JC}	Junction-to-Case thermal resistance		TBD	°C/Watt

Capacitance

Symbol	Parameter and Conditions	Min	Max	Unit
C_i	Low-swing input parasitic capacitance		2	pF
$C_{i,TTL}$	TTL input parasitic capacitance		8	pF

Power Consumption

Mode	Description	Min	Max	Unit
Powerdown	Device shut down		TBD	mW
Standby	Device inactive		220	mW
Active	Device evaluating request packet		550	mW
Read	Data being transferred from device		760	mW
Write	Data being transferred to device		860	mW

Recommended Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
V_{DD}, V_{DDA}	Supply voltage — 3.3-volt version	3.15	3.45	V
V_{REF}	Reference voltage	1.9	2.4	V
V_L	Input low voltage	$V_{REF} - 0.8$	$V_{REF} - 0.2$	V
V_H	Input high voltage	$V_{REF} + 0.2$	$V_{REF} + 0.8$	V
$V_{L,TTL}$	TTL input low voltage	-0.5	0.8	V
$V_{H,TTL}$	TTL input high voltage	2.0	$V_{DD} + 0.5$	V

Electrical Characteristics

Symbol	Parameter and Conditions	Min	Max	Unit
I_{REF}	V_{REF} current @ V_{REF}, MAX	-10	10	μA
I_{OH}	Output high current @ ($0 \leq V_{OUT} \leq V_{DD}$)	-10	10	μA
I_{OL}	Output low current @ $V_{OUT} = 1.6V$		35	mA
ΔI_{OL}	Error in programmed output low current (from unit to unit)	-1.1	1.1	mA
$I_{I,TTL}$	TTL input leakage current @ ($0 \leq V_{I,TTL} \leq V_{DD}$)	-10.0	10.0	μA
$V_{OL,TTL}$	TTL output voltage @ $I_{OL,TTL} = 1.0mA$	0.0	0.4	V
$V_{OH,TTL}$	TTL output high voltage @ $I_{OH,TTL} = -0.25mA$	2.4	V_{DD}	V

Recommended Timing Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
t_{CR}, t_{CF}	TxCk and RxClk input rise and fall times	0.3	0.7	ns
t_{CYCLE}	TxCk and RxClk cycle times	4	10	ns
t_{TCK}	Transport time per bit per pin (this timing interval is synthesized by the RDRAM's internal clock generator)	0.5 (2ns @ $t_{CYCLE} = 4ns$)	0.5 (2ns @ $t_{CYCLE} = 4ns$)	t_{CYCLE}
t_{CH}, t_{CL}	TxCk and RxClk high and low times	45%	55%	t_{CYCLE}
t_{TR}	TxCk-RxCk differential	0	$t_{CYCLE} - 0.6$	ns
t_{DR}, t_{DF}	Data/Control input rise and fall times	0.3	0.7	ns
t_{OR}, t_{OF}	Data/Control output rise and fall times	0.4	0.6	ns
t_S	Data/Control-to-RxCk setup time	0.3		ns
t_H	RxCk-to-Data/Control hold time	0.3		ns
t_{REF}	Refresh interval		32	ms
$t_{LOCK,ACTIVE}$	RDRAM internal clock generator lock time in active mode		500(1ms @ $t_{CYCLE} = 4ns$)	t_{CYCLE}
$t_{LOCK,STANDBY}$	RDRAM internal clock generator lock time in standby mode		500(1ms @ $t_{CYCLE} = 4ns$)	t_{CYCLE}

Timing Characteristics

Symbol	Parameter and Conditions	Min	Max	Unit
t_{PD}	Stn-to- $\overline{S}$ Out propagation delay @ $C_{LOAD,TTL} = 40pF$		25	ns
t_D	TClk-to-Data/Control output time	$t_{CYCLE}/4 - 0.3$	$t_{CYCLE}/4 + 0.3$	ns

Rambus Channel Timing

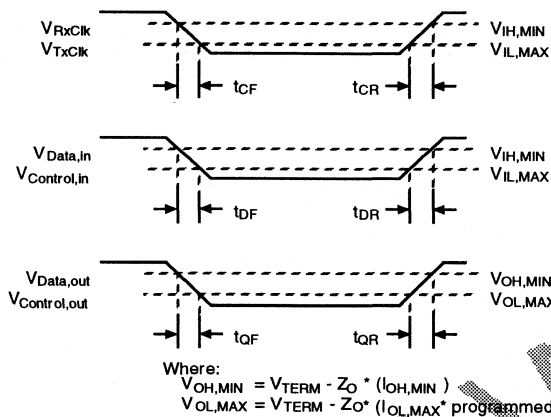
The next table shows important timings on the Rambus Channel for common operations. Please refer to the RDRAM Reference Manual and 16Mb RDRAM Specification for all possible interactions that could occur on the Rambus Channel. All timings are from the point of view of the Channel master, and thus have the bus overhead delay of 4ns per bus transversal included where appropriate

Symbol	Parameter and Conditions	Min	Max	Unit
t_{CYCLE}	TxCk and RxClk cycle times	4	10	ns
t_{RESPONSE}	Start of request packet to start of acknowledge packet.	6 ⁽¹⁾	9 ⁽¹⁾	t_{CYCLE}
t_{READHIT}	Start of request packet to start of read data packet for row hit (Okay).	10 ⁽¹⁾	41 ⁽¹⁾	t_{CYCLE}
t_{WRITEHIT}	Start of request packet to start of write data packet for row hit (Okay).	4 ⁽¹⁾	35 ⁽¹⁾	t_{CYCLE}
$t_{\text{RETRYSENSED}}$ CLEAN (no restore)	Start of request packet for row miss (Nack) to start of request packet for row hit (Okay). The previous row is unmodified.	22 ⁽²⁾		t_{CYCLE}
$t_{\text{RETRYSENSED}}$ DIRTY (restore)	Start of request packet for row miss (Nack) to start of request packet for row hit (Okay). The previous row is modified.	29 ⁽²⁾		t_{CYCLE}
$t_{\text{READBURST32}}$	Start of request packet to end of 32 byte read data packet for row hit (Okay).	26 ⁽³⁾		t_{CYCLE}
$t_{\text{READBURST256}}$	Start of request packet to end of 256 byte read data packet for row hit (Okay).	138 ⁽³⁾		t_{CYCLE}
$t_{\text{WRITEBURST32}}$	Start of request packet to end of 32 byte write data packet for row hit (Okay).	20 ⁽⁴⁾		t_{CYCLE}
$t_{\text{WRITEBURST256}}$	Start of request packet to end of 256 byte write data packet for row hit (Okay).	132 ⁽⁴⁾		t_{CYCLE}

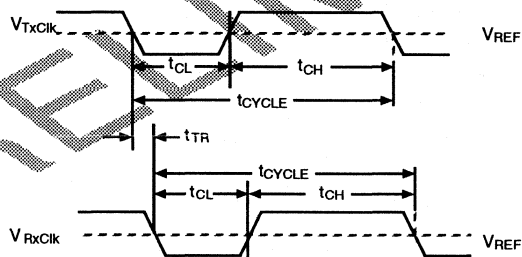
Note

- (1) Programmable
- (2) Minimum at $t_{\text{CYCLE}}^{\text{MIN}}$. Delay programmable to give equivalent timings at longer t_{CYCLE} .
- (3) Calculated with $t_{\text{READHIT}}^{\text{MIN}}$
- (4) Calculated with $t_{\text{WRITEHIT}}^{\text{MIN}}$

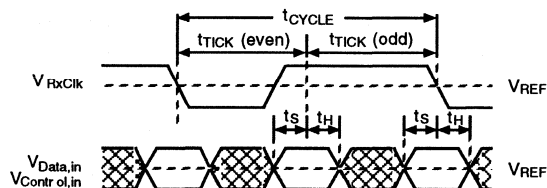
Rise/Fall Timing



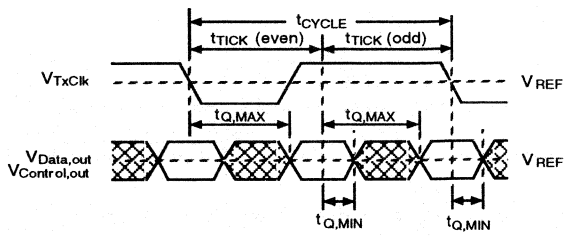
Clock Timing



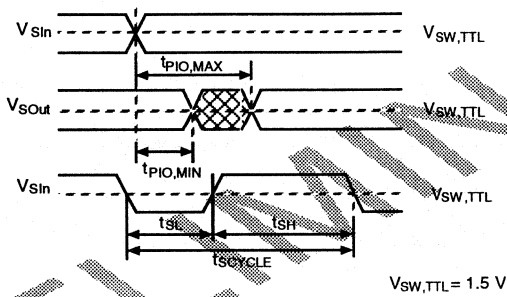
Receive Data Timing



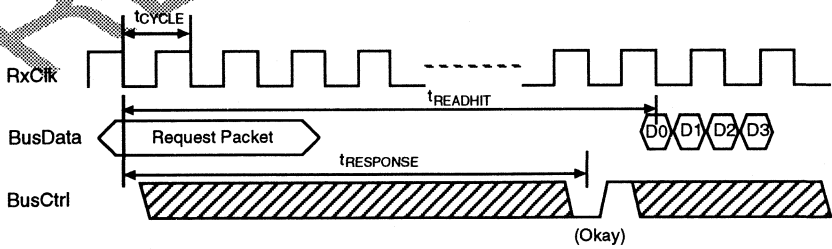
Transmit Data Timing



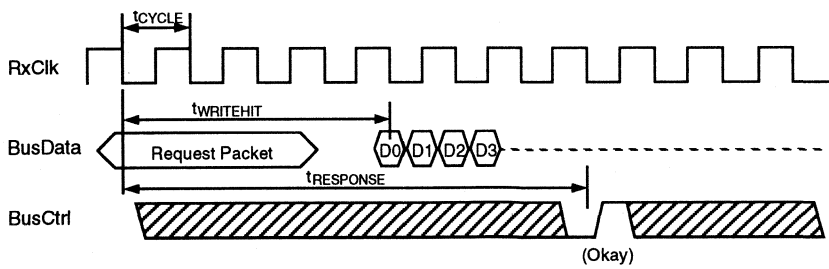
Serial Configuration Pin Timing



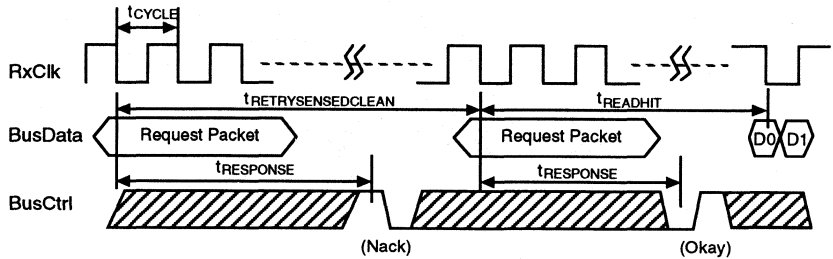
Read Hit Timing Diagram



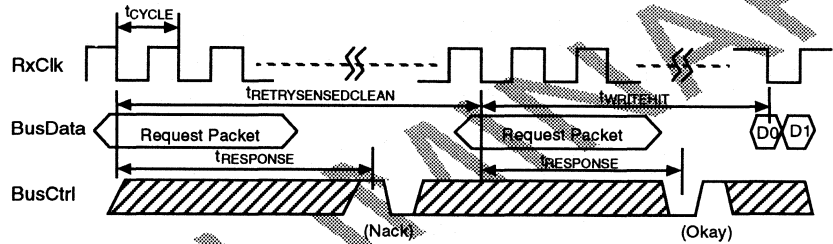
Write Hit Timing Diagram



Read Miss Timing Diagram

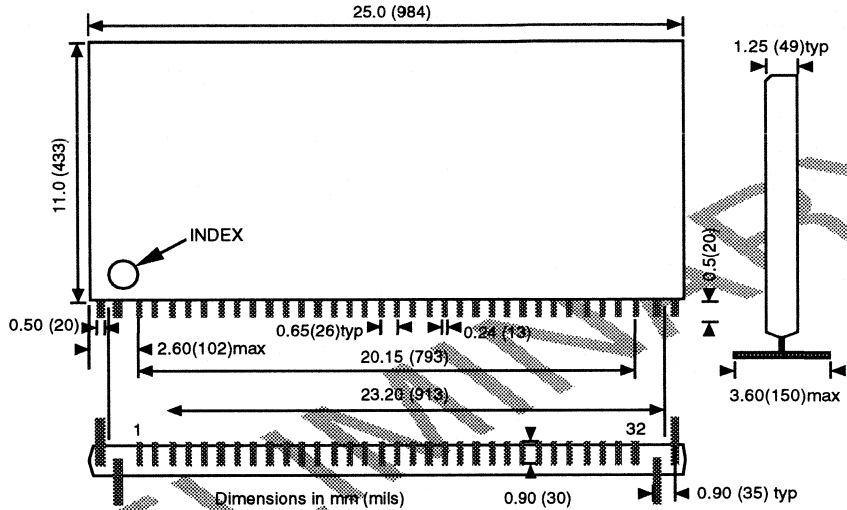


Write Miss Timing Diagram



Package Drawing

The RDRAM package is a vertical surface mount package (SVP) which is an EIAJ standard (#ED-7424). Dimensions are shown in the figure below.



DRAM Module



MOS INTEGRATED CIRCUIT

MC-428000AA40 SERIES

8 M-WORD BY 40-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-428000AA40 is a 8 388 608 words by 40 bits dynamic RAM module on which 20 pieces of 16 M bits CMOS Dynamic RAM (μ PD4217400) are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8 388 608 words by 40 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-428000AA40-60	60 ns	110 ns	5 565 mW	105 mW (CMOS level input)
MC-428000AA40-70	70 ns	130 ns	5 040 mW	
MC-428000AA40-80	80 ns	150 ns	4 515 mW	

- Fast page mode
- 2 048 refresh cycles / 32 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- 40-bit simultaneous switching
- Output buffers control : $\overline{\text{OE}}$ pin
- Single +5.0 V $\pm 5\%$ power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.

The mark ★ shows revised points.

★ Ordering Information

Part number	Access time (MAX.)	Package	Mounted device
MC-428000AA40B-60	60 ns	72-pin Single In-line Memory Module (Socket type) Edge connector : Solder coating (HAL)	20 pieces of μ PD4217400LA (300 mil SOJ) [Double side]
MC-428000AA40B-70	70 ns		
MC-428000AA40B-80	80 ns		
MC-428000AA40F-60	60 ns	72-pin Single In-line Memory Module (Socket type) Edge connector : Gold plating	
MC-428000AA40F-70	70 ns		
MC-428000AA40F-80	80 ns		

Quality Grade

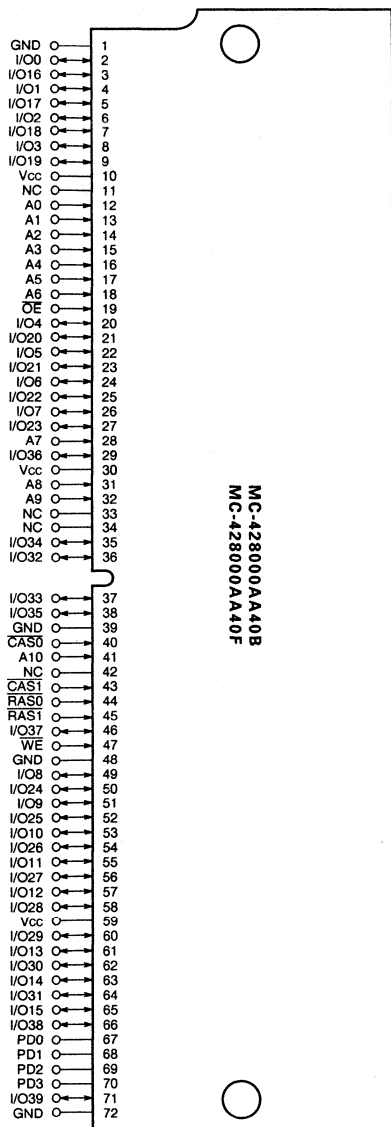
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration



72-pin Single In-line Memory Module Socket Type (Edge connector: Solder Coating, Gold Plating)

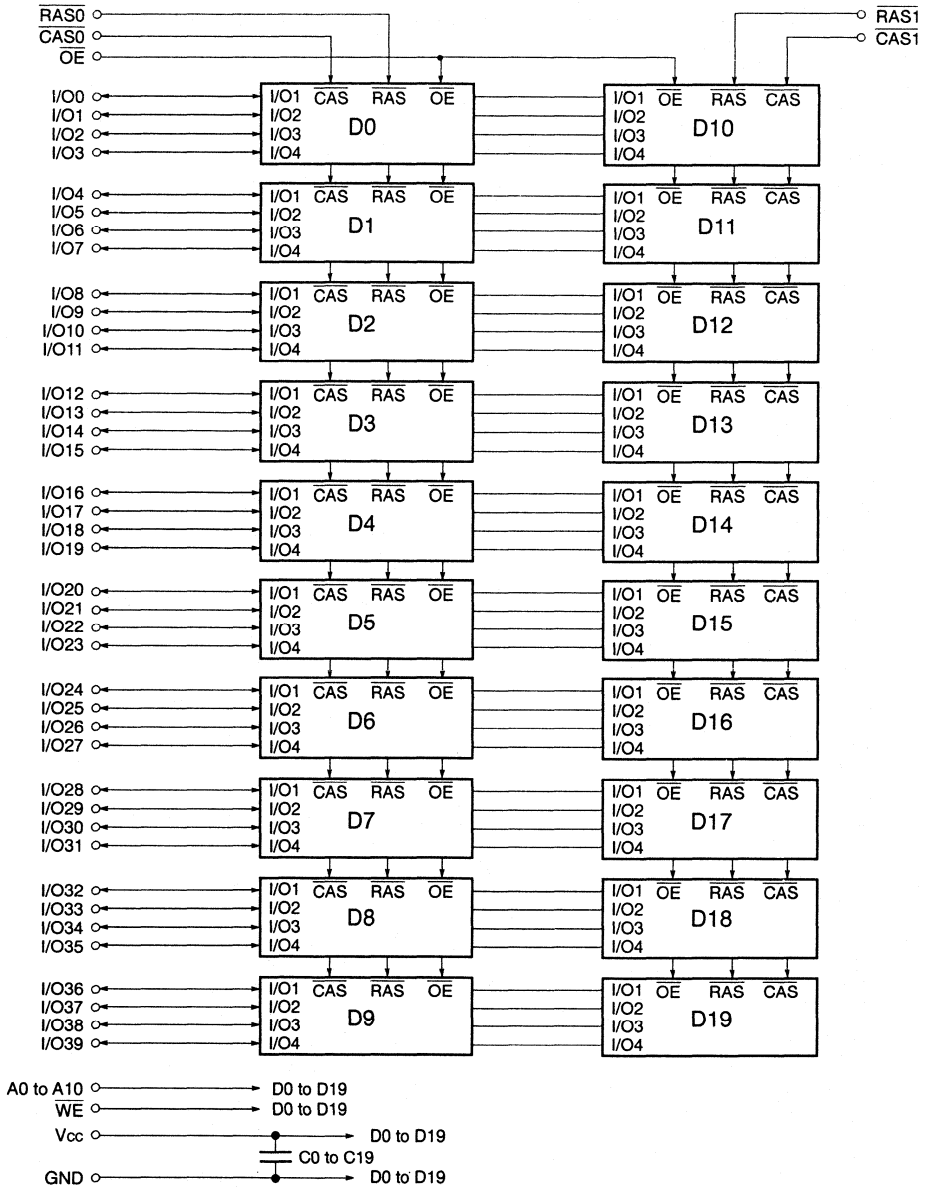


- A0 to A10 : Address Inputs
 I/O0 to I/O39 : Data Inputs/Outputs
 $\overline{\text{CAS0}}, \overline{\text{CAS1}}$: Column Address Strobe
 $\overline{\text{RAS0}}, \overline{\text{RAS1}}$: Row Address Strobe
 $\overline{\text{WE}}$: Write Enable
 $\overline{\text{OE}}$: Output Enable
 Vcc : Power Supply
 GND : Ground
 NC : No Connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

Block Diagram



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		20	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A10			160	pF
	C_{I2}	$\overline{WE}$, $\overline{OE}$			160	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS1}$			85	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS1}$			85	
Data Input/Output capacitance	$C_{I/O}$	I/O0 to I/O39			30	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	RAS, CAS Cycling	t _{RAC} = 60 ns	1 060	mA	3,4,7
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 70 ns	960		
		I _O = 0 mA	t _{RAC} = 80 ns	860		
Standby current	I _{CC2}	RAS, CAS ≥ V _{IH} (MIN.)	I _O = 0 mA	40	mA	
		RAS, CAS ≥ V _{CC} - 0.2 V	I _O = 0 mA	20		
RAS only refresh current	I _{CC3}	RAS Cycling	t _{RAC} = 60 ns	1 060	mA	3,4,5,7
		CAS ≥ V _{IH} (MIN.)	t _{RAC} = 70 ns	960		
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 80 ns	860		
Operating current (Fast page mode)	I _{CC4}	CAS Cycling	t _{RAC} = 60 ns	760	mA	3,4,6
		RAS ≤ V _{IL} (MAX.)	t _{RAC} = 70 ns	660		
		t _{PC} = t _{PC} (MIN.)	t _{RAC} = 80 ns	560		
CAS before RAS refresh current	I _{CC5}	RAS Cycling	t _{RAC} = 60 ns	1 060	mA	3,4
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 70 ns	960		
		I _O = 0 mA	t _{RAC} = 80 ns	860		
Input leakage current	I _I (L)	V _I = 0 to 5.5 V all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _O (L)	V _O = 0 to 5.5 V Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage	V _{OH}	I _O = -5.0 mA	2.4		V	
Low level output voltage	V _{OL}	I _O = +4.2 mA		0.4	V	

AC Characteristics

(Recommended Operating Conditions unless otherwise noted) Notes 8, 9

(1/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t _{RWC}	160		180		205		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	85		90		105		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		15		18		20	ns	10, 11
Access Time from Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEa}		15		18		20	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	15		15		20		ns	
Output Buffer Turn-off Delay from $\overline{\text{OE}}$	t _{OEZ}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0		0		0		ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10 000	70	10 000	80	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15		18		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10 000	18	10 000	20	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	

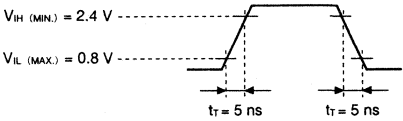
(2/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
$\overline{\text{WE}}$ Pulse Width	t _{WP}	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	40		43		50		ns	17
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	85		95		110		ns	17
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	58		65		70		ns	17
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	55		60		70		ns	17
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20		20		20		ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15		15		15		ns	
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	5		5		5		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10		10		10		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		32		32		32	ms	

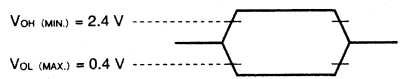
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1 , Icc3 , Icc4 and Icc5 depend on cycle rates (trc and tpc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
- 6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- 7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq \text{Vil}$ (MAX.) and $\overline{\text{CAS}} \geq \text{Vil}$ (MIN.).
- 8. AC measurements assume $\text{tr} = 5 \text{ ns}$.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



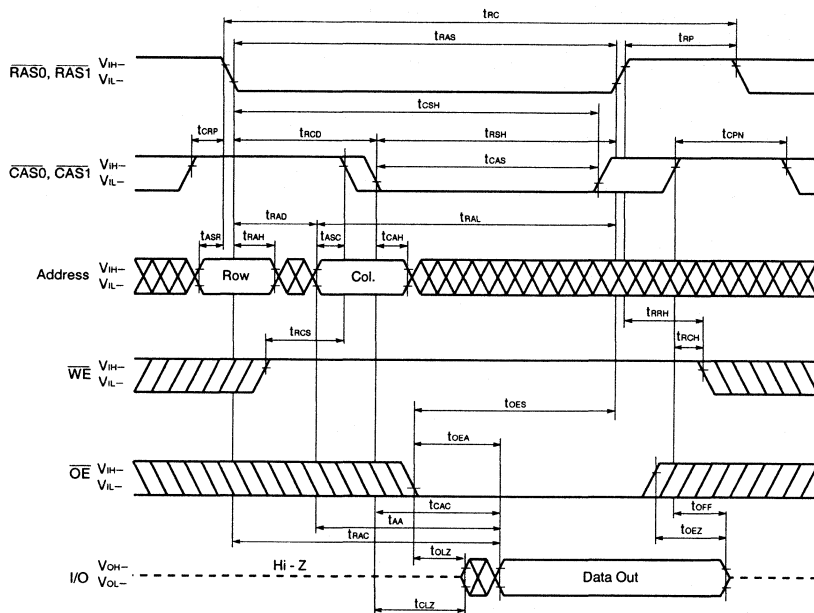
10. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\text{trAD} > \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$	$\text{trAD} + \text{tAA} (\text{MAX.})$
$\text{trCD} > \text{trCD} (\text{MAX.})$	$\text{tCAC} (\text{MAX.})$	$\text{trCD} + \text{tCAC} (\text{MAX.})$

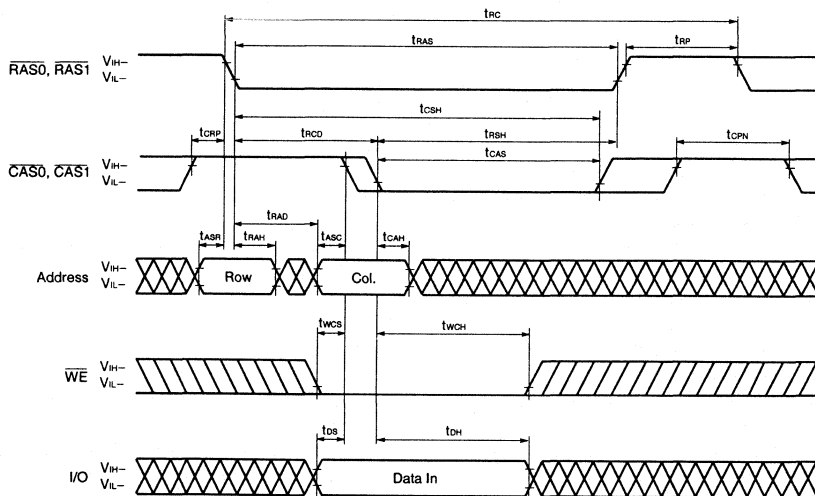
$\text{trAD} (\text{MAX.})$ and $\text{trCD} (\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD} (\text{MAX.})$ and $\text{trCD} \geq \text{trCD} (\text{MAX.})$ will not cause any operation problems.

- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. $\text{toFF} (\text{MAX.})$ and $\text{toEZ} (\text{MAX.})$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
- 13. $\text{tCRP} (\text{MIN.})$ requirement should be applied to $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycles.
- 14. Either $\text{trCH} (\text{MIN.})$ or $\text{trRH} (\text{MIN.})$ should be met in read cycles.
- 15. $\text{tWP} (\text{MIN.})$ is applied to late write cycles or read modify write cycles. In early write cycles, $\text{twCH} (\text{MIN.})$ should be met.
- 16. $\text{tDS} (\text{MIN.})$ and $\text{tDH} (\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
- 17. If $\text{twCS} \geq \text{twCS} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{trWD} \geq \text{trWD} (\text{MIN.})$, $\text{tcWD} \geq \text{tcWD} (\text{MIN.})$, $\text{tAWD} \geq \text{tAWD} (\text{MIN.})$ and $\text{tcpWD} \geq \text{tcpWD} (\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

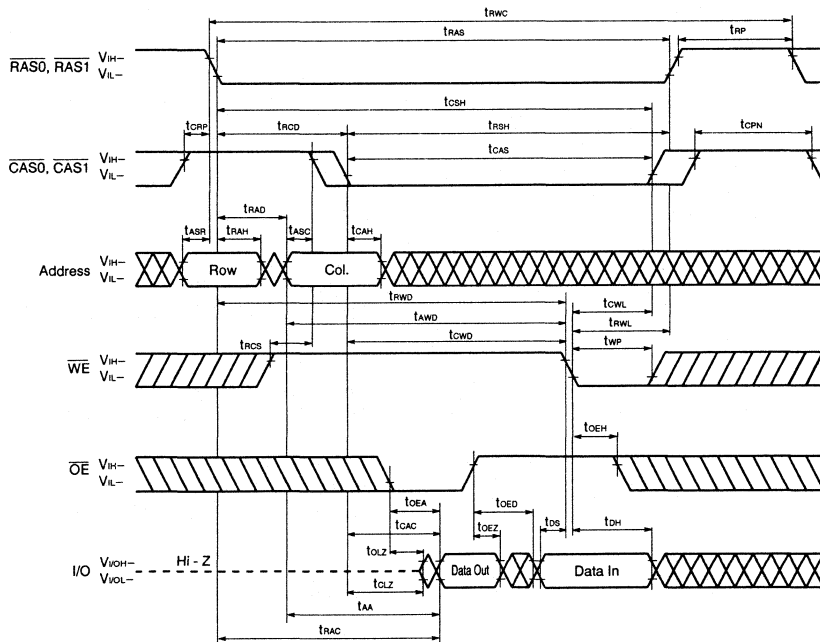
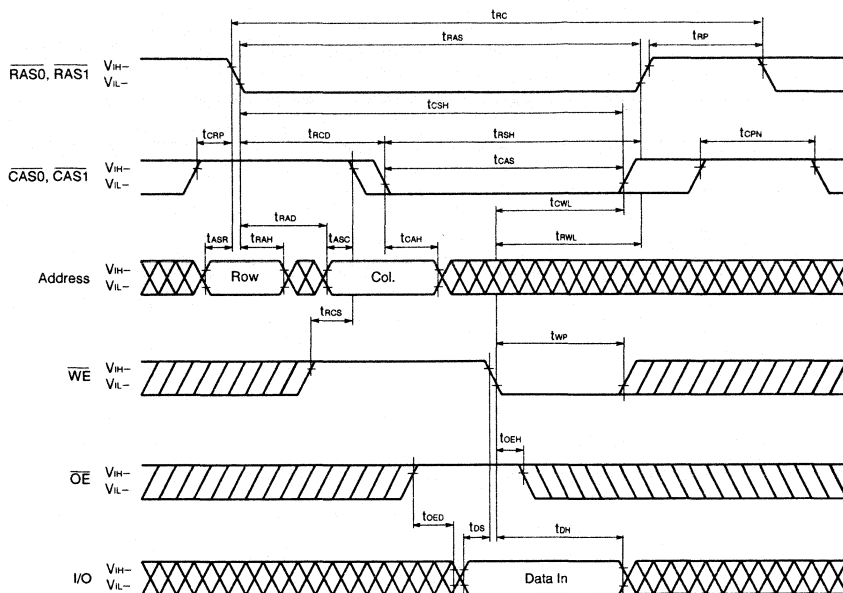
Read Cycle



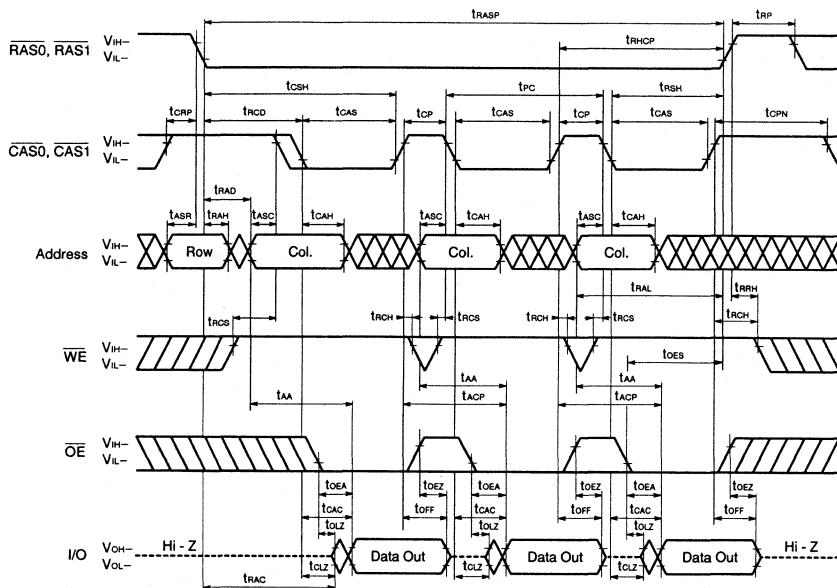
Early Write Cycle



Remark $\overline{OE}$ = Don't Care

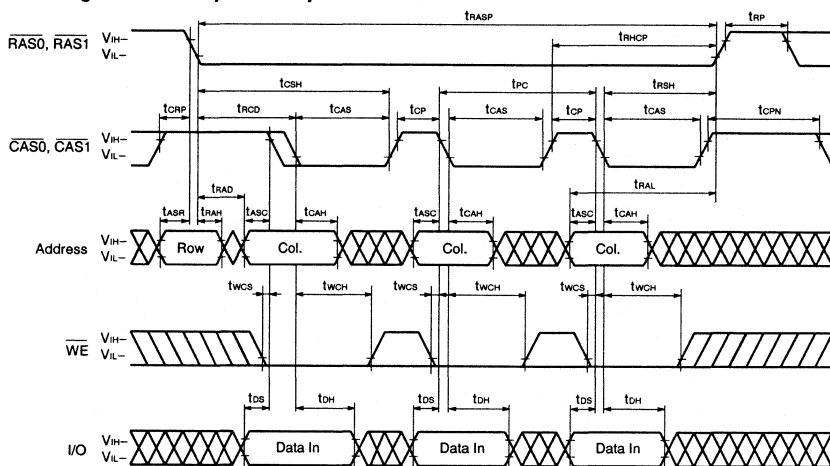


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

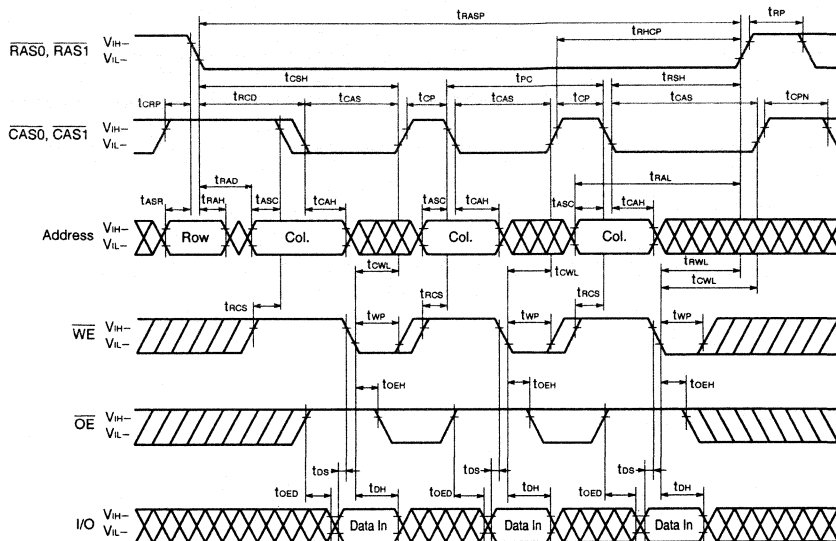
Fast Page Mode Early Write Cycle



Remark $\overline{OE} = \text{Don't Care}$

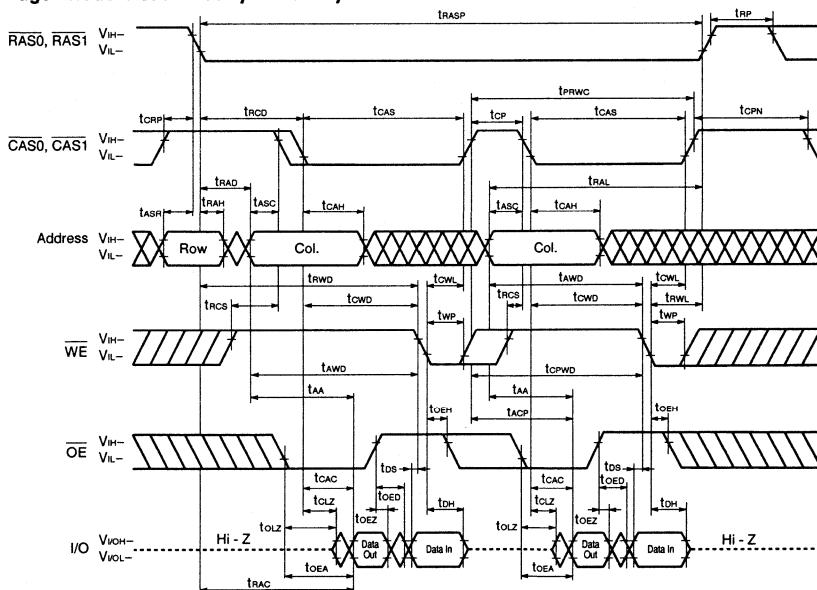
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Late Write Cycle



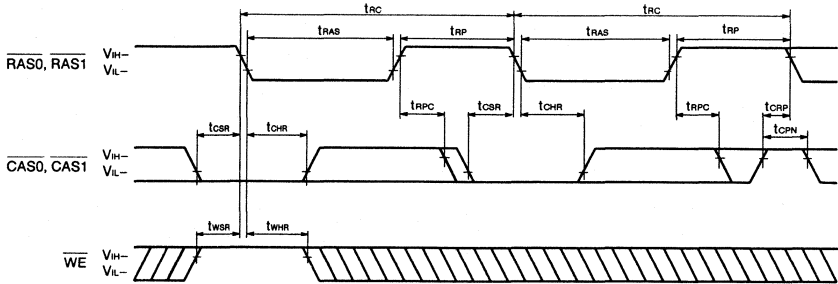
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Read Modify Write Cycle



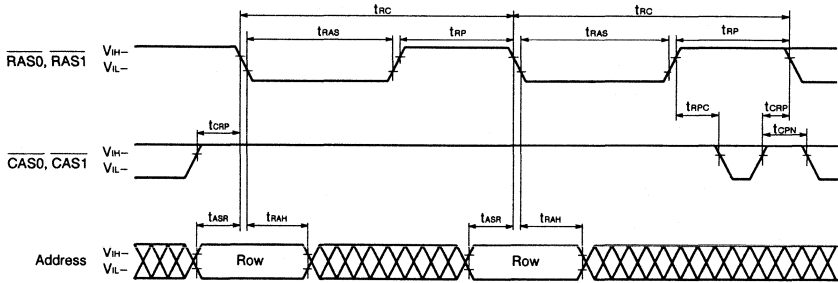
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



Remark Address, $\overline{\text{OE}}$ = Don't care I/O = Hi - Z

RAS Only Refresh Cycle

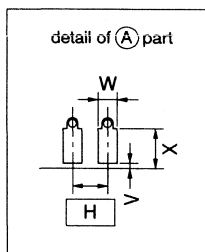
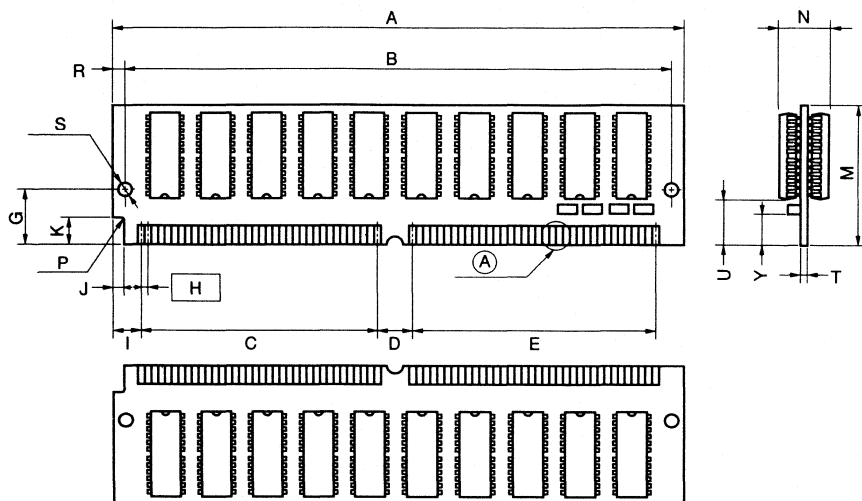


Remark $\overline{\text{WE}}, \overline{\text{OE}}$ = Don't care I/O = Hi - Z

★ Package Drawing

MC-428000AA40B, 428000AA40F

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	3.984 ^{+0.005} _{-0.006}
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
R	3.38±0.13	0.133 ^{+0.006} _{-0.005}
S	∅3.18	∅0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	5.7 MIN.	0.224 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A52

MOS INTEGRATED CIRCUIT

MC-428000A32, 428000A36 SERIES

8 M-WORD BY 32-BIT, 8 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-428000A32 series is a 8,388,608 words by 32 bits dynamic RAM module on which 16 pieces of 16 M DRAM: μ PD4217400 are assembled.

The MC-428000A36 series is a 8,388,608 words by 36 bits dynamic RAM module on which 16 pieces of 16 M DRAM: μ PD4217400 and 8 pieces of 4 M DRAM: μ PD424100 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 32 bits organization (MC-428000A32 series)
- 8,388,608 words by 36 bits organization (MC-428000A36 series)
- Fast access and cycle time

★

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-428000A32-60	60 ns	110 ns	5,170 mW	88 mW (CMOS level input)
MC-428000A32-70	70 ns	130 ns	4,730 mW	
MC-428000A32-80	80 ns	150 ns	4,290 mW	
MC-428000A36-60	60 ns	110 ns	7,810 mW	132 mW (CMOS level input)
MC-428000A36-70	70 ns	130 ns	6,930 mW	
MC-428000A36-80	80 ns	150 ns	6,270 mW	

- 2,048 refresh cycles/32 ms
- 2,048 refresh cycles/16 ms (MC-428000A36 burst refresh)
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ± 0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.

Ordering Information

[MC-428000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	16 pieces of μ PD4217400LA (300 mil SOJ) [Double side]
MC-428000A32B-70	70 ns		
MC-428000A32B-80	80 ns		
MC-428000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-428000A32F-70	70 ns		
MC-428000A32F-80	80 ns		

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[MC-428000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000A36BJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	16 pieces of μ PD4217400LA (300 mil SOJ) 8 pieces of μ PD424100LA (300 mil SOJ) [Double side]
MC-428000A36BJ-70	70 ns		
MC-428000A36BJ-80	80 ns		
MC-428000A36FJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-428000A36FJ-70	70 ns		
MC-428000A36FJ-80	80 ns		

Quality Grade

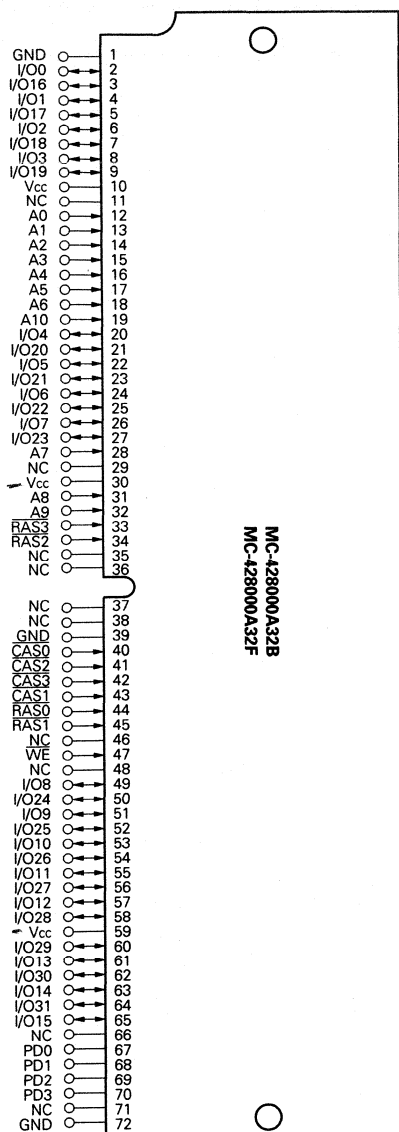
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations

[MC-428000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



- A0 - A10 : Address Inputs
 I/O0 - I/O31 : Data Inputs/Outputs
 $\overline{\text{CAS0}} - \overline{\text{CAS3}}$: Column Address Strobe
 $\overline{\text{RAS0}} - \overline{\text{RAS3}}$: Row Address Strobe
 WE : Write Enable
 V_{cc} : Power Supply
 GND : Ground
 NC : No connection

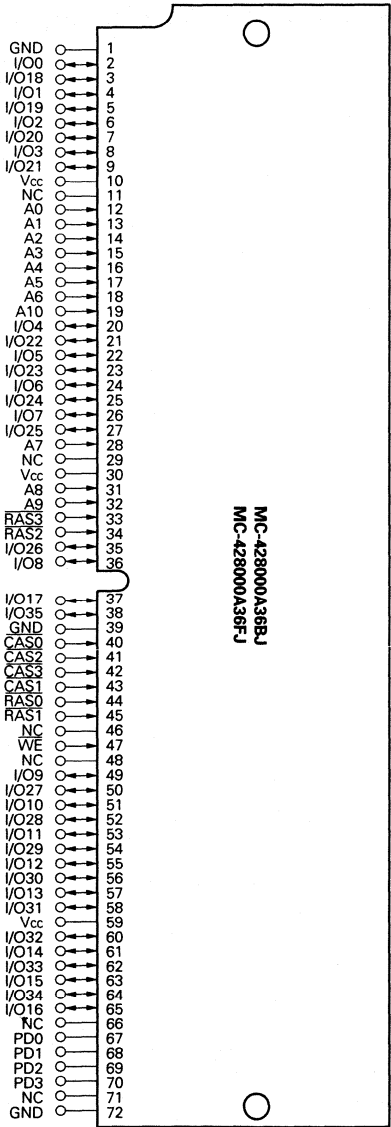
The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

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[MC-428000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



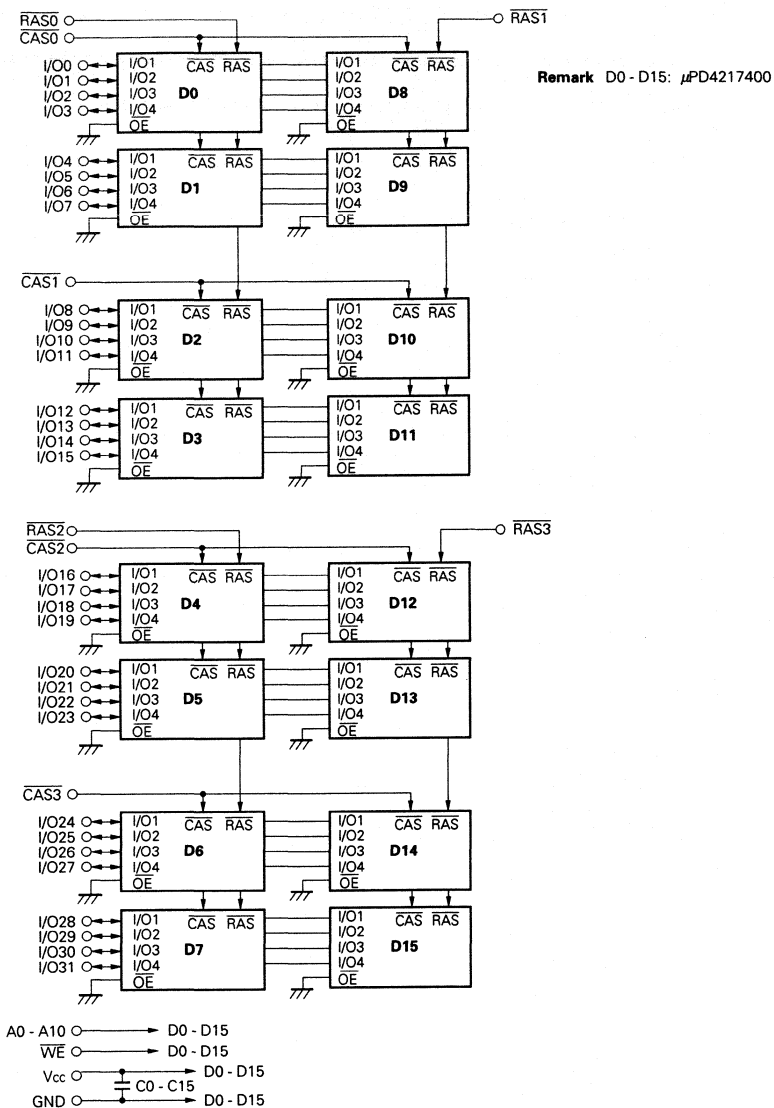
- A0 - A10 : Address Inputs
- I/O0 - I/O35 : Data Inputs/Outputs
- CAS0 - CAS3 : Column Address Strobe
- RAS0 - RAS3 : Row Address Strobe
- WE : Write Enable
- V_{cc} : Power Supply
- GND : Ground
- NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

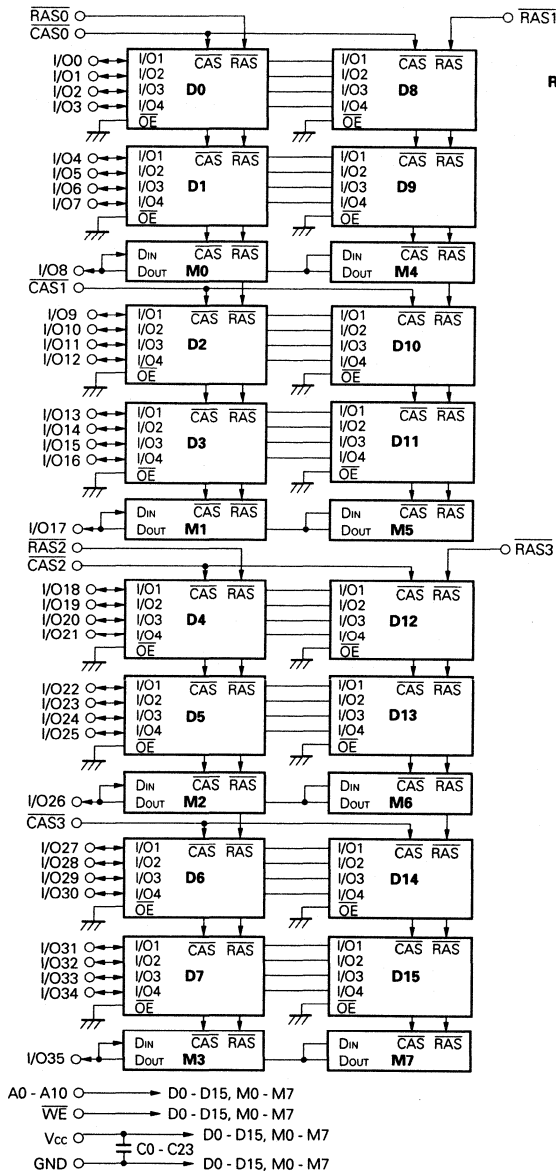
Block Diagrams

[MC-428000A32 series]



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[MC-428000A36 series]



Remark D0 - D15: μ PD4217400
M0 - M7: μ PD424100

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-428000A32	16	W
		MC-428000A36	24	
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

[MC-428000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			121	pF
	C_{I2}	$\overline{WE}$			137	
	C_{I3}	$\overline{RAS0} - \overline{RAS3}$			48	
	C_{I4}	$\overline{CAS0} - \overline{CAS3}$			48	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

[MC-428000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			161	pF
	C_{I2}	$\overline{WE}$			193	
	C_{I3}	$\overline{RAS0} - \overline{RAS3}$			62	
	C_{I4}	$\overline{CAS0} - \overline{CAS3}$			62	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			29	pF
	$C_{I/O2}$	I/O8, I/O17, I/O26, I/O35			39	

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DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-428000A32 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \text{CAS Cycling}$ $\text{trc} = \text{trc (MIN.)}$ $I_o = 0 \text{ mA}$	trac = 60 ns	940	mA	3, 4, 7
			trac = 70 ns	860		
			trac = 80 ns	780		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \text{CAS} \geq V_{IH \text{ (MIN.)}}$	$I_o = 0 \text{ mA}$	32	mA	
		$\overline{\text{RAS}}, \text{CAS} \geq V_{CC} - 0.2 \text{ V}$	$I_o = 0 \text{ mA}$	16		
RAS only refresh current	I _{CC3}	$\overline{\text{RAS}} \text{ Cycling}$ $\text{CAS} \geq V_{IH \text{ (MIN.)}}$ $\text{trc} = \text{trc (MIN.)}$ $I_o = 0 \text{ mA}$	trac = 60 ns	940	mA	3, 4, 5, 7
			trac = 70 ns	860		
			trac = 80 ns	780		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{IL \text{ (MAX.)}}, \overline{\text{CAS}} \text{ Cycling}$ $\text{tpc} = \text{tpc (MIN.)}$ $I_o = 0 \text{ mA}$	trac = 60 ns	620	mA	3, 4, 6
			trac = 70 ns	540		
			trac = 80 ns	460		
CAS before RAS refresh current	I _{CC5}	$\overline{\text{RAS}} \text{ Cycling}$ $\text{trc} = \text{trc (MIN.)}$ $I_o = 0 \text{ mA}$	trac = 60 ns	940	mA	3, 4
			trac = 70 ns	860		
			trac = 80 ns	780		
Input leakage current	I _{I (IL)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O (IL)}	$V_o = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	

[MC-428000A36 series]

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Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1,420	mA	3, 4, 7
			$t_{\text{RAC}} = 70 \text{ ns}$	1,260		
			$t_{\text{RAC}} = 80 \text{ ns}$	1,140		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$		48	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ $I_{\text{O}} = 0 \text{ mA}$		24		
RAS only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1,420	mA	3, 4, 5, 7
			$t_{\text{RAC}} = 70 \text{ ns}$	1,260		
			$t_{\text{RAC}} = 80 \text{ ns}$	1,140		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	980	mA	3, 4, 6
			$t_{\text{RAC}} = 70 \text{ ns}$	860		
			$t_{\text{RAC}} = 80 \text{ ns}$	740		
CAS before RAS refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1,420	mA	3, 4
			$t_{\text{RAC}} = 70 \text{ ns}$	1,260		
			$t_{\text{RAC}} = 80 \text{ ns}$	1,140		
Input leakage current	I _{I (IL)}	$V_{\text{I}} = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O (IL)}	$V_{\text{O}} = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage	V _{OH}	$I_{\text{O}} = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_{\text{O}} = +4.2 \text{ mA}$		0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

[MC-428000A32 series]

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RSP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15		18		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RNH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	5		5		5		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10		10		10		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		32		32		32	ms	

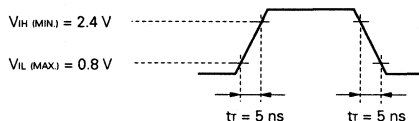
[MC-428000A36 series]

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20		20		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		10		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		10		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	15		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	10		10		10		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10		10		10		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	Distributed refresh	t _{REF}	32		32		32	ms	
	Burst refresh		16		16		16	ms	

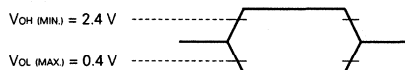
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on cycle rates (trac and tpc).
4. Specified values are obtained with outputs unloaded.
5. Icc3 is measured assuming that all column address inputs are held at either high or low.
6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq \text{VIL (MAX.)}$ and $\overline{\text{CAS}} \geq \text{VIH (MIN.)}$.
8. AC measurements assume $\text{tr} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



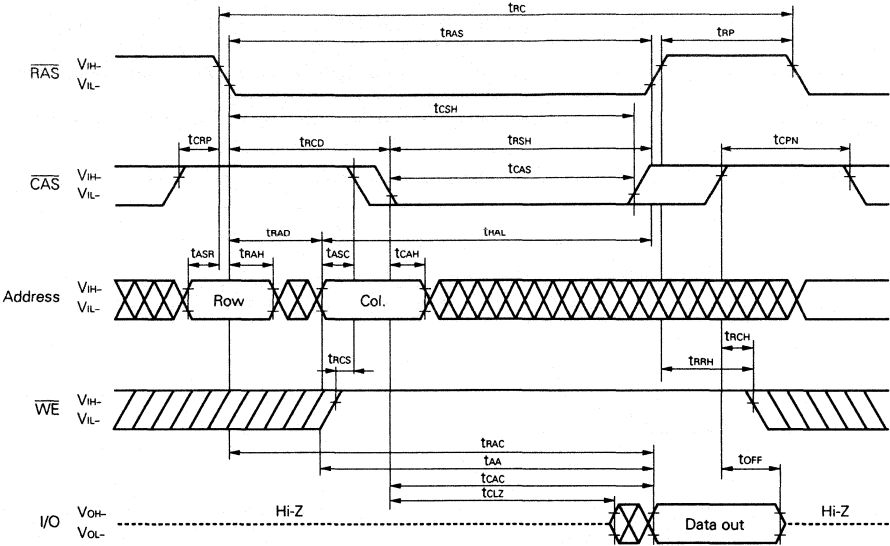
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

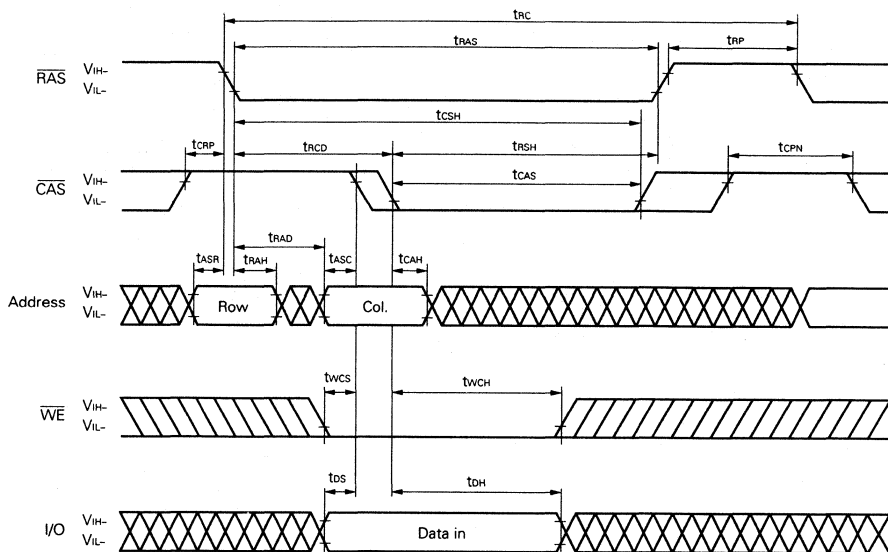
trAD (MAX.) and trCD (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. toFF (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to VOH or VOL .
13. tCRP (MIN.) requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either trCH (MIN.) or trRH (MIN.) should be met in read cycles.
15. In early write cycles, twCH (MIN.) should be met.
16. tDS (MIN.) and tDH (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $\text{twCS} \geq \text{twCS (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Read Cycle



Early Write Cycle

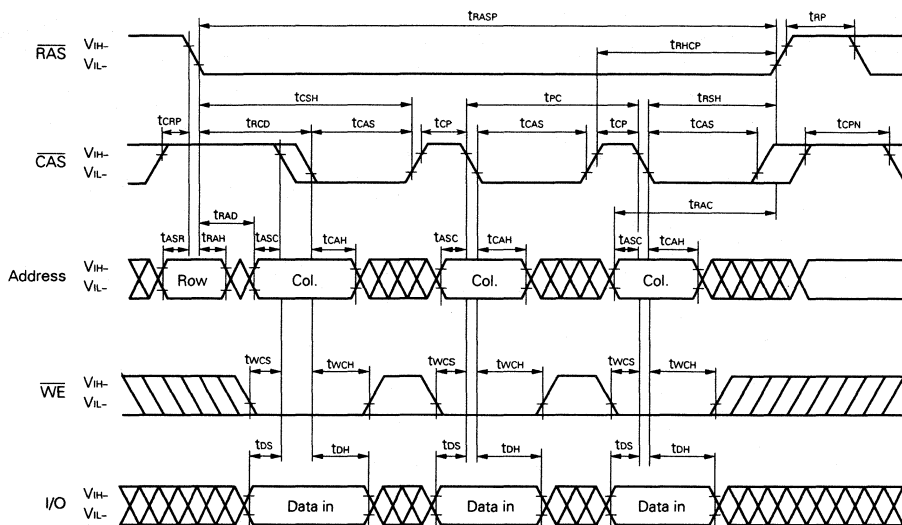


The diagram illustrates the timing relationships for a 64K16 DRAM. The signals shown are RAS, CAS, Address, WE, and I/O. The timing parameters are defined as follows:

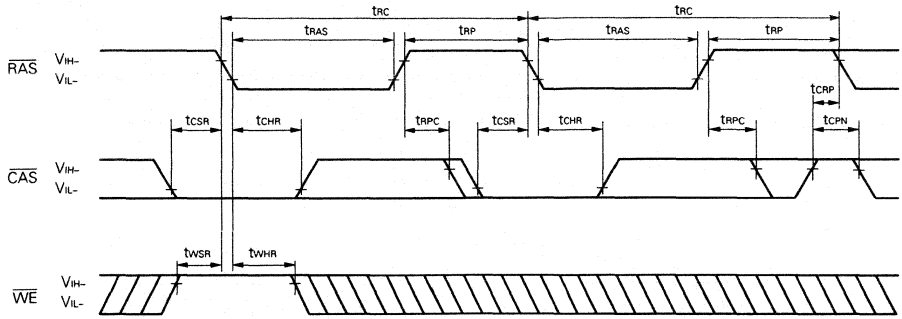
- RAS:** t_{RASP} (RAS pulse width), t_{RHCP} (RAS hold time), t_{RP} (RAS precharge time).
- CAS:** t_{CRP} (CAS precharge time), t_{CD} (CAS delay), t_{CAS} (CAS access time), t_{CP} (CAS pulse width), t_{CSH} (CAS hold time), t_{CNP} (CAS non-pulse time), t_{TRSH} (CAS to RAS setup time).
- Address:** t_{RAD} (Row address delay), t_{RAH} (Row address hold time), t_{ASC} (Column address delay), t_{CAH} (Column address hold time), t_{TRAL} (Address to RAS delay), t_{TRCH} (Address to RAS hold time).
- WE:** t_{WCH} (Write enable delay), t_{WRH} (Write enable hold time), t_{WAC} (Write enable access time), t_{WTC} (Write enable to CAS delay), t_{WTR} (Write enable to RAS delay).
- I/O:** t_{OAH} (Output address delay), t_{OAL} (Output address hold time), t_{OCH} (Output column delay), t_{OCL} (Output column hold time), t_{OAC} (Output access time), t_{OFC} (Output to CAS delay), t_{OFR} (Output to RAS delay).

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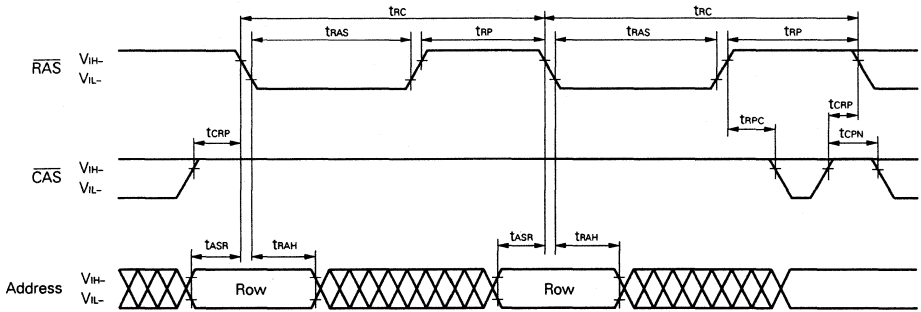
Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

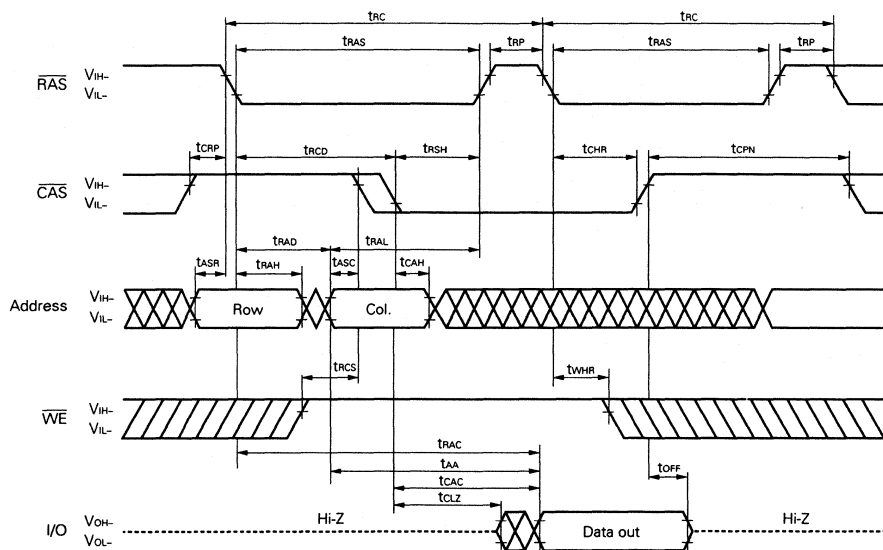
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

Remark Address: Don't care I/O: Hi-Z

 $\overline{\text{RAS}}$ Only Refresh Cycle

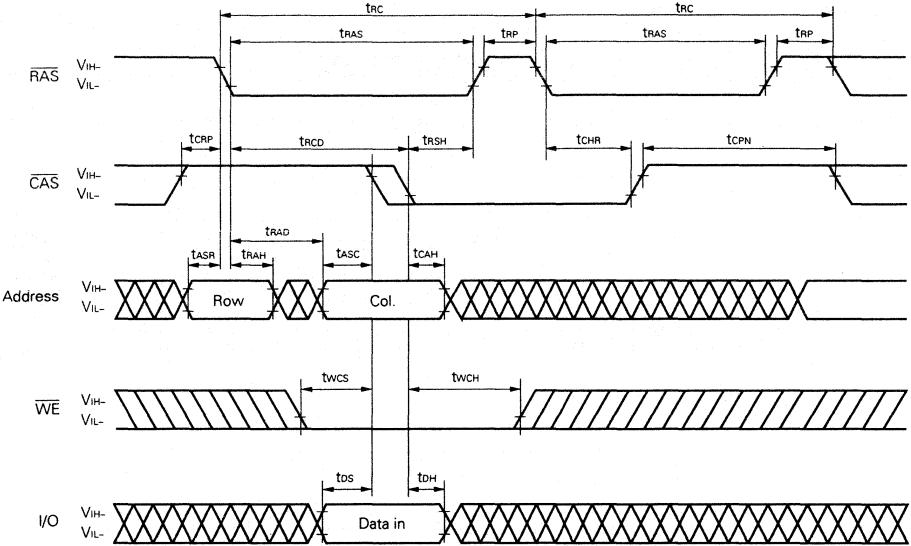
Remark $\overline{\text{WE}}$: Don't care I/O: Hi-Z

★ Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

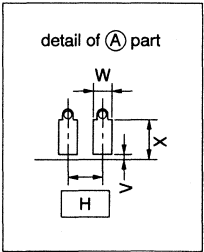
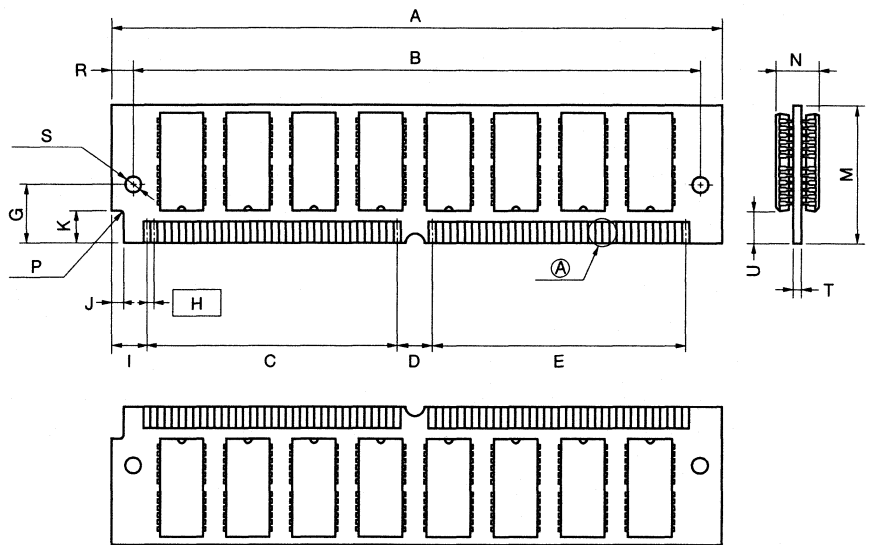
★



Package Drawings

[MC-428000A32B, 428000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



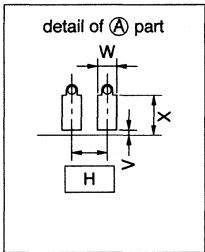
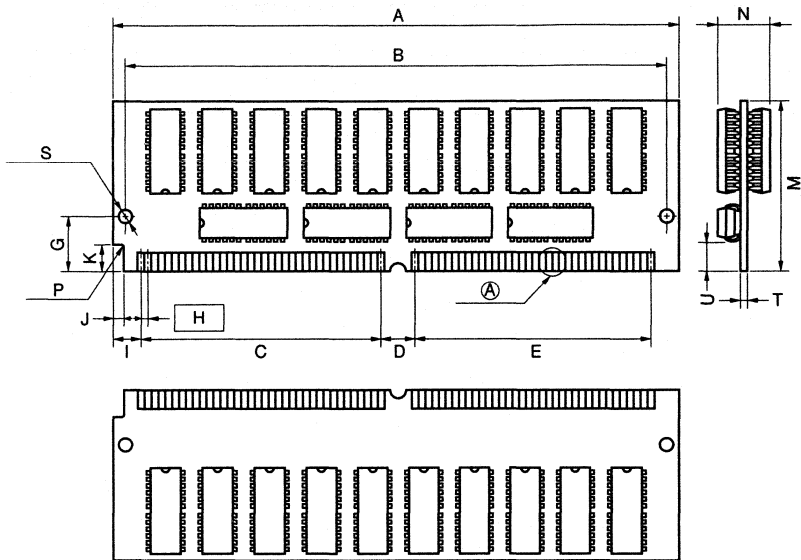
ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	3.984 ^{+0.005} _{-0.006}
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
R	3.38±0.13	0.133 ^{+0.006} _{-0.005}
S	φ3.18	φ0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A55

[MC-428000A36BJ, 428000A36FJ]

★

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	φ3.18	φ0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

M72B-50A50

MOS INTEGRATED CIRCUIT

MC-424000AA40 SERIES

4 M-WORD BY 40-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-424000AA40 is a 4 194 304 words by 40 bits dynamic RAM module on which 10 pieces of 16 M bits CMOS Dynamic RAM (μ PD4217400) are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4 194 304 words by 40 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000AA40-60	60 ns	110 ns	5 250 mW	52.5 mW (CMOS level input)
MC-424000AA40-70	70 ns	130 ns	4 725 mW	
MC-424000AA40-80	80 ns	150 ns	4 200 mW	

- Fast page mode
- 2 048 refresh cycles / 32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- 40-bit simultaneous switching
- Output buffers control : $\overline{\text{OE}}$ pin
- Single +5.0 V $\pm 5\%$ power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.

★ Ordering Information

Part number	Access time (MAX.)	Package	Mounted device
MC-424000AA40B-60	60 ns	72-pin Single In-line Memory Module (Socket type) Edge connector : Solder coating (HAL)	10 pieces of μ PD4217400LA (300 mil SOJ) [Single side]
MC-424000AA40B-70	70 ns		
MC-424000AA40B-80	80 ns		
MC-424000AA40F-60	60 ns	72-pin Single In-line Memory Module (Socket type) Edge connector : Gold plating	
MC-424000AA40F-70	70 ns		
MC-424000AA40F-80	80 ns		

Quality Grade

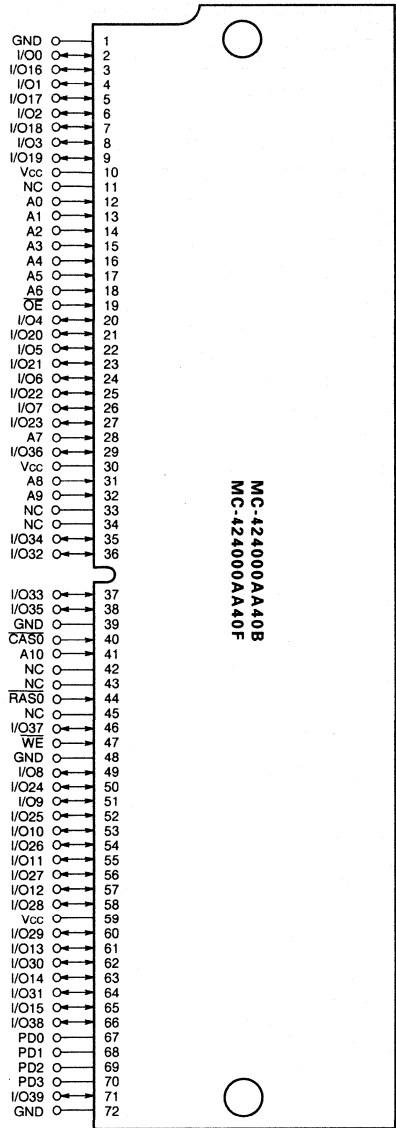
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration



72-pin Single In-line Memory Module Socket Type (Edge Connector : Solder Coating, Gold Plating)

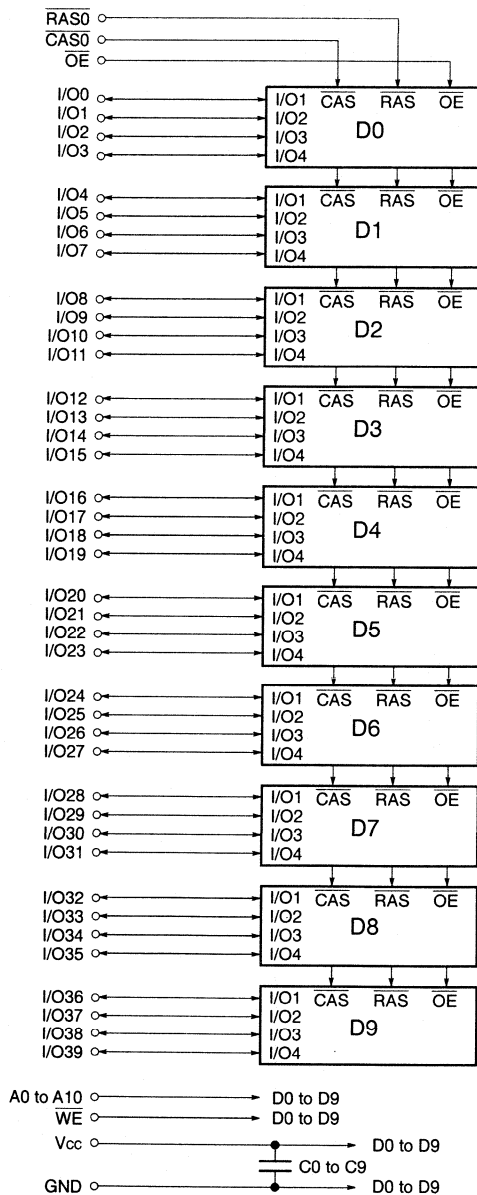


- A0 to A10 : Address Inputs
- I/O0 to I/O39 : Data Inputs/Outputs
- $\overline{\text{CAS0}}$: Column Address Strobe
- $\overline{\text{RAS0}}$: Row Address Strobe
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	GND	GND	GND
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

Block Diagram



Remark D0 to D9 : μ PD4217400

Electrical Specifications Notes 1, 2**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		10	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A10			110	pF
	C_{I2}	$\overline{WE}$, OE			110	
	C_{I3}	$\overline{RAS0}$			85	
	C_{I4}	$\overline{CAS0}$			85	
Data Input/Output capacitance	$C_{I/O}$	I/O0 to I/O39			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	$t_{RAC} = 60 \text{ ns}$		1 000	mA	3,4,7
		$t_{RC} = t_{RC(MIN.)}$	$t_{RAC} = 70 \text{ ns}$		900		
		$I_O = 0 \text{ mA}$	$t_{RAC} = 80 \text{ ns}$		800		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$	$I_O = 0 \text{ mA}$		20	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}-0.2 \text{ V}$	$I_O = 0 \text{ mA}$		10		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling	$t_{RAC} = 60 \text{ ns}$		1 000	mA	3,4,5,7
		$\overline{CAS} \geq V_{IH(MIN.)}$	$t_{RAC} = 70 \text{ ns}$		900		
		$t_{RC} = t_{RC(MIN.)}$	$t_{RAC} = 80 \text{ ns}$		800		
Operating current (Fast page mode)	I_{CC4}	$\overline{CAS}$ Cycling	$t_{RAC} = 60 \text{ ns}$		700	mA	3,4,6
		$\overline{RAS} \leq V_{IL(MAX.)}$	$t_{RAC} = 70 \text{ ns}$		600		
		$t_{PC} = t_{PC(MIN.)}$	$t_{RAC} = 80 \text{ ns}$		500		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling,	$t_{RAC} = 60 \text{ ns}$		1 000	mA	3,4
		$t_{RC} = t_{RC(MIN.)}$	$t_{RAC} = 70 \text{ ns}$		900		
		$I_O = 0 \text{ mA}$	$t_{RAC} = 80 \text{ ns}$		800		
Input leakage current	$I_{I(L)}$	$V_I = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V		-10	+10	μA	
Output leakage current	$I_{O(L)}$	$V_O = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)		-10	+10	μA	
High level output voltage	V_{OH}	$I_O = -5.0 \text{ mA}$		2.4		V	
Low level output voltage	V_{OL}	$I_O = +4.2 \text{ mA}$			0.4	V	

AC Characteristics

(Recommended Operating Conditions unless otherwise noted) Notes 8, 9

(1/2)

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		$t_{RAC} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	160		180		205		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time from Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
Access Time from $\overline{OE}$	t_{OEA}		15		18		20	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10 000	70	10 000	80	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125 000	70	125 000	80	125 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10 000	18	10 000	20	10 000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	

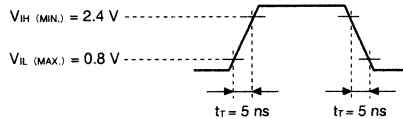
(2/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
WE Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
WE Pulse Width	t _{WP}	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
CAS to WE Delay Time	t _{CWD}	40		43		50		ns	17
RAS to WE Delay Time	t _{RWD}	85		95		110		ns	17
CAS Precharge to WE Delay Time	t _{CPWD}	58		65		70		ns	17
Column Address to WE Delay Time	t _{AWD}	55		60		70		ns	17
WE Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20		20		20		ns	
WE Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15		15		15		ns	
CAS Setup Time (CAS before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	5		5		5		ns	
CAS Hold Time (CAS before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10		10		10		ns	
WE Setup Time	t _{WSR}	10		10		10		ns	
WE Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		32		32		32	ms	

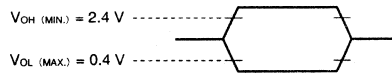
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on cycle rates (trc and trc).
4. Specified values are obtained with outputs unloaded.
5. Icc3 is measured assuming that all column address inputs are held at either high or low.
6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq \text{VIL (MAX.)}$ and $\overline{\text{CAS}} \geq \text{VIH (MIN.)}$.
8. AC measurements assume $\text{tr} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



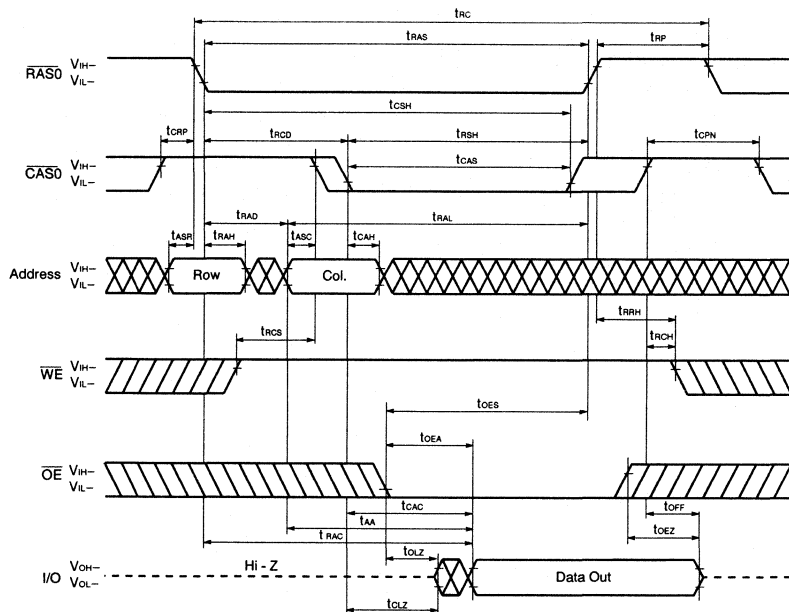
10. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

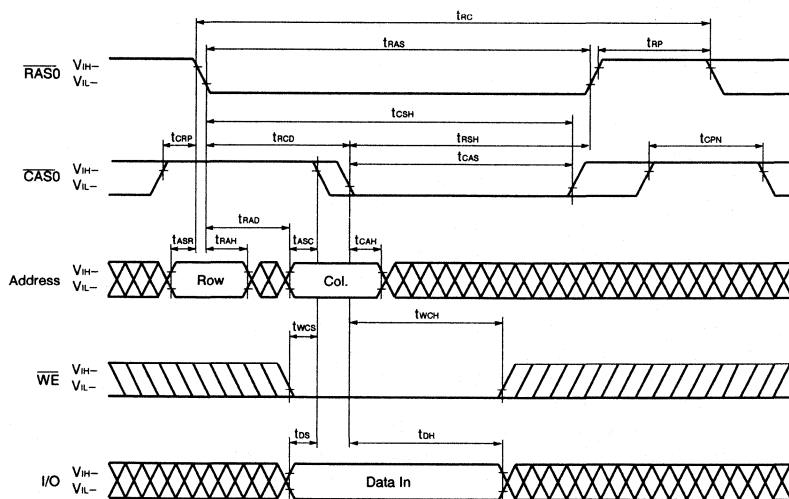
trAD (MAX.) and trCD (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. toff (MAX.) and toEZ (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to VOH or VOL .
13. tCRP (MIN.) requirement should be applied to $\overline{\text{RAS}} / \overline{\text{CAS}}$ cycles.
14. Either trCH (MIN.) or trRH (MIN.) should be met in read cycles.
15. tWP (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twCH (MIN.) should be met.
16. tDS (MIN.) and tDH (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
17. If $\text{twCS} \geq \text{twCS (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{trWD} \geq \text{trWD (MIN.)}$, $\text{tcWD} \geq \text{tcWD (MIN.)}$, $\text{tAWD} \geq \text{tAWD (MIN.)}$ and $\text{tcpWD} \geq \text{tcpWD (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Read Cycle

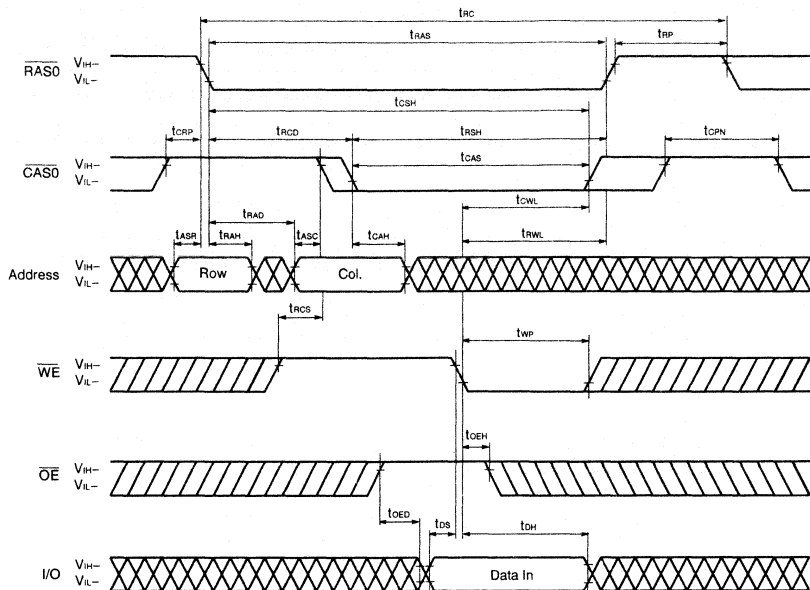


Early Write Cycle

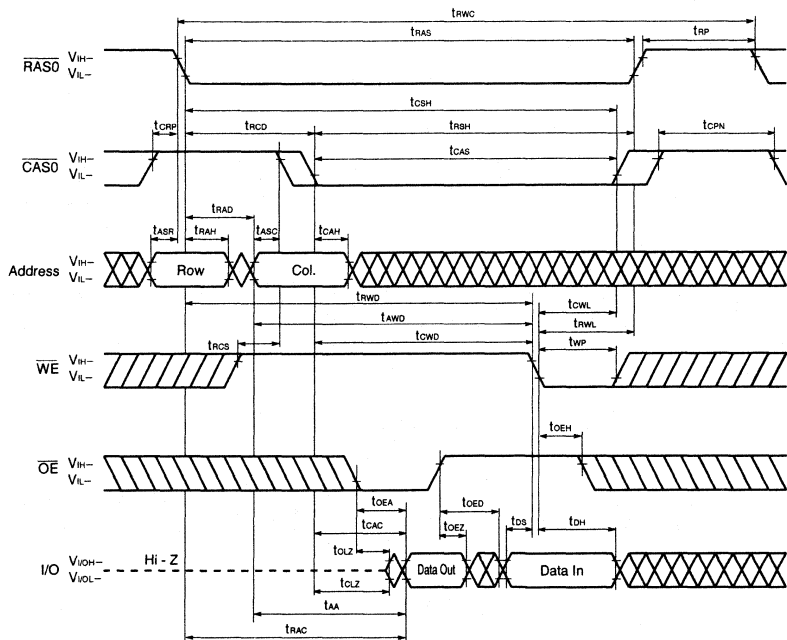


Remark $\overline{OE} = \text{Don't Care}$

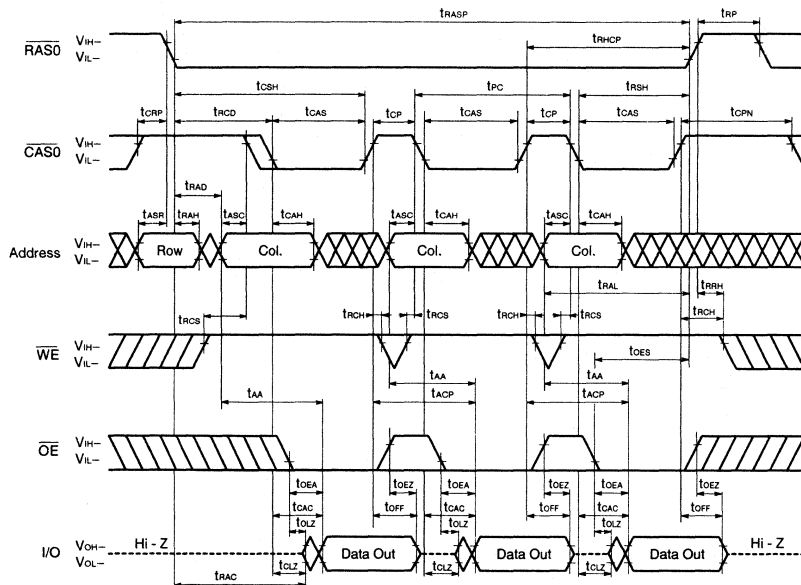
Late Write Cycle



Read Modify Write Cycle

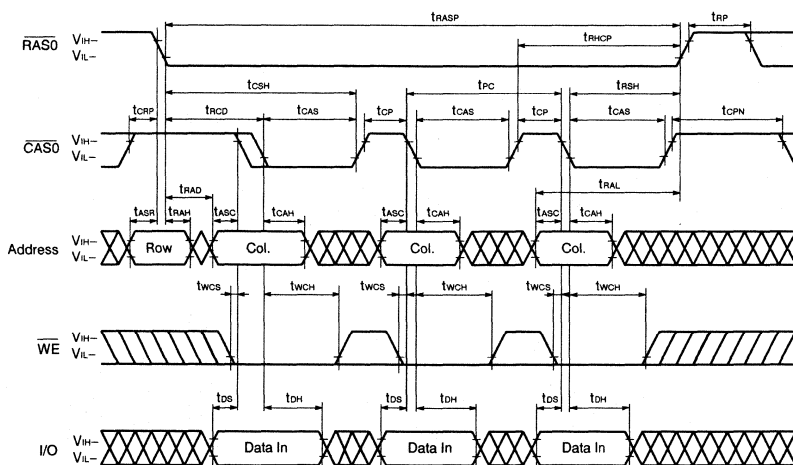


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

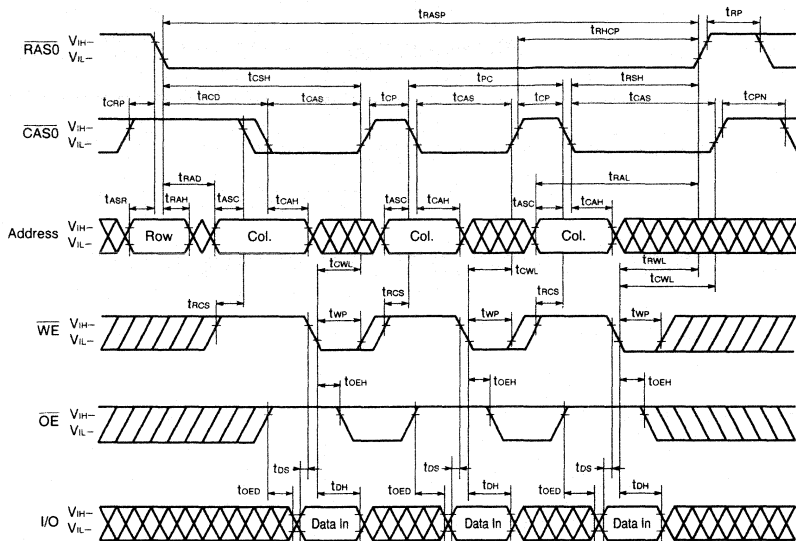
Fast Page Mode Early Write Cycle



Remark $\overline{OE} = \text{Don't Care}$

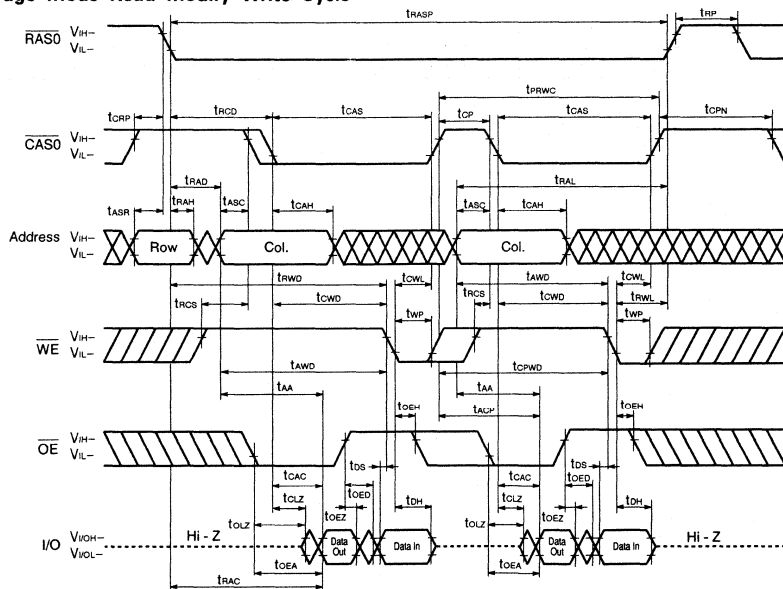
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Late Write Cycle



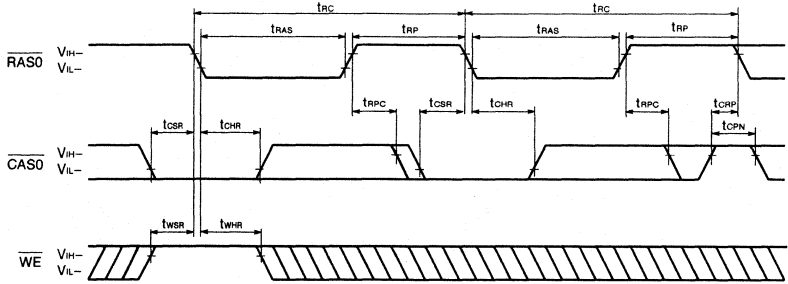
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Read Modify Write Cycle



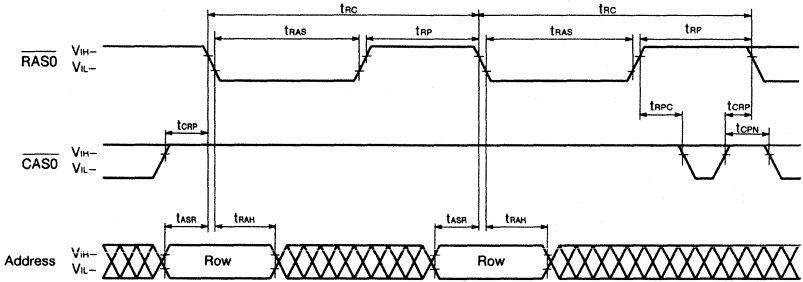
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

CAS Before RAS Refresh Cycle



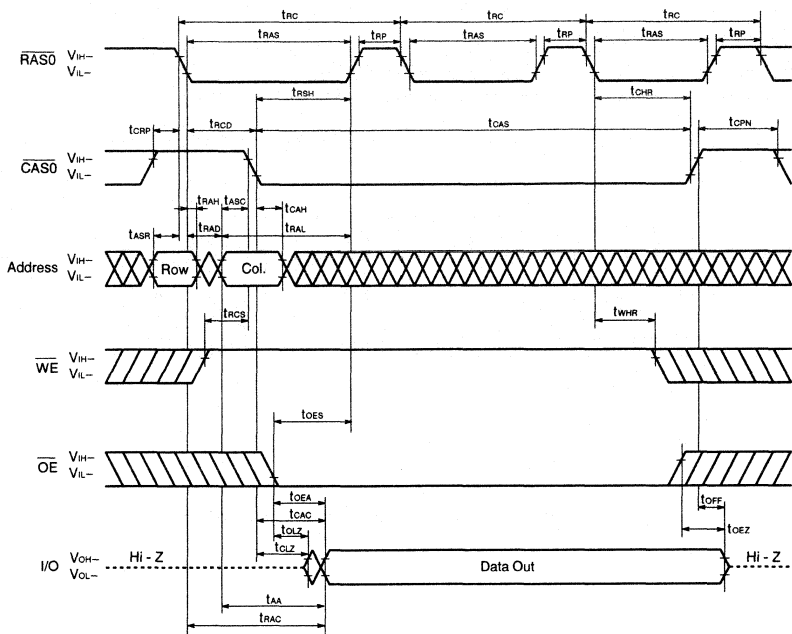
Remark Address, $\overline{OE}$ = Don't care I/O = Hi - Z

RAS Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$ = Don't care I/O = Hi - Z

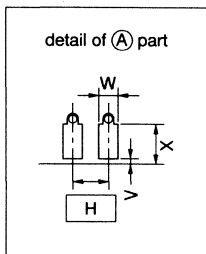
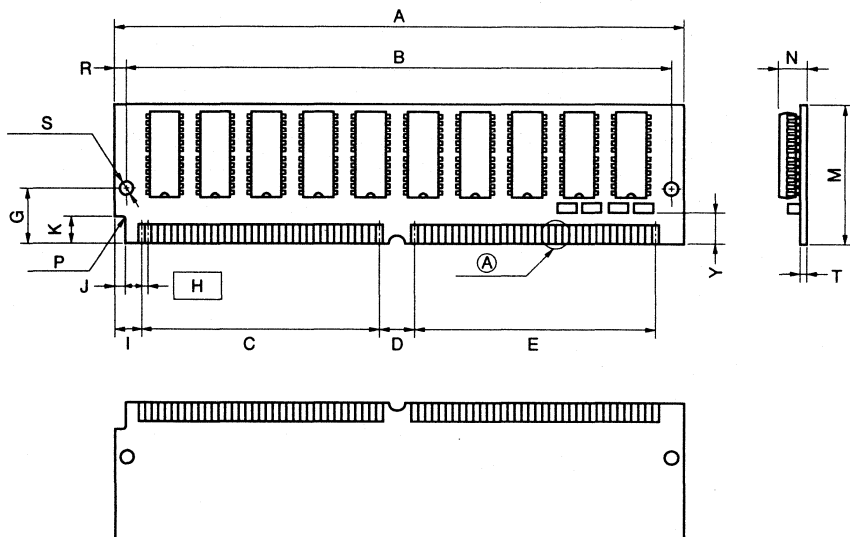
Hidden Refresh Cycle



★ Package Drawing

MC-424000AA40B, 424000AA40F

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	3.984 ^{+0.005} _{-0.006}
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
R	3.38±0.13	0.133 ^{+0.006} _{-0.005}
S	∅3.18	∅0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A53

MOS INTEGRATED CIRCUIT

MC-424000A32, 424000A36 SERIES

4 M-WORD BY 32-BIT, 4 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-424000A32 series is a 4,194,304 words by 32 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μ PD4217400 are assembled.

The MC-424000A36 series is a 4,194,304 words by 36 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μ PD4217400 and 4 pieces of 4 M DRAM: μ PD424100 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 32 bits organization (MC-424000A32 series)
- 4,194,304 words by 36 bits organization (MC-424000A36 series)
- Fast access and cycle time

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Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000A32-60	60 ns	110 ns	4,840 mW	44 mW (CMOS level input)
MC-424000A32-70	70 ns	130 ns	4,400 mW	
MC-424000A32-80	80 ns	150 ns	3,960 mW	
MC-424000A36-60	60 ns	110 ns	7,480 mW	66 mW (CMOS level input)
MC-424000A36-70	70 ns	130 ns	6,600 mW	
MC-424000A36-80	80 ns	150 ns	5,940 mW	

- 2,048 refresh cycles/32 ms
- 2,048 refresh cycles/16 ms (MC-424000A36 burst refresh)
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ± 0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.

★ Ordering Information

[MC-424000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μ PD4217400LA (300 mil SOJ) [Single side]
MC-424000A32B-70	70 ns		
MC-424000A32B-80	80 ns		
MC-424000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-424000A32F-70	70 ns		
MC-424000A32F-80	80 ns		

[MC-424000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices	
MC-424000A36BE-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μ PD4217400LA (300 mil SOJ)	
MC-424000A36BE-70	70 ns		72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μ PD424100LA (300 mil SOJ)
MC-424000A36BE-80	80 ns			[Double side]
MC-424000A36FE-60	60 ns			
MC-424000A36FE-70	70 ns			
MC-424000A36FE-80	80 ns			
MC-424000A36BJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)		8 pieces of μ PD4217400LA (300 mil SOJ)
MC-424000A36BJ-70	70 ns		72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μ PD424100LA (300 mil SOJ)
MC-424000A36BJ-80	80 ns			[Single side]
MC-424000A36FJ-60	60 ns			
MC-424000A36FJ-70	70 ns			
MC-424000A36FJ-80	80 ns			

Quality Grade

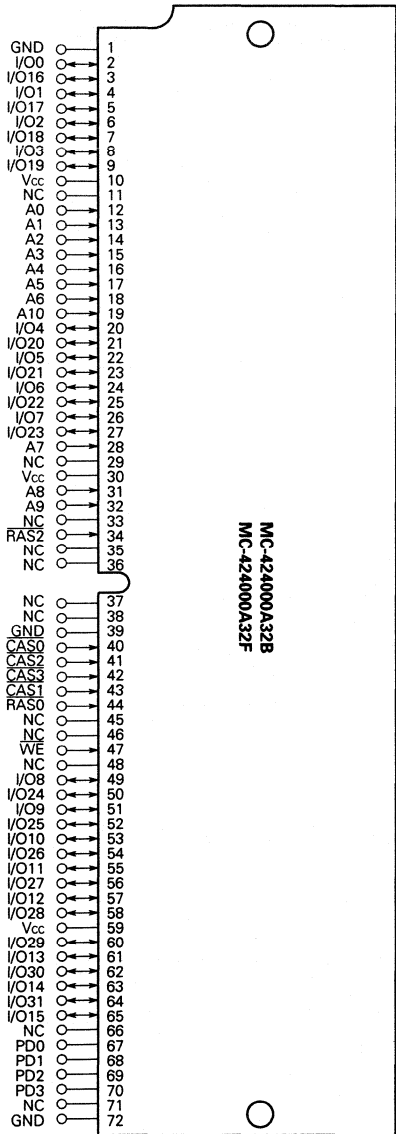
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration

[MC-424000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



- A0 - A10 : Address Inputs
- I/O0 - I/O31 : Data Inputs/Outputs
- CAS0 - CAS3 : Column Address Strobe
- RAS0, RAS2 : Row Address Strobe
- WE : Write Enable
- Vcc : Power Supply
- GND : Ground
- NC : No connection

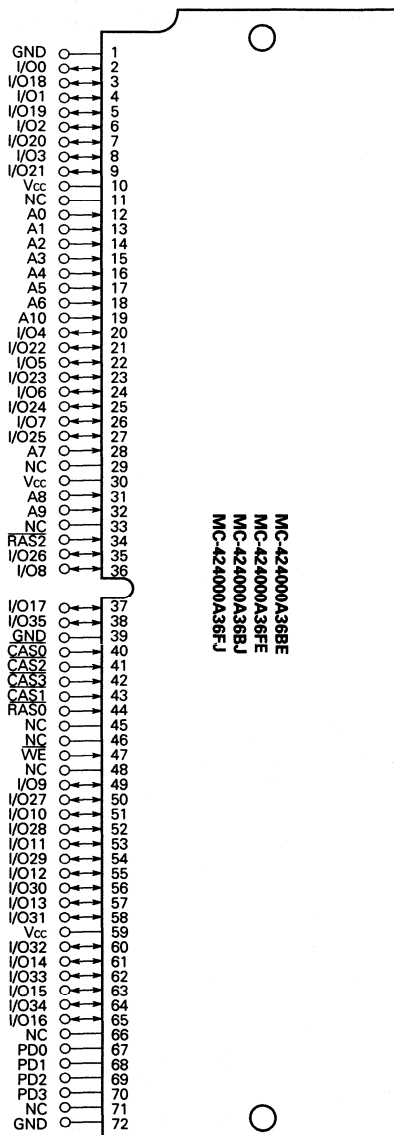
The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	GND	GND	GND
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

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[MC-424000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



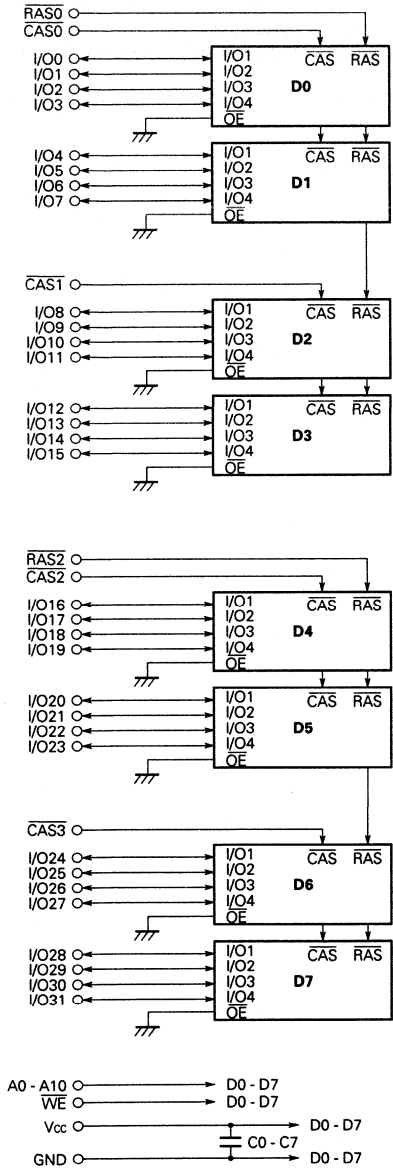
- A0 - A10 : Address Inputs
I/O0 - I/O35 : Data Inputs/Outputs
 $\overline{\text{CAS0}} - \text{CAS3}$: Column Address Strobe
 $\overline{\text{RAS0}}, \text{RAS2}$: Row Address Strobe
 $\overline{\text{WE}}$: Write Enable
Vcc : Power Supply
GND : Ground
NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	GND	GND	GND
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

Block Diagram

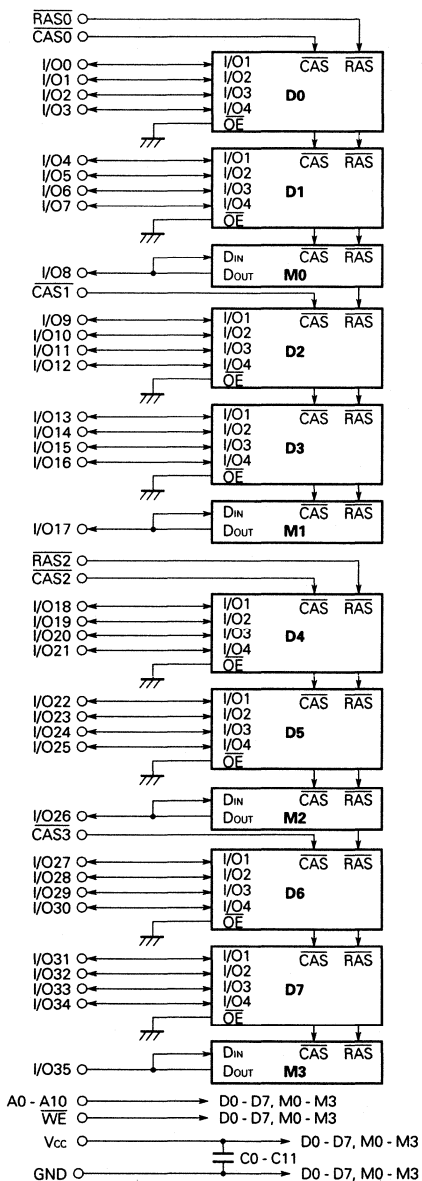
[MC-424000A32 series]



Remark D0 - D7 : μ PD4217400

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[MC-424000A36 series]



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-424000A32	8	W
		MC-424000A36	12	
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

[MC-424000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			68	pF
	C_{I2}	$\overline{WE}$			76	
	C_{I3}	$\overline{RAS0}, \overline{RAS2}$			43	
	C_{I4}	$\overline{CAS0} - \overline{CAS3}$			29	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			17	pF

[MC-424000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			88	pF
	C_{I2}	$\overline{WE}$			104	
	C_{I3}	$\overline{RAS0}, \overline{RAS2}$			57	
	C_{I4}	$\overline{CAS0} - \overline{CAS3}$			36	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			17	pF
	$C_{I/O2}$	I/O8, I/O17, I/O26, I/O35			22	

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DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-424000A32 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{Io} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$	880	mA	3, 4, 7
			$\text{trac} = 70 \text{ ns}$	800		
			$\text{trac} = 80 \text{ ns}$	720		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $\text{Io} = 0 \text{ mA}$		16	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ $\text{Io} = 0 \text{ mA}$		8		
RAS only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.})$ $\text{Io} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$	880	mA	3, 4, 5, 7
			$\text{trac} = 70 \text{ ns}$	800		
			$\text{trac} = 80 \text{ ns}$	720		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.})$ $\text{Io} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$	560	mA	3, 4, 6
			$\text{trac} = 70 \text{ ns}$	480		
			$\text{trac} = 80 \text{ ns}$	400		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{Io} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$	880	mA	3, 4
			$\text{trac} = 70 \text{ ns}$	800		
			$\text{trac} = 80 \text{ ns}$	720		
Input leakage current	I _{I (IL)}	$V_{\text{I}} = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O (IL)}	$V_{\text{O}} = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage	V _{OH}	$\text{Io} = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$\text{Io} = +4.2 \text{ mA}$		0.4	V	

[MC-424000A36 series]

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Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1,360	mA	3, 4, 7
			$t_{\text{RAC}} = 70 \text{ ns}$	1,200		
			$t_{\text{RAC}} = 80 \text{ ns}$	1,080		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$I_o = 0 \text{ mA}$	24	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$I_o = 0 \text{ mA}$	12		
RAS only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1,360	mA	3, 4, 5, 7
			$t_{\text{RAC}} = 70 \text{ ns}$	1,200		
			$t_{\text{RAC}} = 80 \text{ ns}$	1,080		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	920	mA	3, 4, 6
			$t_{\text{RAC}} = 70 \text{ ns}$	800		
			$t_{\text{RAC}} = 80 \text{ ns}$	680		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1,360	mA	3, 4
			$t_{\text{RAC}} = 70 \text{ ns}$	1,200		
			$t_{\text{RAC}} = 80 \text{ ns}$	1,080		
Input leakage current	I _{I (IL)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O (IL)}	$V_o = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

[MC-424000A32 series]

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15		18		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	5		5		5		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10		10		10		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		32		32		32	ms	

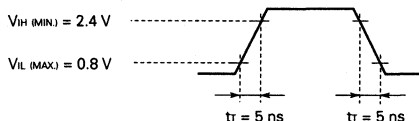
[MC-424000A36 series]

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RSP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20		20		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		10		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		10		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	15		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	10		10		10		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10		10		10		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	Distributed refresh	t _{REF}	32		32		32	ms	
	Burst refresh		16		16		16	ms	

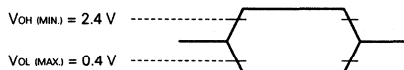
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. tcc1 , tcc3 , tcc4 and tcc5 depend on cycle rates (trc and tpc).
4. Specified values are obtained with outputs unloaded.
5. tcc3 is measured assuming that all column address inputs are held at either high or low.
6. tcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. tcc1 and tcc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq \text{VIL (MAX.)}$ and $\overline{\text{CAS}} \geq \text{VIH (MIN.)}$.
8. AC measurements assume $\text{tr} = 5 \text{ ns}$.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



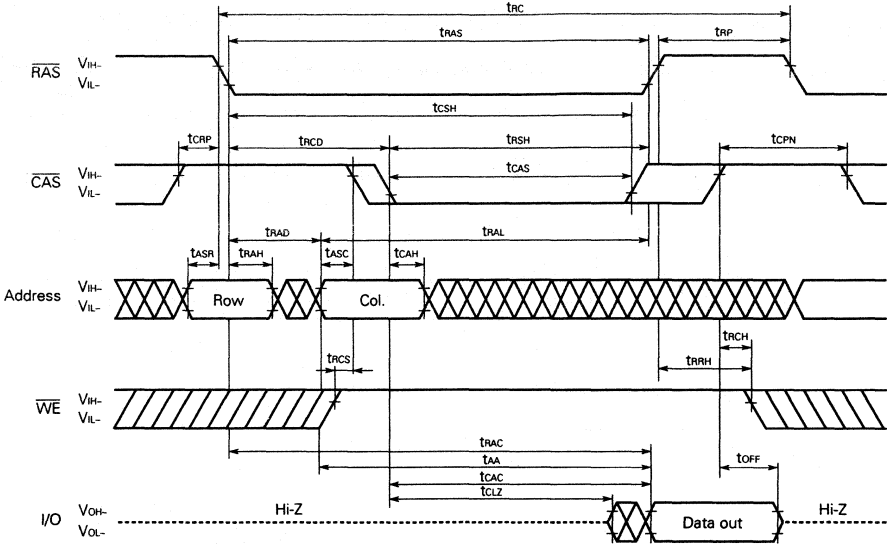
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD (MAX.) and trCD (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. tOFF (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to VOH or VOL .
13. tCRP (MIN.) requirements should be applied to $\overline{\text{RAS/CAS}}$ cycles.
14. Either trCH (MIN.) or trRH (MIN.) should be met in read cycles.
15. In early write cycles, twCH (MIN.) should be met.
16. tDS (MIN.) and tDH (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $\text{twCS} \geq \text{twCS (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

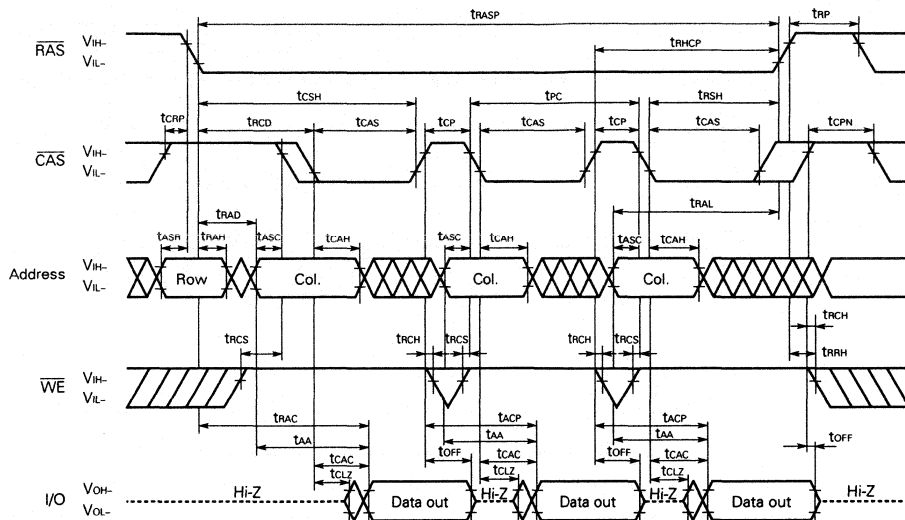
Read Cycle



The diagram illustrates the timing relationships for a 256Kbit DRAM. The signals shown are $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, $\overline{\text{WE}}$, and I/O. The timing parameters are defined as follows:

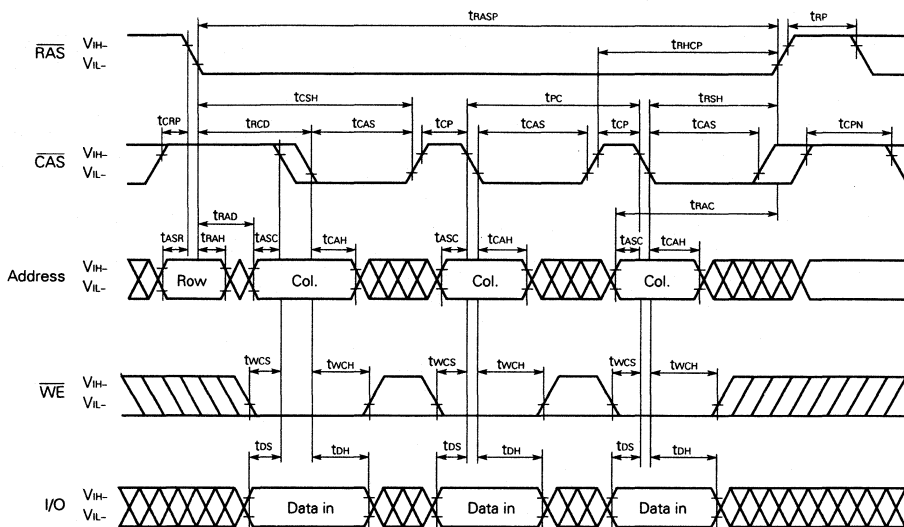
- t_{RAS} : RAS access time (from $\overline{\text{RAS}}$ falling edge to data valid).
- t_{CAS} : CAS access time (from $\overline{\text{CAS}}$ falling edge to data valid).
- t_{AD} : Address setup time (from address last change to $\overline{\text{RAS}}$ falling edge).
- t_{AD} : Address hold time (from $\overline{\text{RAS}}$ falling edge to address first change).
- t_{AS} : RAS to CAS delay (from $\overline{\text{RAS}}$ falling edge to $\overline{\text{CAS}}$ falling edge).
- t_{AS} : CAS to RAS delay (from $\overline{\text{CAS}}$ falling edge to $\overline{\text{RAS}}$ falling edge).
- t_{WE} : Write enable pulse width (from $\overline{\text{WE}}$ falling edge to rising edge).
- t_{WE} : Write enable setup time (from $\overline{\text{WE}}$ falling edge to data valid).
- t_{WE} : Write enable hold time (from $\overline{\text{WE}}$ rising edge to data valid).
- t_{DS} : Data setup time (from data last change to $\overline{\text{RAS}}$ falling edge).
- t_{DH} : Data hold time (from $\overline{\text{RAS}}$ falling edge to data first change).
- t_{RC} : Row cycle time (from $\overline{\text{RAS}}$ falling edge to next $\overline{\text{RAS}}$ falling edge).
- t_{RP} : RAS precharge time (from $\overline{\text{RAS}}$ rising edge to next $\overline{\text{RAS}}$ falling edge).
- t_{CP} : CAS precharge time (from $\overline{\text{CAS}}$ rising edge to next $\overline{\text{CAS}}$ falling edge).
- t_{CSH} : CAS setup time (from $\overline{\text{CAS}}$ falling edge to data valid).
- t_{CHS} : CAS hold time (from data valid to $\overline{\text{CAS}}$ rising edge).
- t_{CAS} : CAS access time (from $\overline{\text{CAS}}$ falling edge to data valid).
- t_{CAS} : CAS to RAS delay (from $\overline{\text{CAS}}$ falling edge to $\overline{\text{RAS}}$ falling edge).
- t_{RAD} : Row address strobe delay (from $\overline{\text{RAS}}$ falling edge to row address).
- t_{RAH} : Row address strobe hold time (from $\overline{\text{RAS}}$ falling edge to row address).
- t_{ASC} : Column address strobe delay (from $\overline{\text{CAS}}$ falling edge to column address).
- t_{CAH} : Column address strobe hold time (from $\overline{\text{CAS}}$ falling edge to column address).
- $t_{\text{I/O}}$: I/O setup time (from I/O last change to $\overline{\text{RAS}}$ falling edge).
- $t_{\text{I/O}}$: I/O hold time (from $\overline{\text{RAS}}$ falling edge to I/O first change).

Fast Page Mode Read Cycle



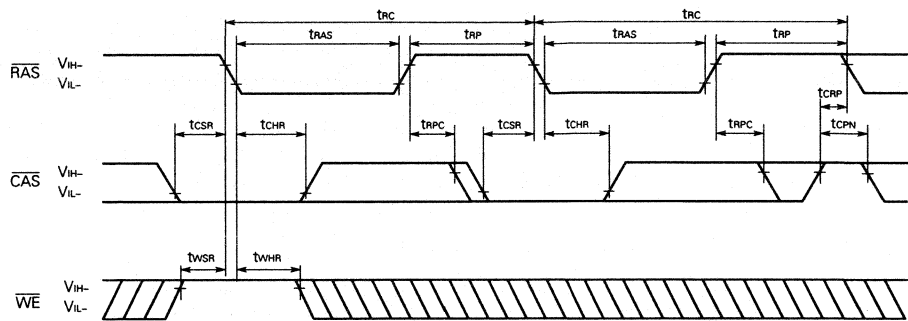
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



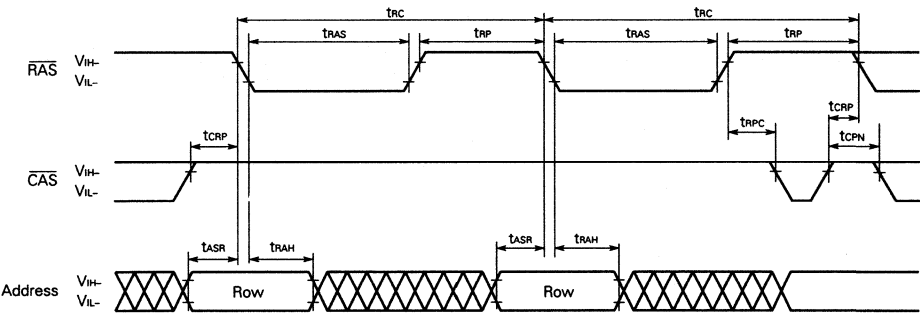
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



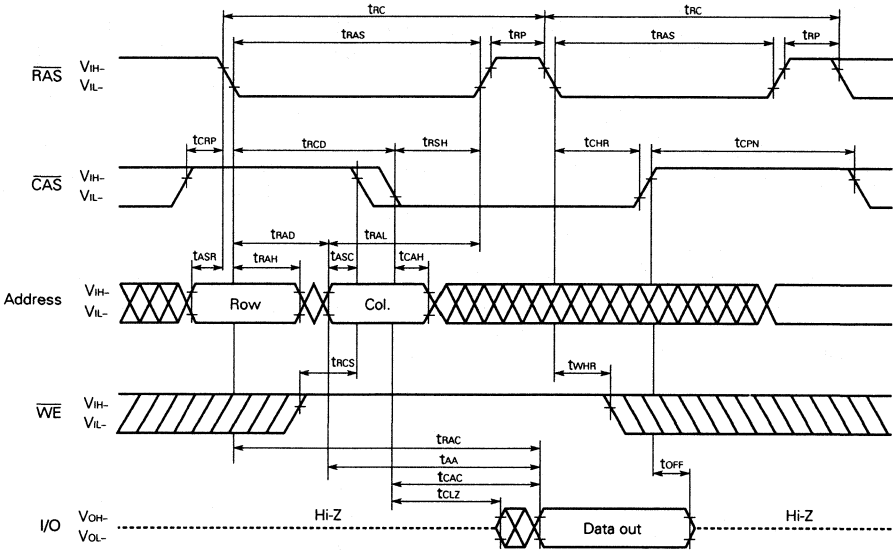
Remark Address: Don't care I/O: Hi-Z

RAS Only Refresh Cycle



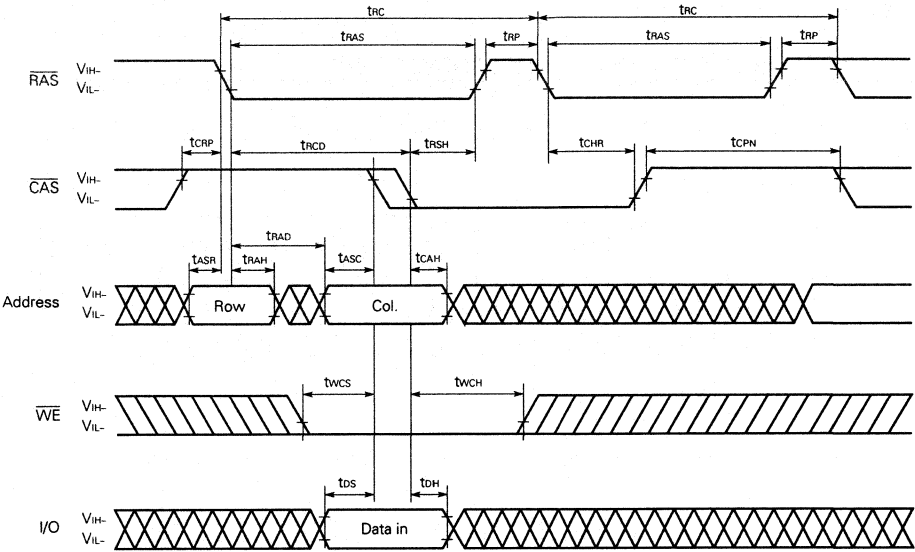
Remark WE: Don't care I/O: Hi-Z

★ Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

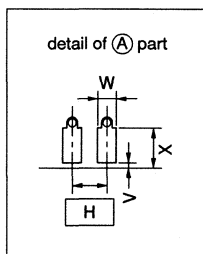
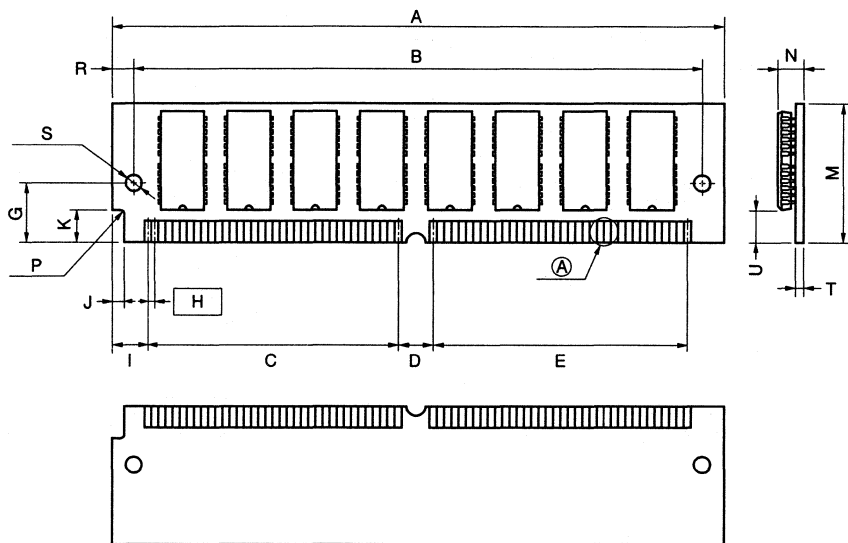
★



Package Drawings

[MC-424000A32B, 424000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



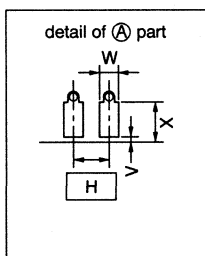
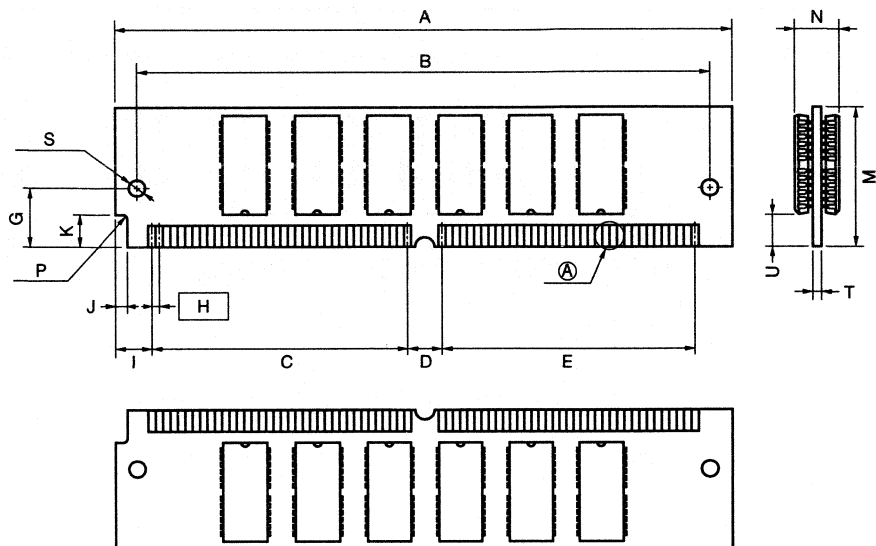
ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	3.984 ^{+0.005} _{-0.006}
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
R	3.38±0.13	0.133 ^{+0.006} _{-0.005}
S	φ3.18	φ0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A54

[MC-424000A36BE, 424000A36FE]

★

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)

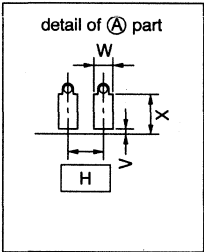
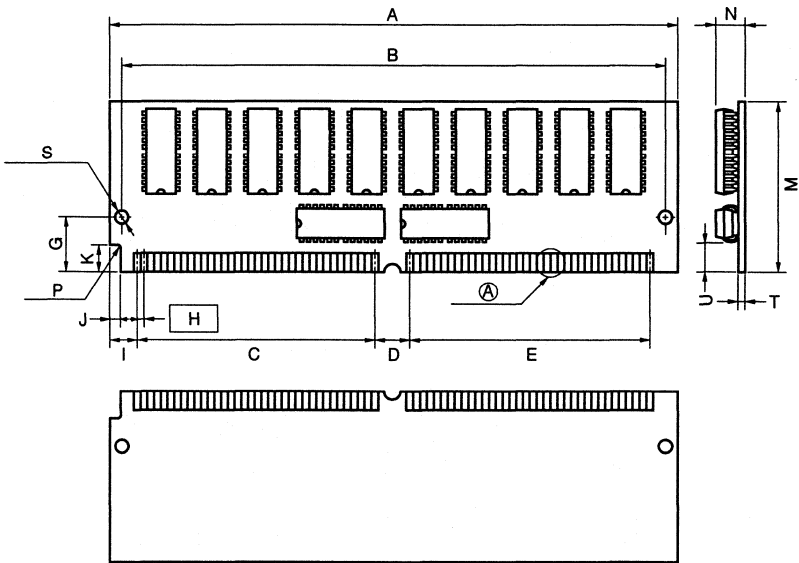


ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	φ3.18	φ0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	5.08 MIN.	0.200 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

M72B-50A47

★ [MC-424000A36BJ, 424000A36FJ]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
S	φ3.18	φ0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

M72B-50A51-1

MOS INTEGRATED CIRCUIT

MC-422000AA40 SERIES

2 M-WORD BY 40-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-422000AA40 series is a 2 097 152 words by 40 bits dynamic RAM module on which 20 pieces of 4 M bits CMOS Dynamic RAM (μ PD424400LA SOJ) are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Features

- 2 097 152 words by 40 bits organization
- Fast access and cycle time

Family	Access time ns (MAX.)	R/W cycle time ns (MIN.)	Power consumption mW (MAX.)	
			Active	Standby
MC-422000AA40-60	60	120	6 615	105
MC-422000AA40-70	70	140	5 565	105
MC-422000AA40-80	80	160	5 040	105
MC-422000AA40-10	100	190	4 515	105



- Fast page mode.
- 1 024 refresh cycles / 16 ms.
- Three refresh methods can be applied :
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- 72-pin single in-line memory module package (Pin pitch = 1.27 mm).
- 40-bit simultaneous switching.
- Output buffers control : $\overline{\text{OE}}$ pin.
- All inputs and outputs TTL compatible.
- Single +5 V $\pm$ 5 % power supply.
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3).

The information in this document is subject to change without notice.



Ordering Information

Part number	Access time ns (MAX.)	Package	Mounted device
MC-422000AA40B-60	60	72-pin Single In-line Memory Module (Pluggable type) (Edge connector : Solder coating (HAL))	μPD424400LA 300 mil SOJ×20 (Double sides)
MC-422000AA40B-70	70		
MC-422000AA40B-80	80		
MC-422000AA40B-10	100		
MC-422000AA40F-60	60	72-pin Single In-line Memory Module (Pluggable type) (Edge connector : Gold plating)	
MC-422000AA40F-70	70		
MC-422000AA40F-80	80		
MC-422000AA40F-10	100		

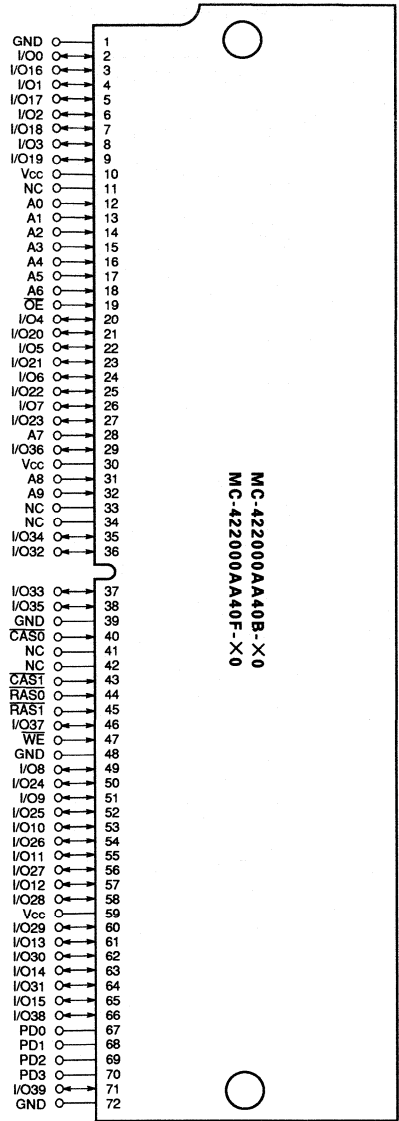
Quality Grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration (Marking Side)

72-pin Single In-line Memory Module Pluggable Type (Solder Coating, Gold Plating)

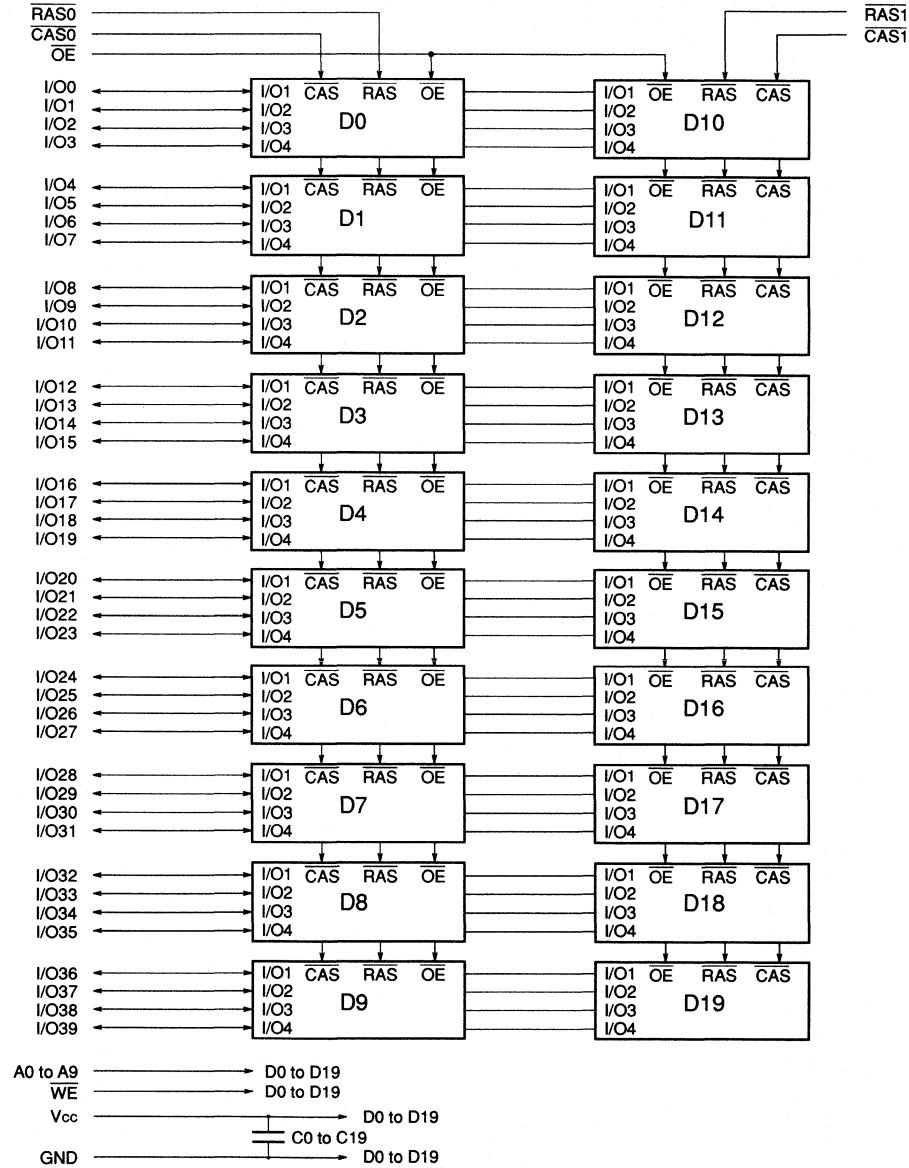


- A0 to A9 : Address Inputs
- I/O0 to I/O39 : Data Inputs/Outputs
- CAS0, CAS1 : Column Address Strobe
- RAS0, RAS1 : Row Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : +5 V Power Supply
- GND : Ground
- NC : No Connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	NC	NC	NC	NC
PD1	68	NC	NC	NC	NC
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

Block Diagram



Remark D0 to D19 : μ PD424400LA

Electrical Specifications **Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		20	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions NOTE1, 2

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A9			110	pF
	C_{I2}	$\overline{WE}$, $\overline{OE}$			130	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS1}$			60	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS1}$			60	
Data Input/Output capacitance	C_D	I/O0 to I/O39			20	pF

★ DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Note
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 260	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	1 060		
			$t_{\text{RAC}} = 80 \text{ ns}$	960		
			$t_{\text{RAC}} = 100 \text{ ns}$	860		
Standby current	I _{CC2}	$V_{\text{IH(MIN.)}} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$		40	mA	
		$V_{\text{CC}} - 0.2 \text{ V} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$		20		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $V_{\text{IH(MIN.)}} \leq \overline{\text{CAS}}$ $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 260	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	1 060		
			$t_{\text{RAC}} = 80 \text{ ns}$	960		
			$t_{\text{RAC}} = 100 \text{ ns}$	860		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{CAS}}$ Cycling $\overline{\text{RAS}} \leq V_{\text{IL(MAX.)}}$ $t_{\text{PC}} = t_{\text{PC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	960	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	860		
			$t_{\text{RAC}} = 80 \text{ ns}$	760		
			$t_{\text{RAC}} = 100 \text{ ns}$	660		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 260	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	1 060		
			$t_{\text{RAC}} = 80 \text{ ns}$	960		
			$t_{\text{RAC}} = 100 \text{ ns}$	860		
Input leakage current	I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ all other pins except for testing pin = 0 V	-200	+200	μA	
Output leakage current	I _{O(L)}	I/O0 to I/O39 are disabled (Hi-Z) $V_o = 0 \text{ to } 5.5 \text{ V}$	-20	+20	μA	
Output high voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Output low voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	

AC Characteristics

(Recommended Operating Conditions unless otherwise noted) Note 5, 6

(1/2)



Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	120		140		160		190		ns	7
Read Write Cycle Time	t _{RWC}	165		185		210		250		ns	7
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40		45		50		60		ns	7
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	85		90		100		120		ns	7
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80		100	ns	8, 9
Access Time from $\overline{\text{CAS}}$ (Falling Edge)	t _{CAC}		15		20		20		25	ns	8, 9
Access Time from Column Address	t _{AA}		30		35		40		50	ns	8, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45		55	ns	9
Access Time from $\overline{\text{OE}}$	t _{OEA}		20		20		20		25	ns	9
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	17	50	ns	8
$\overline{\text{CAS}}$ -Data Setup Time	t _{CLZ}	0		0		0		0		ns	9
$\overline{\text{OE}}$ -Data Setup Time	t _{OLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay ($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	15	0	20	0	25	ns	10
$\overline{\text{OE}}$ -Data Delay Time	t _{OED}	15		15		20		25		ns	
Output Buffer Turn-off Delay ($\overline{\text{OE}}$)	t _{OEZ}	0	15	0	15	0	20	0	25	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	0		0		0		0		ns	
$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ inactive Setup Time	t _{OES}	0		0		0		0		ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	50		60		70		80		ns	
$\overline{\text{RAS}}$ Pulse Width (Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20		20		20		25		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		100		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	25	75	ns	8
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		10		10		ns	11
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		10		10		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		12		ns	



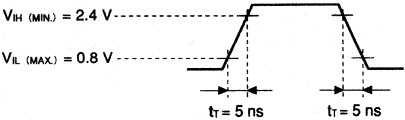
(2/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Column Address Setup Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		50		ns	
Read Command Setup Time	t _{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		0		ns	12
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		15		20		ns	13
Write Command Pulse Width	t _{WP}	15		15		15		20		ns	13
Data-in Setup Time	t _{DS}	0		0		0		0		ns	14
Data-in Hold Time	t _{DH}	15		15		15		20		ns	14
$\overline{\text{WE}}$ Command Setup Time	t _{WCS}	0		0		0		0		ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	40		40		45		55		ns	15
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	80		90		105		130		ns	15
$\overline{\text{CAS}}$ Precharge Delay Time Referenced to $\overline{\text{WE}}$ (Fast Page Mode)	t _{CPWD}	60		60		70		85		ns	15
Column Address Delay Time Referenced to $\overline{\text{WE}}$	t _{AWD}	50		55		65		80		ns	15
Write Command Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20		20		20		25		ns	
Write Command Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15		15		15		20		ns	
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	t _{CSR}	10		10		10		10		ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	t _{CHR}	15		15		15		20		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		20		ns	
Refresh Time	t _{REF}		16		16		16		16	ms	

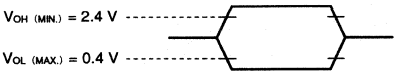
Note

- 1. All voltages are referenced to GND.
- 2. An initial pause of 100 μ s is required after power up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles are required.
- 3. Icc1 , Icc3 , Icc4 , Icc5 , and Icc6 depend on t_{ac} and t_{pc} . Specified values are obtained with outputs open.
- 4. Address can be changed once or less while $\overline{\text{RAS}} = \text{VIL}$ and $\overline{\text{CAS}} = \text{VIH}$.
- 5. AC measurements assume $t_{\text{T}} = 5 \text{ ns}$.
- 6. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



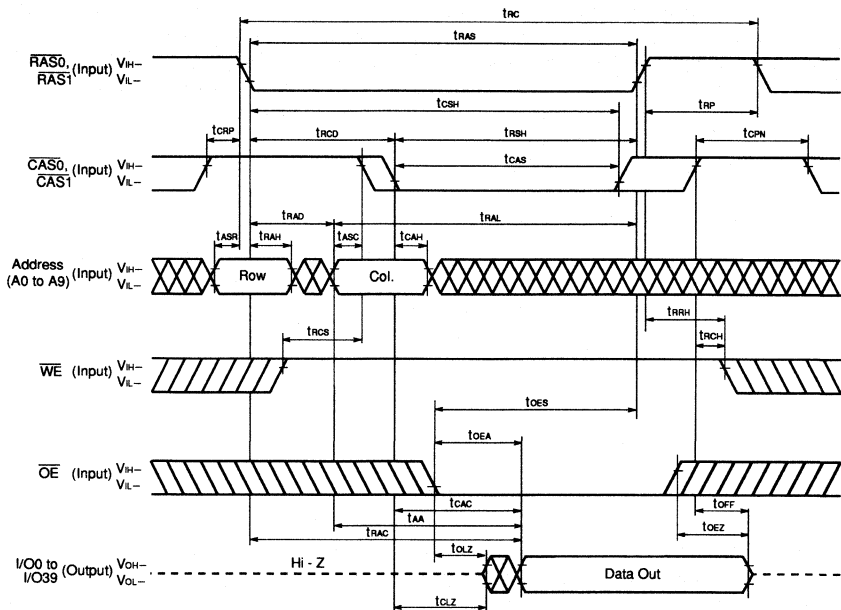
- 7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_{\text{a}} = 0 \text{ to } 70 \text{ }^{\circ}\text{C}$) is assured.
- 8. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

CONDITION	ACCESS TIME
$t_{\text{RAD}} \leq t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD (MAX.)}}$	$t_{\text{RAC (MAX.)}}$
$t_{\text{RAD (MAX.)}} \leq t_{\text{RAD}}$ and $t_{\text{RCD}} \leq t_{\text{RCD (MAX.)}}$	$t_{\text{AA (MAX.)}}$
$t_{\text{RCD (MAX.)}} \leq t_{\text{RCD}}$	$t_{\text{CAC (MAX.)}}$

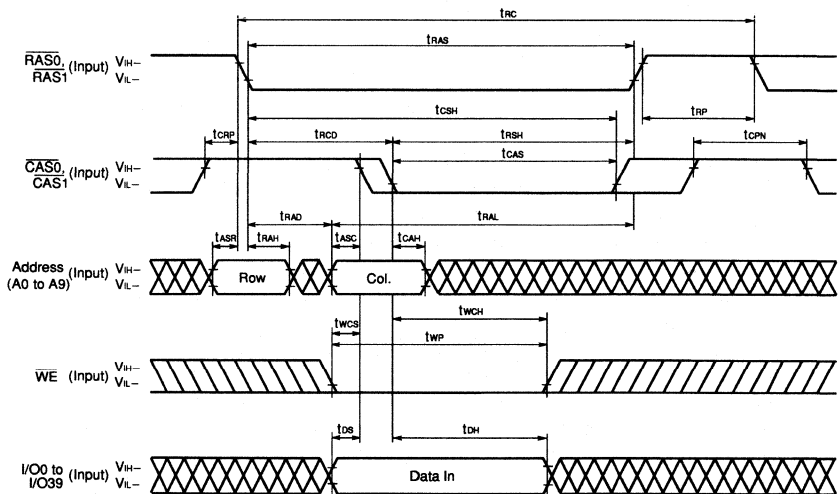
$t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD (MAX.)}}$ indicate the points which the access time changes and are not the limits of operation.

- 9. Loading conditions are 2 TTL and 100 pF.
- 10. $t_{\text{OFF (MAX.)}}$ and $t_{\text{OEZ (MAX.)}}$ define the time at which the output achieves the open circuit condition and are not referenced to VOH or VOL .
- 11. $t_{\text{CRP (MIN.)}}$ requirement should be applicable for $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycles preceded by any cycles.
- 12. Either $t_{\text{RCH (MIN.)}}$ or $t_{\text{RRH (MIN.)}}$ must be satisfied for a read cycle.
- 13. $t_{\text{WP (MIN.)}}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{\text{WCH (MIN.)}}$ should be satisfied.
- 14. This specification is referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{WE}}$ falling edge in late write or read modify write cycles.
- 15. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS (MIN.)}} \leq t_{\text{WCS}}$, the cycle is an early write cycle and the data out pins will remain Hi-Z through the entire cycle. If $t_{\text{RWD (MIN.)}} \leq t_{\text{RWD}}$, $t_{\text{CWD (MIN.)}} \leq t_{\text{CWD}}$, $t_{\text{AWD (MIN.)}} \leq t_{\text{AWD}}$ and $t_{\text{CPWD (MIN.)}} \leq t_{\text{CPWD}}$, the cycle is a read modify write cycle and condition of the data out (at access time) is indeterminate.

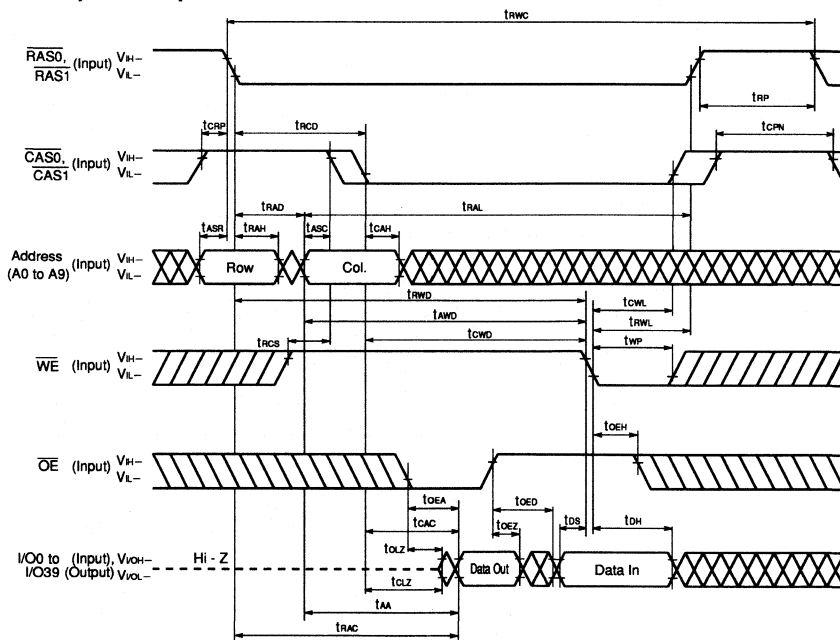
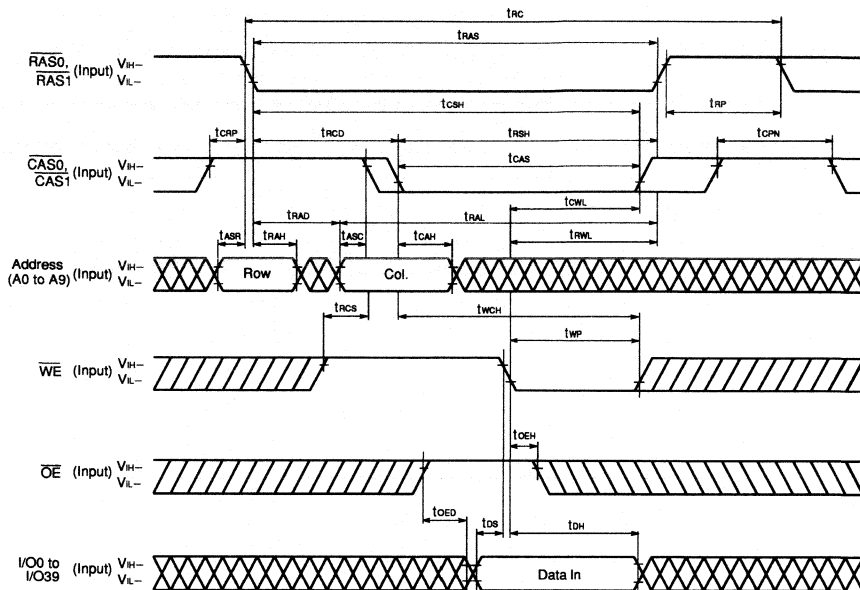
Read Cycle



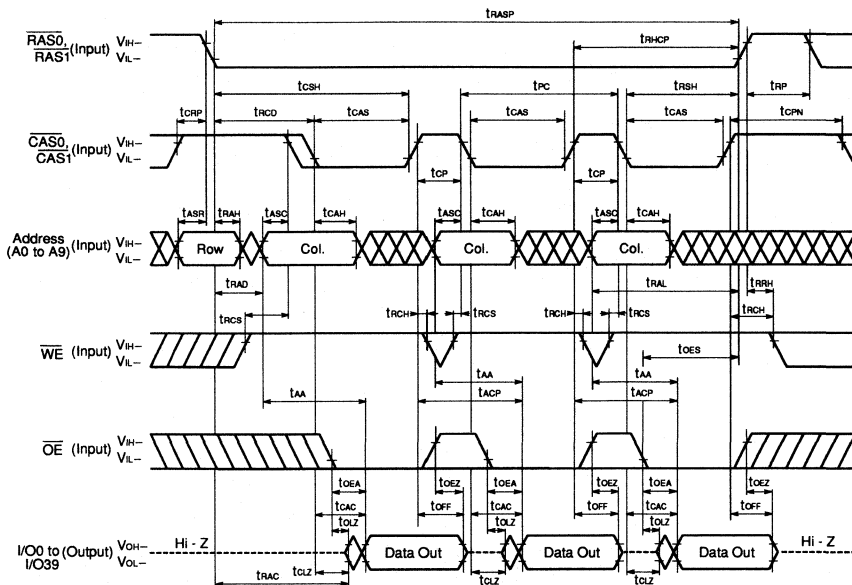
Early Write Cycle



Remark $\overline{OE}$ = Don't Care

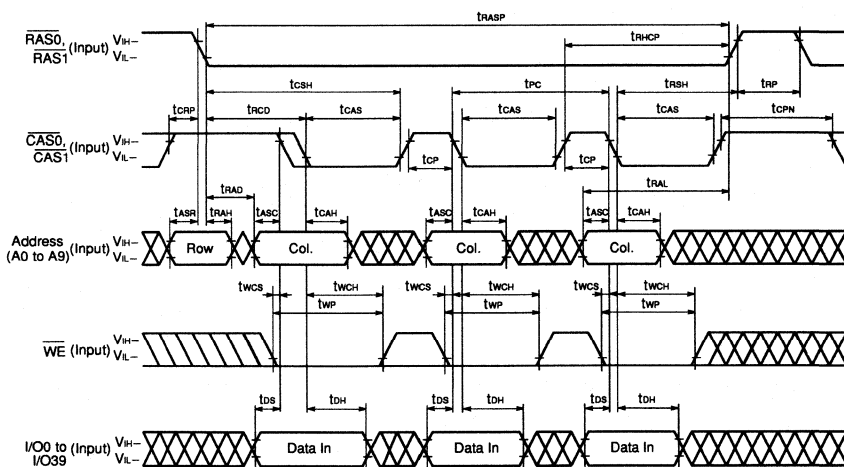


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

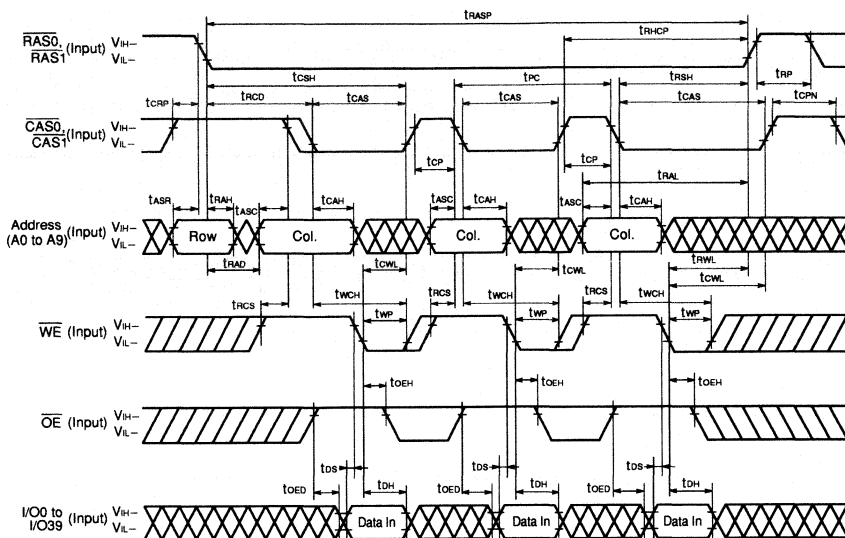
Fast Page Mode Early Write Cycle



Remark $\overline{OE} = \text{Don't Care}$

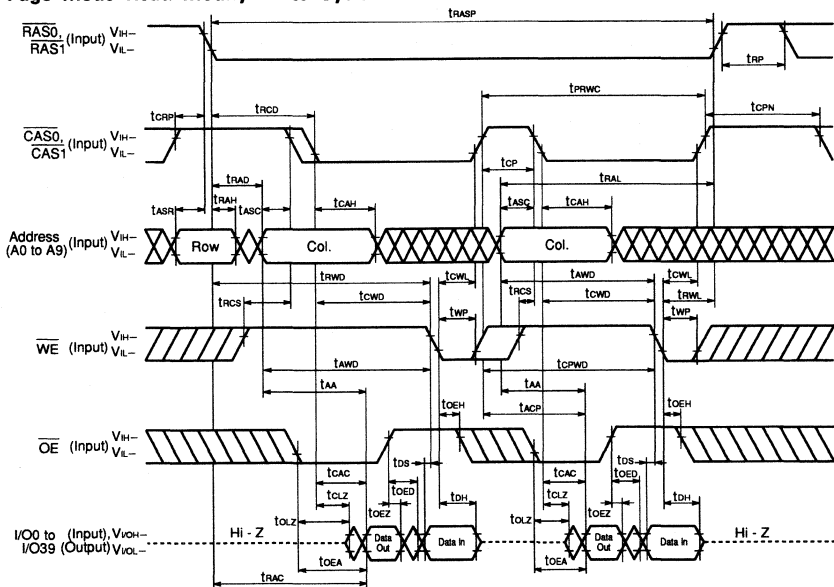
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Late Write Cycle



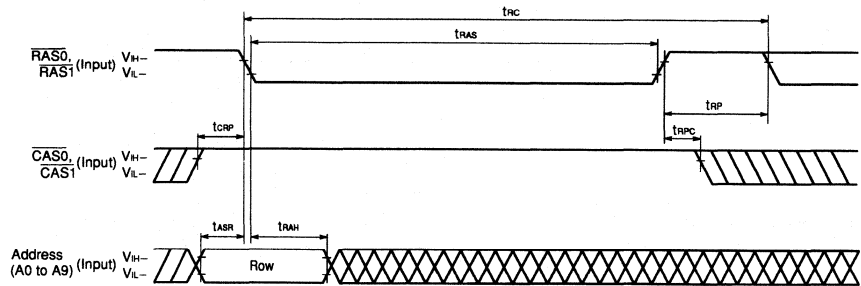
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Read Modify Write Cycle



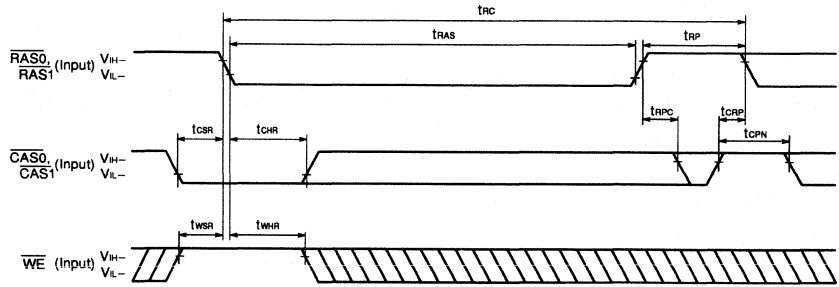
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

RAS Only Refresh Cycle



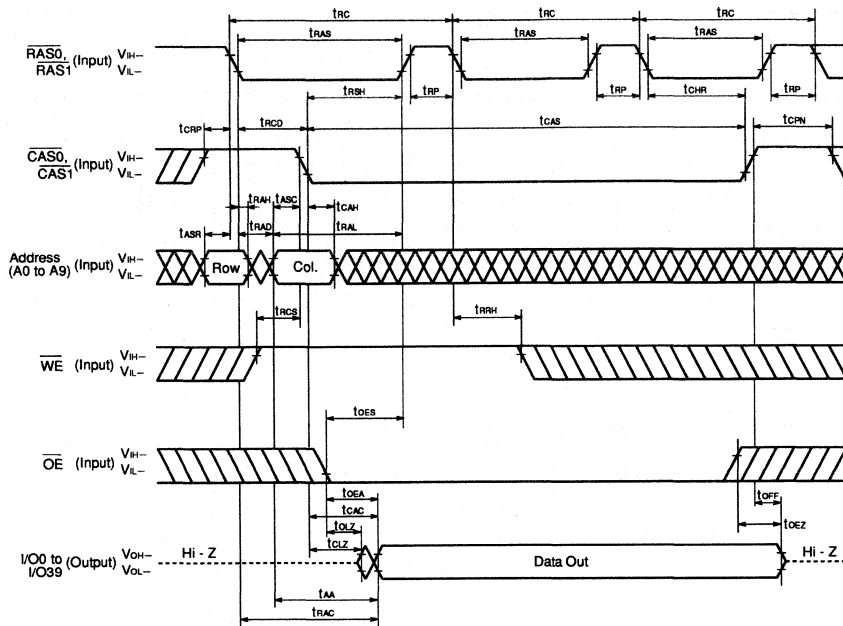
Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$ = Don't care I/O0 to I/O39 = Hi - Z

CAS Before RAS Refresh



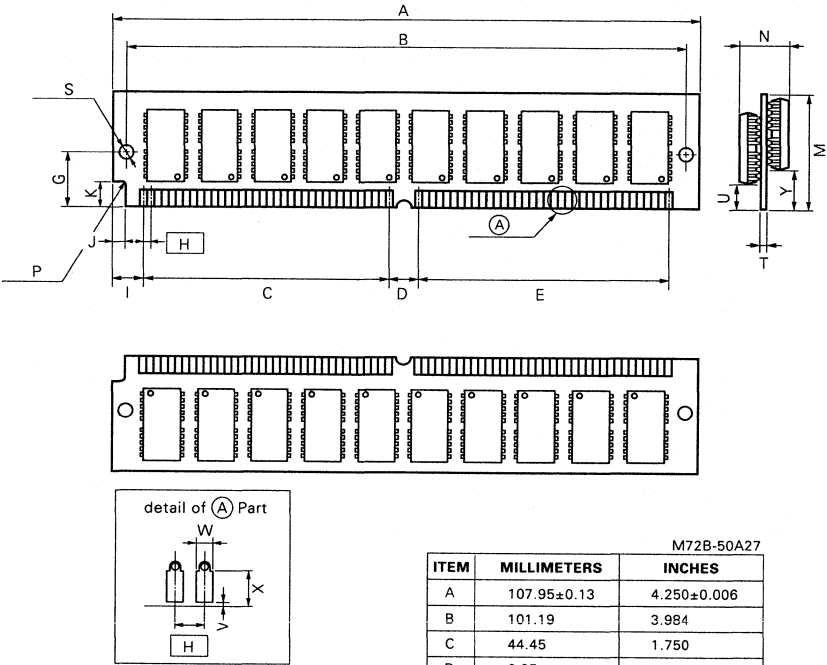
Remark Address (A0 to A9), $\overline{\text{OE}}$ = Don't care I/O0 to I/O39 = Hi - Z

Hidden Refresh Cycle



Package Drawing

72 PIN SINGLE IN-LINE MODULE (Pluggable Type)



M72B-50A27

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R 2.0	R 0.079
S	Ø3.18	Ø0.125
T	1.27 ^{+0.10} _{-0.08}	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	5.71 MIN.	0.224 MIN.

MOS INTEGRATED CIRCUIT

MC-422000A32, 422000A36 SERIES

2 M-WORD BY 32-BIT, 2 M-WORD BY 36-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-422000A32 series is a 2 097 152 words by 32 bits dynamic RAM module on which 16 pieces of 4 M DRAM (μ PD424400) are assembled.

The MC-422000A36 series is a 2 097 152 words by 36 bits dynamic RAM module on which 16 pieces of 4 M DRAM (μ PD424400) and 8 pieces of 1 M DRAM (μ PD421000) are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2 097 152 words by 32 bits organization (MC-422000A32 series)
- 2 097 152 words by 36 bits organization (MC-422000A36 series)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000A32-60	60 ns	120 ns	5 355 mW	84 mW
MC-422000A32-70	70 ns	140 ns	4 515 mW	
MC-422000A32-80	80 ns	160 ns	4 095 mW	
MC-422000A32-10	100 ns	190 ns	3 675 mW	
MC-422000A36-60	60 ns	120 ns	6 825 mW	126 mW
MC-422000A36-70	70 ns	140 ns	6 195 mW	
MC-422000A36-80	80 ns	160 ns	5 565 mW	
MC-422000A36-10	100 ns	190 ns	4 935 mW	

- 1 024 refresh cycles/16 ms
- Three refresh modes are available: $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- All inputs and outputs are TTL compatible
- Single +5.0 V $\pm$ 5 % power supply
- Access time can be distinguished with characteristics of PD-pins(PD0 to PD3)

The information in this document is subject to change without notice.

The mark ★ shows revised points.

★ Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	16 pieces of μ PD424400LA (300 mil SOJ) [Double side]
MC-422000A32B-70	70 ns		
MC-422000A32B-80	80 ns		
MC-422000A32B-10	100 ns		
MC-422000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-422000A32F-70	70 ns		
MC-422000A32F-80	80 ns		
MC-422000A32F-10	100 ns		
MC-422000A36B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	16 pieces of μ PD424400LA (300 mil SOJ) 8 pieces of μ PD421000GX (6 mm×16 mm TSOP (I)) [Double side]
MC-422000A36B-70	70 ns		
MC-422000A36B-80	80 ns		
MC-422000A36B-10	100 ns		
MC-422000A36F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-422000A36F-70	70 ns		
MC-422000A36F-80	80 ns		
MC-422000A36F-10	100 ns		
MC-422000A36BK-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	16 pieces of μ PD424400LA (300 mil SOJ) 8 pieces of μ PD421000LA (300 mil SOJ) [Double side]
MC-422000A36BK-70	70 ns		
MC-422000A36BK-80	80 ns		
MC-422000A36BK-10	100 ns		
MC-422000A36FK-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-422000A36FK-70	70 ns		
MC-422000A36FK-80	80 ns		
MC-422000A36FK-10	100 ns		

Quality Grade

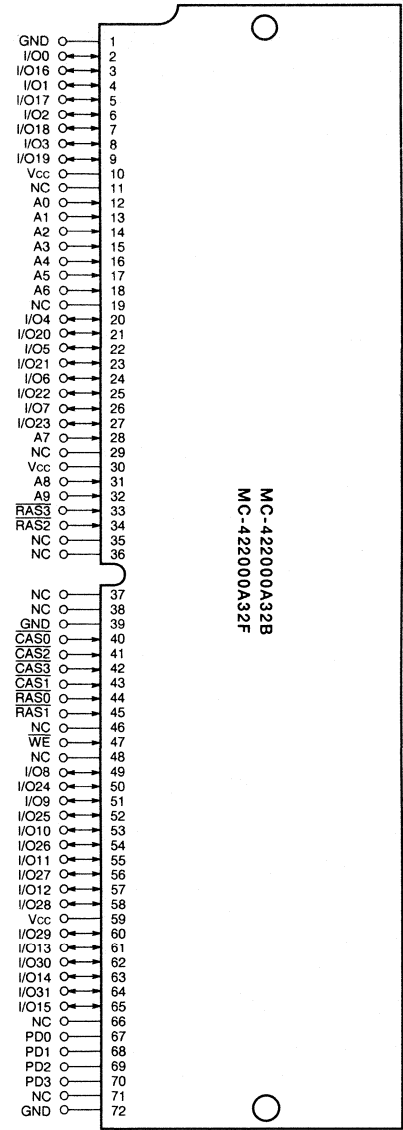
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Front view)

[MC-422000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



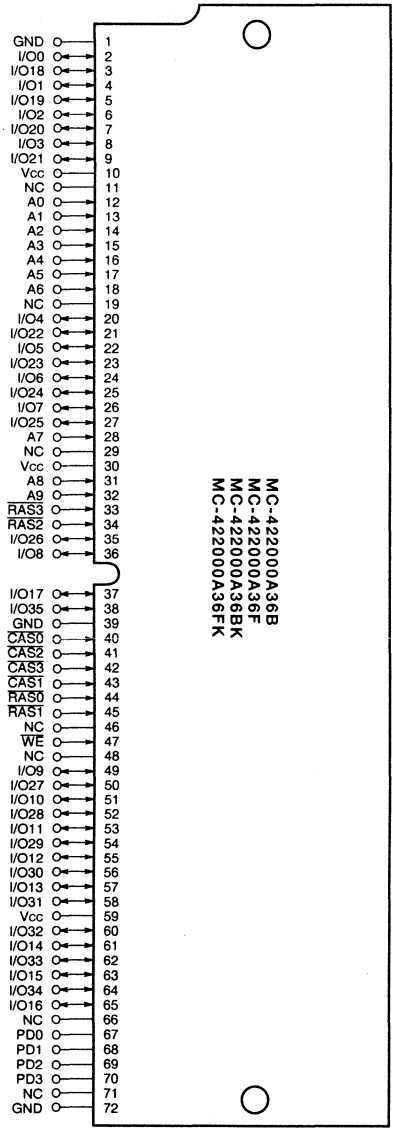
- A0-A9 : Address Inputs
I/O0-I/O31 : Data Inputs/Outputs
CAS0-CAS3 : Column Address Strobe
RAS0-RAS3 : Row Address Strobe
WE : Write Enable
Vcc : Power Supply
GND : Ground
NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	NC	NC	NC	NC
PD1	68	NC	NC	NC	NC
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

[MC-422000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



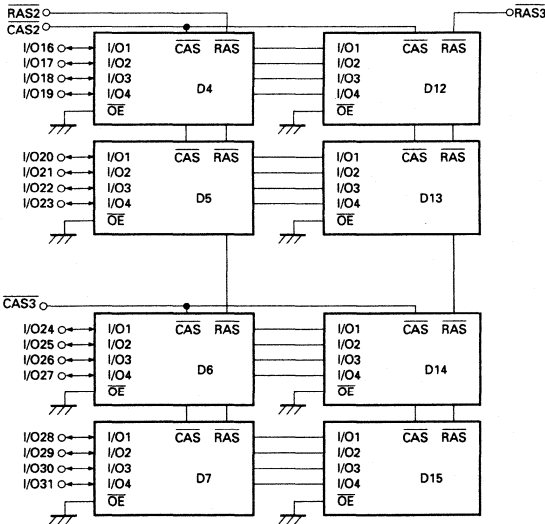
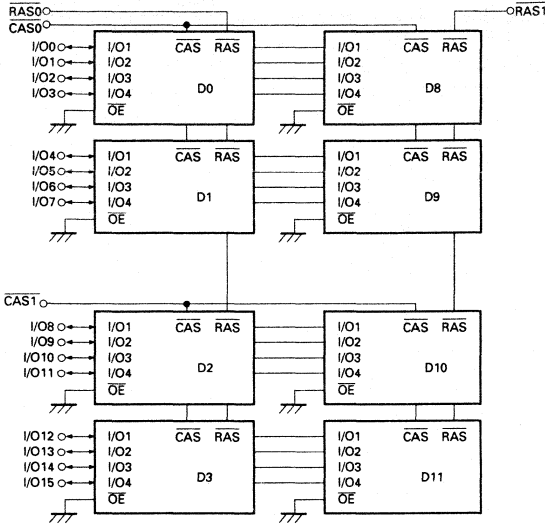
- A0-A9 : Address Inputs
- I/O0-I/O35 : Data Inputs/Outputs
- CAS0-CAS3 : Column Address Strobe
- RAS0-RAS3 : Row Address Strobe
- WE : Write Enable
- Vcc : Power Supply
- GND : Ground
- NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin	Pin	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	NC	NC	NC	NC
PD1	68	NC	NC	NC	NC
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

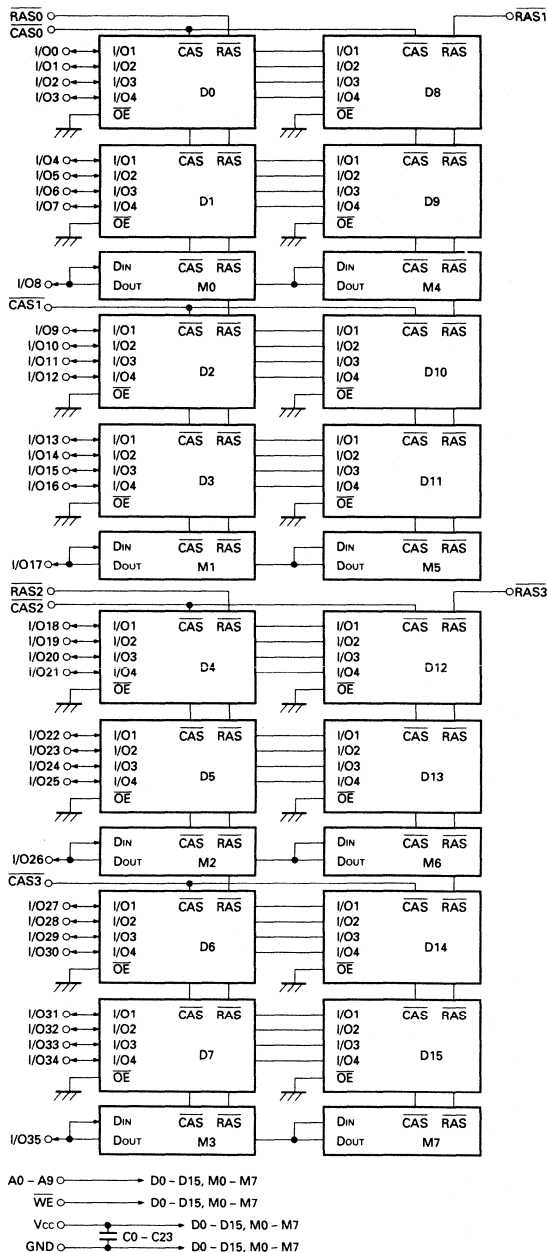
Block Diagrams

[MC-422000A32 series]



A0 - A9 → D0 - D15
 WE → D0 - D15
 Vcc → D0 - D15
 GND → D0 - D15

[MC-422000A36 series]



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-422000A32	16	W
		MC-422000A36	24	
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance ($T_a = +25^\circ\text{C}$, $f = 1\text{ MHz}$)

[MC-422000A32 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			121	pF
	C_{I2}	$\overline{WE}$			137	
	C_{I3}	$\overline{RAS0} - \overline{RAS3}$			48	
	C_{I4}	$\overline{CAS0} - \overline{CAS3}$			48	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

[MC-422000A36 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			161	pF
	C_{I2}	$\overline{WE}$			193	
	C_{I3}	$\overline{RAS0} - \overline{RAS3}$			62	
	C_{I4}	$\overline{CAS0} - \overline{CAS3}$			62	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			29	pF
	$C_{I/O2}$	I/O8, I/O17, I/O26, I/O35			39	

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-422000A32 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 020	mA	3,4,7
			$t_{\text{RAC}} = 70 \text{ ns}$	860		
			$t_{\text{RAC}} = 80 \text{ ns}$	780		
			$t_{\text{RAC}} = 100 \text{ ns}$	700		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $I_O = 0 \text{ mA}$		32	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ $I_O = 0 \text{ mA}$		16		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 020	mA	3,4,5,7
			$t_{\text{RAC}} = 70 \text{ ns}$	860		
			$t_{\text{RAC}} = 80 \text{ ns}$	780		
			$t_{\text{RAC}} = 100 \text{ ns}$	700		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$, $\overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	780	mA	3,4,6
			$t_{\text{RAC}} = 70 \text{ ns}$	700		
			$t_{\text{RAC}} = 80 \text{ ns}$	620		
			$t_{\text{RAC}} = 100 \text{ ns}$	540		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 020	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	860		
			$t_{\text{RAC}} = 80 \text{ ns}$	780		
			$t_{\text{RAC}} = 100 \text{ ns}$	700		
Input leakage current	I _{I(L)}	$V_I = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	I/O0 to I/O31 is disabled (Hi-Z) $V_O = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V _{OH}	$I_O = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_O = +4.2 \text{ mA}$		0.4	V	

[MC-422000A36 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$	1 300	mA	3,4,7
			$\text{trac} = 70 \text{ ns}$	1 180		
			$\text{trac} = 80 \text{ ns}$	1 060		
			$\text{trac} = 100 \text{ ns}$	940		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$ $I_o = 0 \text{ mA}$		48	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC}-0.2 \text{ V}$ $I_o = 0 \text{ mA}$		24		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$	1 300	mA	3,4,5,7
			$\text{trac} = 70 \text{ ns}$	1 180		
			$\text{trac} = 80 \text{ ns}$	1 060		
			$\text{trac} = 100 \text{ ns}$	940		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{IL}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$	1 100	mA	3,4,6
			$\text{trac} = 70 \text{ ns}$	980		
			$\text{trac} = 80 \text{ ns}$	860		
			$\text{trac} = 100 \text{ ns}$	740		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$	1 300	mA	3,4
			$\text{trac} = 70 \text{ ns}$	1 180		
			$\text{trac} = 80 \text{ ns}$	1 060		
			$\text{trac} = 100 \text{ ns}$	940		
Input leakage current	I _{I(L)}	$V_I = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	I/O0 to I/O35 is disabled (Hi-Z) $V_O = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	

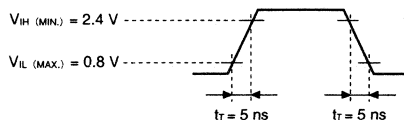
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter		Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Read or Write Cycle Time			t _{RC}	120		140		160		190		ns	
Fast Page Mode Cycle Time (Read or Write)			t _{PC}	40		45		50		60		ns	
Access Time from $\overline{\text{RAS}}$			t _{RAC}		60		70		80		100	ns	10,11
Access Time from $\overline{\text{CAS}}$ (Falling Edge)	MC-422000A32	t _{CAC}		15	20		20		25	ns	10,11		
	MC-422000A36			20									
Access Time from Column Address			t _{AA}		30		35		40		50	ns	10,11
Access Time from $\overline{\text{CAS}}$ Precharge			t _{ACP}		35		40		45		55	ns	11
RAS to Column Address Delay Time			t _{RAD}	15	30	15	35	17	40	17	50	ns	10
CAS to Data Setup Time			t _{CLZ}	0		0		0		0		ns	11
Output Buffer Turn-off Delay Time ($\overline{\text{CAS}}$)			t _{OFF}	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)			t _T	3	50	3	50	3	50	3	50	ns	
RAS Precharge Time			t _{RP}	50		60		70		80		ns	
RAS Pulse Width (Random Read, Write Cycle)			t _{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
RAS Pulse Width (Fast Page Mode)			t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
RAS Hold Time			t _{RSH}	20		20		20		25		ns	
CAS Pulse Width			t _{CAS}	20	10 000	20	10 000	20	10 000	25	10 000	ns	
CAS Hold Time			t _{CSH}	60		70		80		100		ns	
RAS to CAS Delay Time	MC-422000A32	t _{RCd}	20	40	20	50	25	60	25	90	ns	10	
	MC-422000A36									75			
CAS to RAS Precharge Time			t _{CRP}	10		10		10		10		ns	13
CAS Precharge Time			t _{CPN}	10		10		10		10		ns	
CAS Precharge Time (Fast Page Mode)			t _{CP}	10		10		10		10		ns	
RAS Precharge CAS Hold Time			t _{RPC}	10		10		10		10		ns	
RAS Hold Time from CAS Precharge			t _{RHCP}	35		40		45		55		ns	
Row Address Setup Time			t _{ASR}	0		0		0		0		ns	
Row Address Hold Time			t _{RAH}	10		10		12		12		ns	
Column Address Setup Time			t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	MC-422000A32	t _{CAH}	15		15	15	20		20		ns		
	MC-422000A36				17								
Column Address Lead Time Referenced to $\overline{\text{RAS}}$			t _{RAL}	30		35		40		50		ns	
Read Command Setup Time			t _{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to RAS			t _{RRH}	10		10		10		10		ns	14
Read Command Hold Time Referenced to CAS			t _{RCH}	0		0		0		0		ns	14
Write Command Hold Time Referenced to CAS			t _{WCH}	15		15		15		20		ns	15
Data-in Setup Time			t _{DS}	0		0		0		0		ns	16
Data-in Hold Time	MC-422000A32	t _{DH}	15		15	15	20		20		ns	16	
	MC-422000A36				20								
Write Command Setup Time			t _{WCS}	0		0		0		0		ns	17
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ before RAS Refresh			t _{CSR}	10		10		10		10		ns	
CAS Hold Time for CAS before RAS Refresh			t _{CHR}	15		15		15		20		ns	
WE Setup Time			t _{WSR}	10		10		10		10		ns	
WE Hold Time			t _{WHR}	15		15		15		20		ns	
Refresh Time			t _{REF}		16		16		16		16	ms	

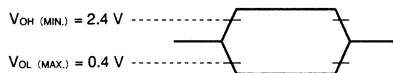
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on cycle rates (trc and trc).
4. Specified values are obtained with outputs unloaded.
5. Icc3 is measured assuming that all column address inputs are held at either high or low.
6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.).
8. AC measurements assume $\text{tr} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



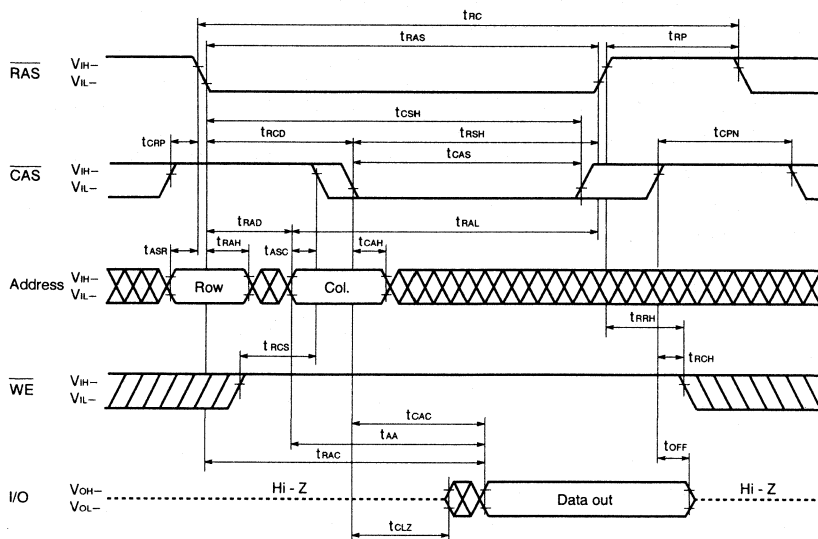
10. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD} (\text{MAX.})$, $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\text{trAD} > \text{trAD} (\text{MAX.})$, $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$	$\text{trAD} + \text{tAA} (\text{MAX.})$
$\text{trCD} > \text{trCD} (\text{MAX.})$	$\text{tCAC} (\text{MAX.})$	$\text{trCD} + \text{tCAC} (\text{MAX.})$

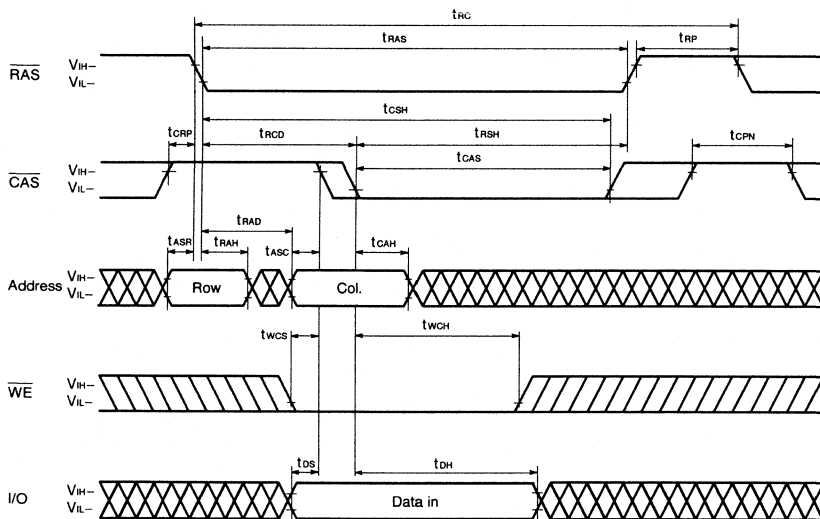
$\text{trAD} (\text{MAX.})$ and $\text{trCD} (\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD} (\text{MAX.})$ and $\text{trCD} \geq \text{trCD} (\text{MAX.})$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. $\text{tOFF} (\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $\text{tCRP} (\text{MIN.})$ requirement should be applied for $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycles preceded by any cycles.
14. Either $\text{trCH} (\text{MIN.})$ or $\text{trRH} (\text{MIN.})$ should be met in read cycles.
15. In early write cycles, $\text{twCH} (\text{MIN.})$ should be met.
16. $\text{tDS} (\text{MIN.})$ and $\text{tDH} (\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $\text{twCS} \geq \text{twCS} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

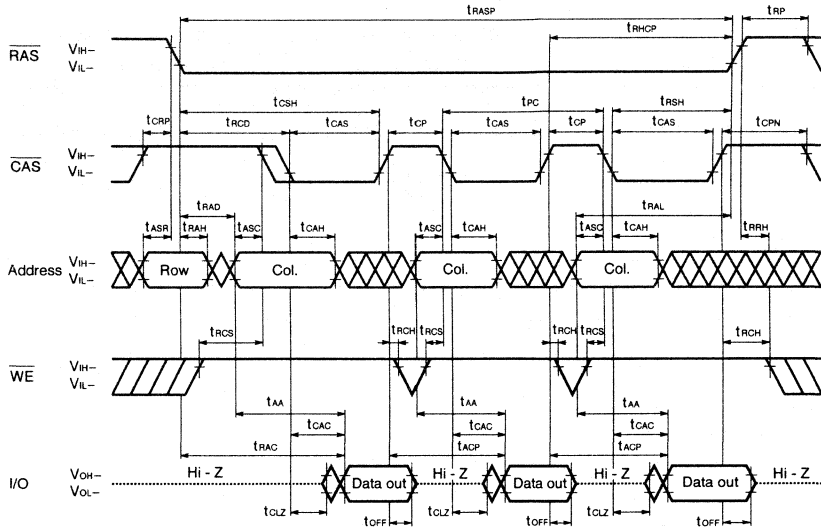
Read Cycle



Early Write Cycle

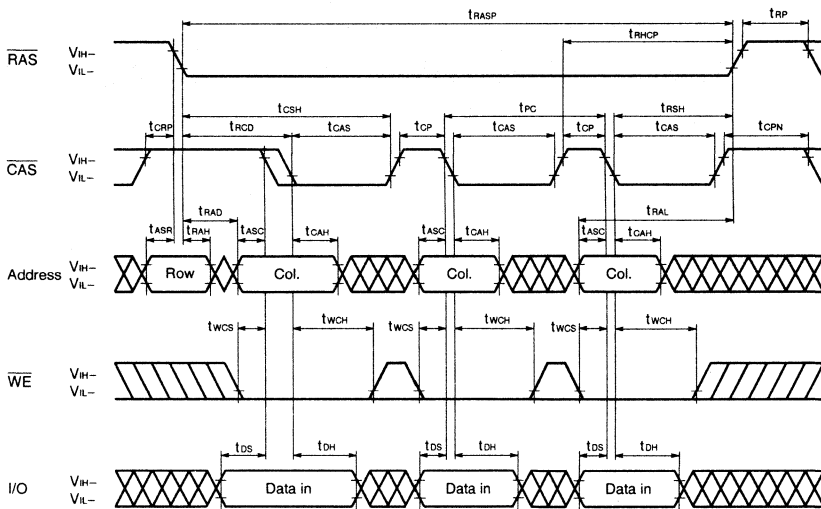


Fast Page Mode Read Cycle



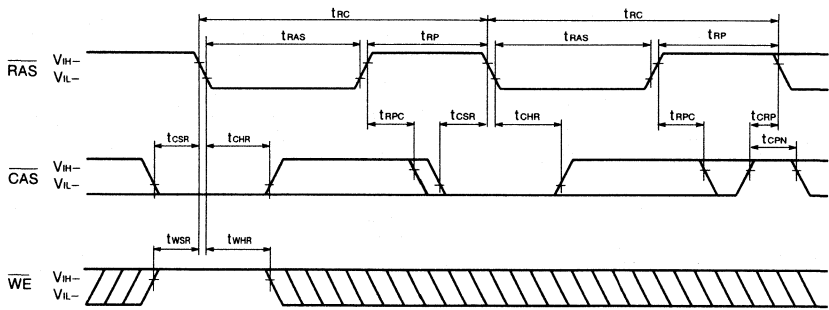
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



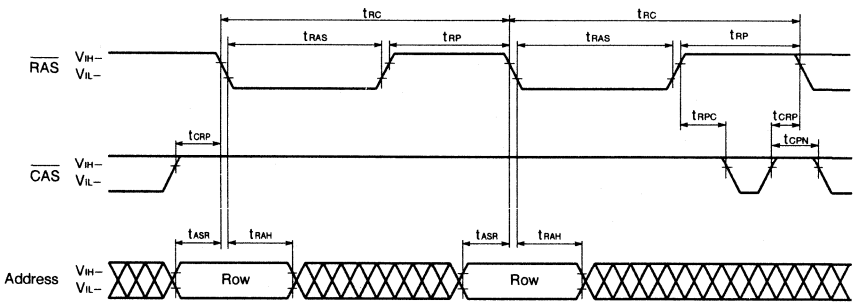
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



Remark Address = Don't care I/O = Hi - Z

RAS Only Refresh Cycle



Remark WE = Don't care I/O = Hi - Z

The timing diagram illustrates the relationship between the RAS, CAS, Address, WE, and I/O signals. Key timing parameters are labeled as follows:

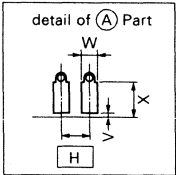
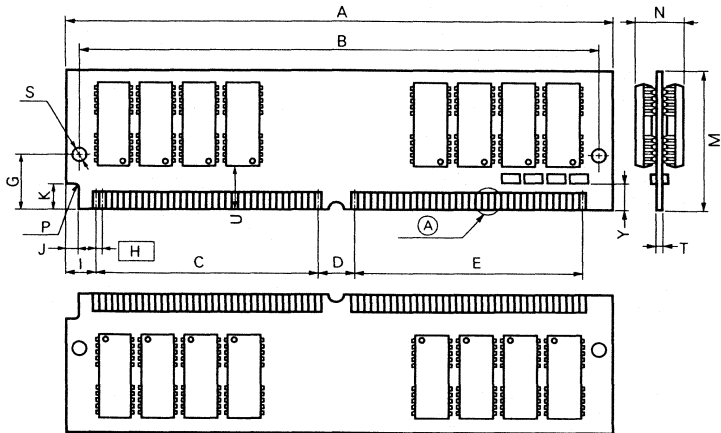
- RAS:** t_{RC} (RAS to data hold), t_{RAS} (RAS pulse width), t_{RP} (RAS to next RAS).
- CAS:** t_{CP} (CAS to data hold), t_{CD} (CAS to data setup), t_{CSH} (CAS to next CAS), t_{CAS} (CAS pulse width), t_{CHR} (CAS to data hold), t_{CPN} (CAS to next CAS).
- Address:** t_{ASR} (Address setup), t_{RAD} (Address to data), t_{RAH} (Address to data hold), t_{ASC} (Address to data setup), t_{CAH} (Address to data hold), t_{RAL} (Address to data).
- WE:** t_{RCS} (WE to data), t_{WHR} (WE to data hold), t_{OFF} (WE to data hold).
- I/O:** t_{AC} (Data out to data hold), t_{GLZ} (Data out to data hold), t_{AA} (Data out to data hold), t_{RAC} (Data out to data hold).



Package Drawings

MC-422000A32B, 422000A32F

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)

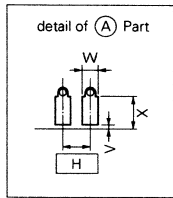
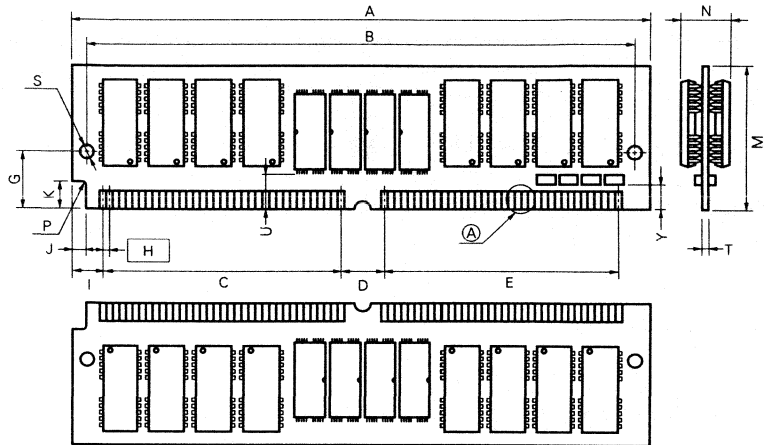


M72B-50A22-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R 2.0	R 0.079
S	Ø3.18	Ø0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	6.5 MIN.	0.255 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

MC-422000A36B, 422000A36F

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)

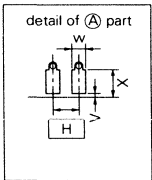
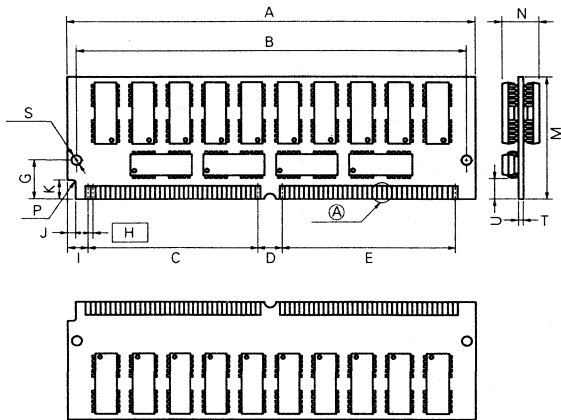


M72B-50A20-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.354 MAX.
P	R 2.0	R 0.079
S	φ3.18	φ0.125
T	1.27±0.08	0.050±0.004
U	5.32 MIN.	0.209 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

MC-422000A36BK, 422000A36FK

72PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



M72B-50A44

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	φ3.18	φ0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

MOS INTEGRATED CIRCUIT

MC-422000A32BA, 422000A32FA

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-422000A32BA, 422000A32FA are 2,097,152 words by 32 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μ PD4218160 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 32 bits organization
- Fast access and cycle time

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Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000A32-60	60 ns	110 ns	1,782 mW	22 mW (CMOS level input)
MC-422000A32-70	70 ns	130 ns	1,672 mW	
MC-422000A32-80	80 ns	150 ns	1,562 mW	

- 1,024 refresh cycles/16 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V $\pm$ 0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

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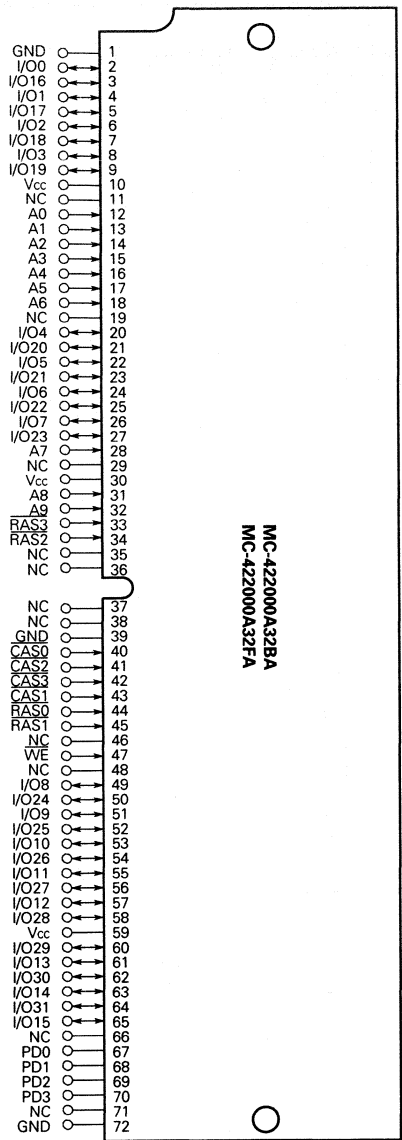
The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000A32BA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	4 pieces of μ PD4218160LE (400 mil SOJ) [Double side]
MC-422000A32BA-70	70 ns		
MC-422000A32BA-80	80 ns		
MC-422000A32FA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-422000A32FA-70	70 ns		
MC-422000A32FA-80	80 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

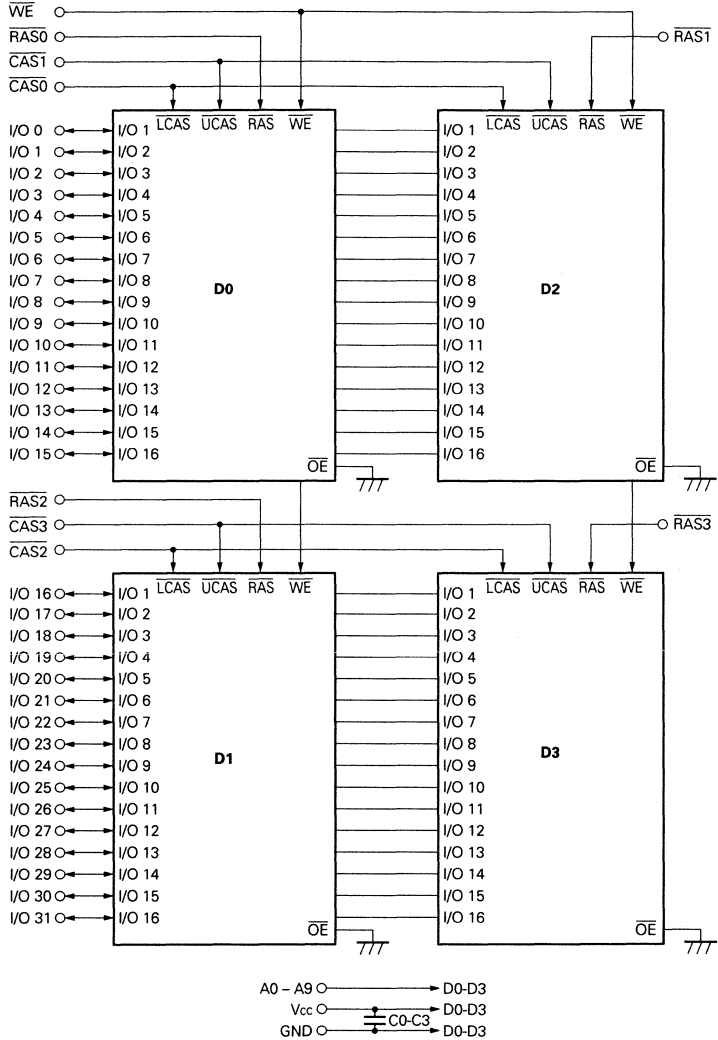


- A0 - A9 : Address Inputs
I/O0 - I/O31 : Data Inputs/Outputs
CAS0 - CAS3 : Column Address Strobe
RAS0 - RAS3 : Row Address Strobe
WE : Write Enable
Vcc : Power Supply
GND : Ground
NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

Block Diagram



Remark D0 - D3: μ PD4218160

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V _T		−1.0 to +7.0	V
Supply voltage	V _{CC}		−1.0 to +7.0	V
Output current	I _O		50	mA
Power dissipation	P _D		17	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{sig}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		4.5	5.0	5.5	V
High level input voltage	V _{IH}		2.4		V _{CC} + 1.0	V
Low level input voltage	V _{IL}		−1.0		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 - A9			40	pF
	C _{I2}	$\overline{WE}$			48	
	C _{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			22	
	C _{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output capacitance	C _{I/O}	I/O0 - I/O31			26	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}} (\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	324	mA	3, 4, 7
			$t_{\text{RAC}} = 70 \text{ ns}$	304		
			$t_{\text{RAC}} = 80 \text{ ns}$	284		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.})$ $I_O = 0 \text{ mA}$		8	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ $I_O = 0 \text{ mA}$		4		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}} (\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	324	mA	3, 4, 5, 7
			$t_{\text{RAC}} = 70 \text{ ns}$	304		
			$t_{\text{RAC}} = 80 \text{ ns}$	284		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}} (\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}} (\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	184	mA	3, 4, 6
			$t_{\text{RAC}} = 70 \text{ ns}$	164		
			$t_{\text{RAC}} = 80 \text{ ns}$	144		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}} (\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	324	mA	3, 4
			$t_{\text{RAC}} = 70 \text{ ns}$	304		
			$t_{\text{RAC}} = 80 \text{ ns}$	284		
Input leakage current	I _{I (L)}	$V_I = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O (L)}	$V_O = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage	V _{OH}	$I_O = -2.5 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_O = +2.1 \text{ mA}$		0.4	V	

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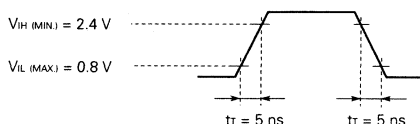
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t _{rac} = 60 ns		t _{rac} = 70 ns		t _{rac} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from RAS	t _{RA}		60		70		80	ns	10, 11
Access Time from CAS	t _{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from CAS Precharge	t _{ACP}		35		40		45	ns	11
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	t _{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{RP}	40		50		60		ns	
RAS Pulse Width	t _{RA}	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RA} SP	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	t _{RSH}	15		18		20		ns	
CAS Pulse Width	t _{CAS}	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	t _{CSH}	60		70		80		ns	
RAS to CAS Delay Time	t _{ACD}	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	t _{CRP}	5		5		5		ns	13
CAS Precharge Time	t _{CPN}	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
RAS Precharge CAS Hold Time	t _{RPC}	5		5		5		ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	35		40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to RAS	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	t _{RCH}	0		0		0		ns	14
WE Hold Time Referenced to CAS	t _{WCH}	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	t _{CSR}	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10		10		10		ns	
WE Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		16		16		16	ms	

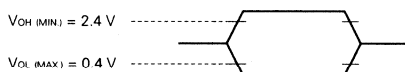
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.).
8. AC measurements assume $t_{\text{r}} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



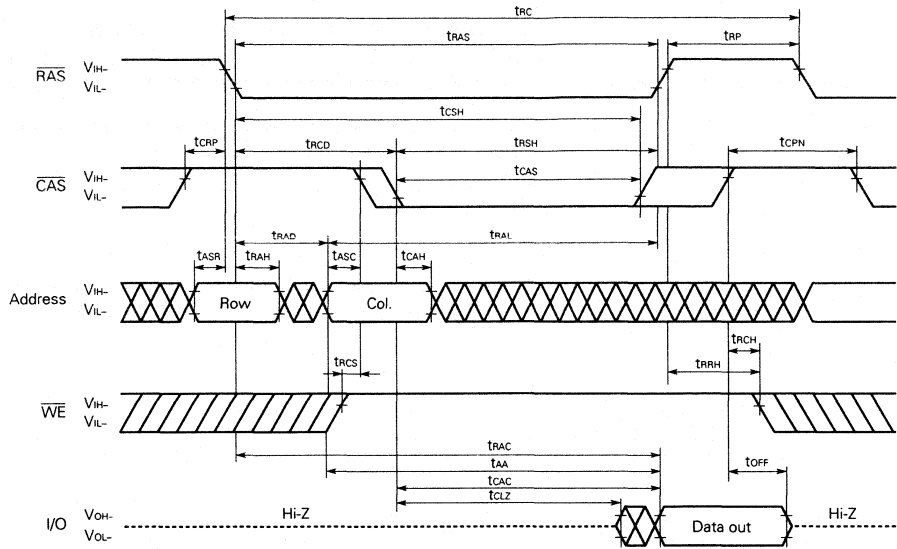
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX.})$	$t_{\text{RAC}} (\text{MAX.})$	$t_{\text{RAC}} (\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX.})$	$t_{\text{AA}} (\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}} (\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}} (\text{MAX.})$	$t_{\text{CAC}} (\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}} (\text{MAX.})$

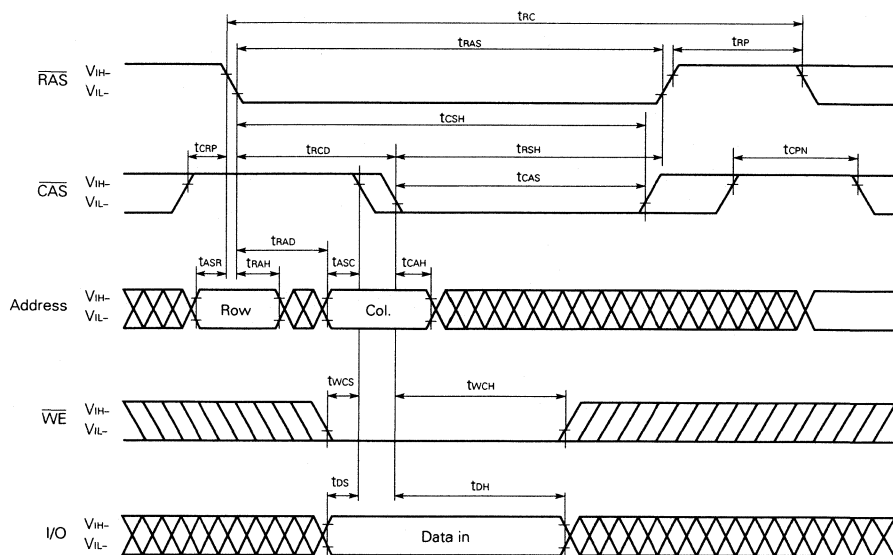
$t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} (\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{MAX.})$ will not cause any operation problems.

- ★ 11. Loading conditions are 1 TTL and 100 pF.
12. $t_{\text{OFF}} (\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $t_{\text{CRP}} (\text{MIN.})$ requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either $t_{\text{RCH}} (\text{MIN.})$ or $t_{\text{RRH}} (\text{MIN.})$ should be met in read cycles.
15. In early write cycles, $t_{\text{WCH}} (\text{MIN.})$ should be met.
16. $t_{\text{DS}} (\text{MIN.})$ and $t_{\text{DH}} (\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

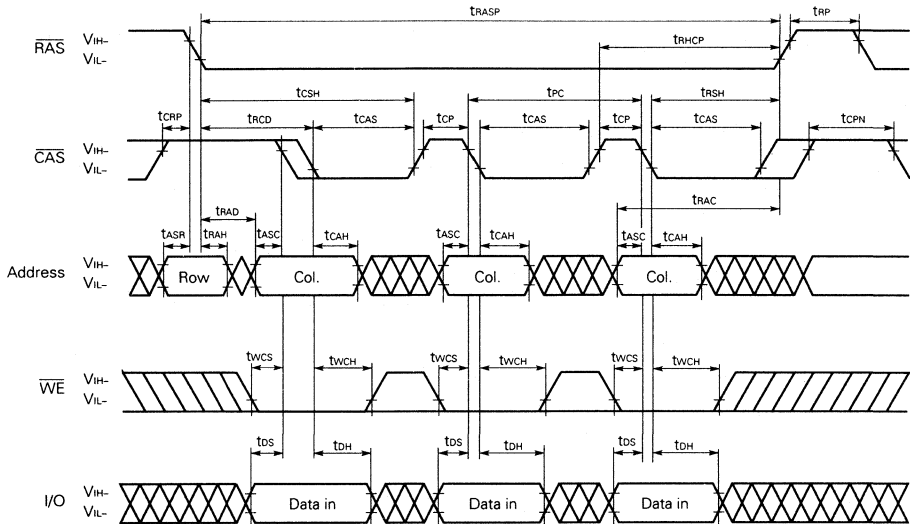
Read Cycle



Early Write Cycle

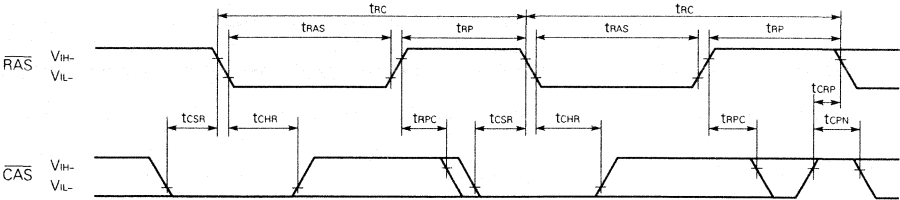


Fast Page Mode Early Write Cycle



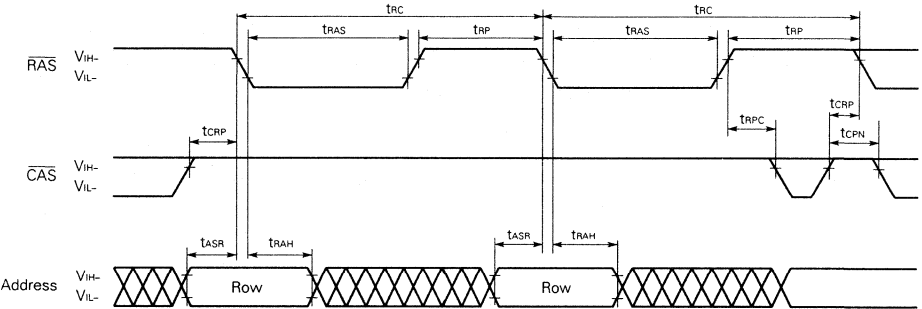
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



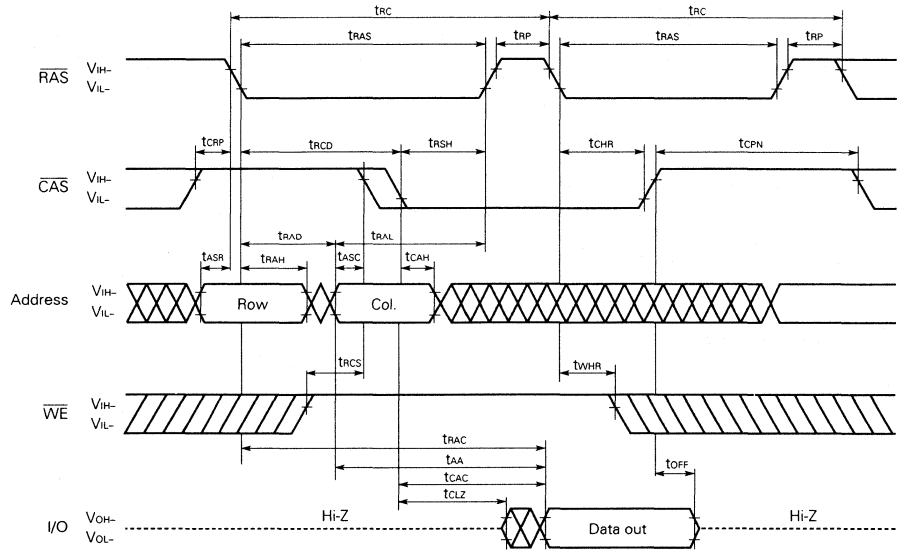
Remark Address, $\overline{WE}$: Don't care I/O: Hi-Z

RAS Only Refresh Cycle



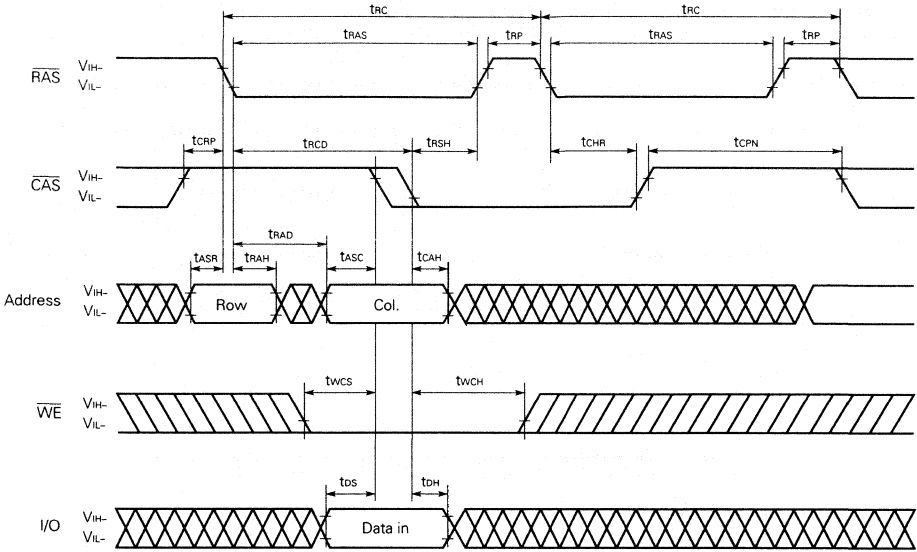
Remark $\overline{WE}$: Don't care I/O: Hi-Z

★ Hidden Refresh Cycle (Read)



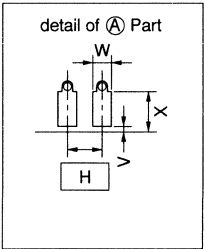
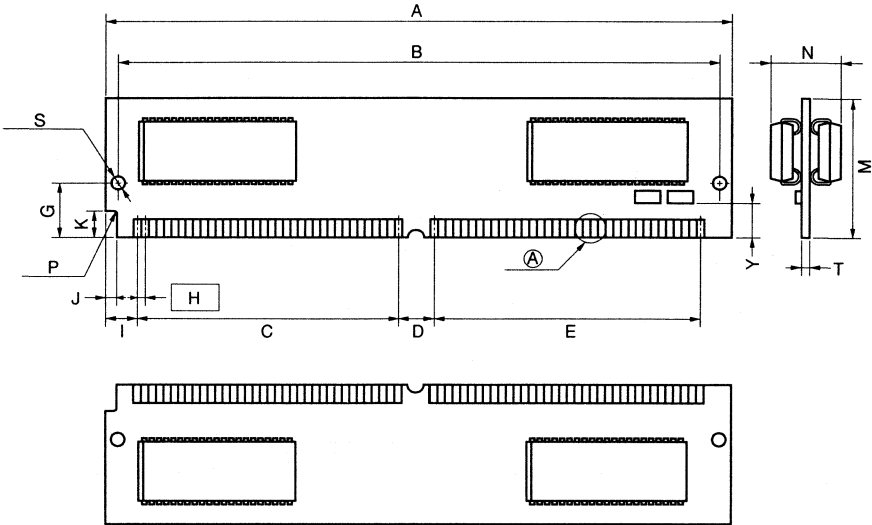
Hidden Refresh Cycle (Write)

★



Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	φ3.18	φ0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A45

MOS INTEGRATED CIRCUIT

MC-421000AA40 SERIES

1 M-WORD BY 40-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-421000AA40 is a 1 048 576 words by 40 bits dynamic RAM module on which 10 pieces of 4 M bits CMOS Dynamic RAM (μ PD424400) are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features



- 1 048 576 words by 40 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000AA40-60	60 ns	120 ns	6 300 mW	52.5 mW (CMOS level input)
MC-421000AA40-70	70 ns	140 ns	5 250 mW	
MC-421000AA40-80	80 ns	160 ns	4 725 mW	
MC-421000AA40-10	100 ns	190 ns	4 200 mW	

- Fast page mode
- 1 024 refresh cycles / 16 ms
- Three refresh methods can be applied : $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- 40-bit simultaneous switching
- Output buffers control : $\overline{\text{OE}}$ pin
- All inputs and outputs TTL compatible
- Single +5.0 V $\pm$ 5 % power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.

★ **Ordering Information**

Part number	Access time (MAX.)	Package	Mounted device
MC-421000AA40B-60	60 ns	72-pin Single In-line Memory Module (Socket type) Edge connector : Solder coating (HAL)	μ PD424400LA 300 mil SOJ×10 (Single side)
MC-421000AA40B-70	70 ns		
MC-421000AA40B-80	80 ns		
MC-421000AA40B-10	100 ns		
MC-421000AA40F-60	60 ns	72-pin Single In-line Memory Module (Socket type) Edge connector : Gold plating	
MC-421000AA40F-70	70 ns		
MC-421000AA40F-80	80 ns		
MC-421000AA40F-10	100 ns		

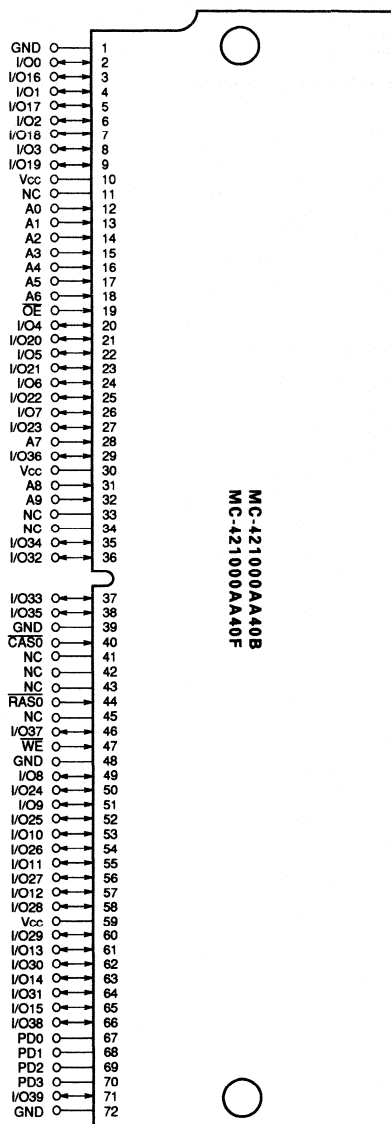
Quality Grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration (Front view)

72-pin Single In-line Memory Module Socket Type (Edge connector : Solder Coating, Gold Plating)

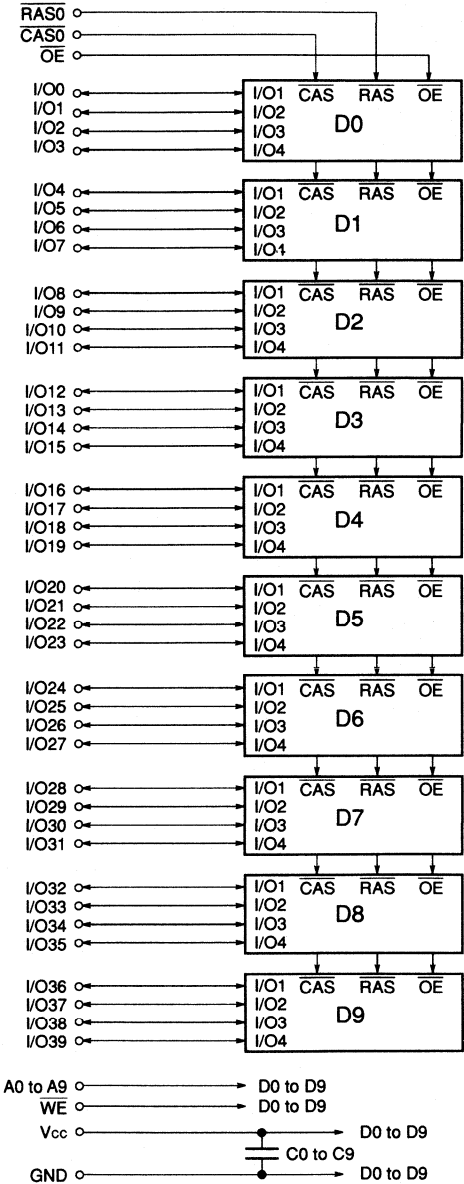


- A0 to A9 : Address Inputs
 I/O0 to I/O39 : Data Inputs/Outputs
CAS0 : Column Address Strobe
RAS0 : Row Address Strobe
WE : Write Enable
OE : Output Enable
 Vcc : Power Supply
 GND : Ground
 NC : No Connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

Block Diagram



Remark D0 to D9 : $\mu\text{PD424400LA}$

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		10	W
Operating temperature	T_{Op1}		0 to +70	°C
Storage temperature	T_{Stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_A		0		70	°C

Capacitance ($T_A = +25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A9			65	pF
	C_{I2}	$\overline{WE}$, $\overline{OE}$			70	
	C_{I3}	$\overline{RAS0}$			60	
	C_{I4}	$\overline{CAS0}$			60	
Data Input/Output capacitance	$C_{I/O}$	I/O0 to I/O39			12	pF

★ DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}(\text{MIN.})}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 200	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	1 000		
			$t_{\text{RAC}} = 80 \text{ ns}$	900		
			$t_{\text{RAC}} = 100 \text{ ns}$	800		
Standby current	I _{CC2}	$V_{\text{IH}(\text{MIN.})} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$		20	mA	
		$V_{\text{CC}} - 0.2 \text{ V} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$		10		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $V_{\text{IH}(\text{MIN.})} \leq \overline{\text{CAS}}$ $t_{\text{RC}} = t_{\text{RC}(\text{MIN.})}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 200	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	1 000		
			$t_{\text{RAC}} = 80 \text{ ns}$	900		
			$t_{\text{RAC}} = 100 \text{ ns}$	800		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{CAS}}$ Cycling $\overline{\text{RAS}} \leq V_{\text{IL}(\text{MAX.})}$ $t_{\text{PC}} = t_{\text{PC}(\text{MIN.})}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	900	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	800		
			$t_{\text{RAC}} = 80 \text{ ns}$	700		
			$t_{\text{RAC}} = 100 \text{ ns}$	600		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}(\text{MIN.})}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 200	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	1 000		
			$t_{\text{RAC}} = 80 \text{ ns}$	900		
			$t_{\text{RAC}} = 100 \text{ ns}$	800		
Input leakage current	I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	I/O0 to I/O39 are disabled (Hi-Z) $V_o = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted) Notes 5, 6

(1/2)



Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	120		140		160		190		ns	7
Read Write Cycle Time	t _{RWC}	165		185		210		250		ns	7
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40		45		50		60		ns	7
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	85		90		100		120		ns	7
Access Time from RAS	t _{RAC}		60		70		80		100	ns	8, 9
Access Time from $\overline{\text{CAS}}$ (Falling Edge)	t _{CAC}		15		20		20		25	ns	8, 9
Access Time from Column Address	t _{AA}		30		35		40		50	ns	8, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45		55	ns	9
Access Time from $\overline{\text{OE}}$	t _{OEa}		20		20		20		25	ns	9
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	17	50	ns	8
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		0		ns	9
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay Time ($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	15	0	20	0	25	ns	10
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	15		15		20		25		ns	
Output Buffer Turn-off Delay Time ($\overline{\text{OE}}$)	t _{OEZ}	0	15	0	15	0	20	0	25	ns	10
$\overline{\text{OE}}$ Command Hold Time	t _{OEh}	0		0		0		0		ns	
$\overline{\text{OE}}$ to RAS Inactive Setup Time	t _{OES}	0		0		0		0		ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{RP}	50		60		70		80		ns	
RAS Pulse Width (Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
RAS Hold Time	t _{RSH}	20		20		20		25		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		100		ns	
RAS to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	25	90	ns	8
$\overline{\text{CAS}}$ to RAS Precharge Time	t _{CRP}	10		10		10		10		ns	11
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		10		ns	
RAS Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		10		10		ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to RAS	t _{RAL}	30		35		40		50		ns	
Read Command Setup Time	t _{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		0		ns	12

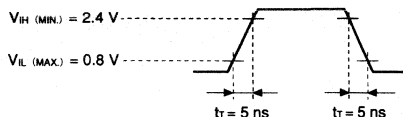
(2/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		15		20		ns	13
Write Command Pulse Width	t _{WP}	15		15		15		20		ns	13
Data-in Setup Time	t _{DS}	0		0		0		0		ns	14
Data-in Hold Time	t _{DH}	15		15		15		20		ns	14
$\overline{\text{WE}}$ Command Setup Time	t _{WCS}	0		0		0		0		ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	40		40		45		55		ns	15
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	80		90		105		130		ns	15
$\overline{\text{CAS}}$ Precharge Delay Time Referenced to $\overline{\text{WE}}$ (Fast Page Mode)	t _{CPWD}	55		60		70		85		ns	15
Column Address Delay Time Referenced to $\overline{\text{WE}}$	t _{AWD}	50		55		65		80		ns	15
Write Command Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20		20		20		25		ns	
Write Command Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15		15		15		20		ns	
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	t _{CSR}	10		10		10		10		ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	t _{CHR}	15		15		15		20		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		20		ns	
Refresh Time	t _{REF}		16		16		16		16	ms	

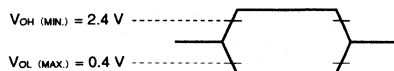
Notes

1. All voltages are referenced to GND.
2. An initial pause of 100 μ s is required after power up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles are required.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on trc and trc . Specified values are obtained with outputs open.
4. Address can be changed once or less while $\overline{\text{RAS}} = \text{VIL}$ and $\overline{\text{CAS}} = \text{VH}$.
5. AC measurements assume $\text{tr} = 5$ ns.
6. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



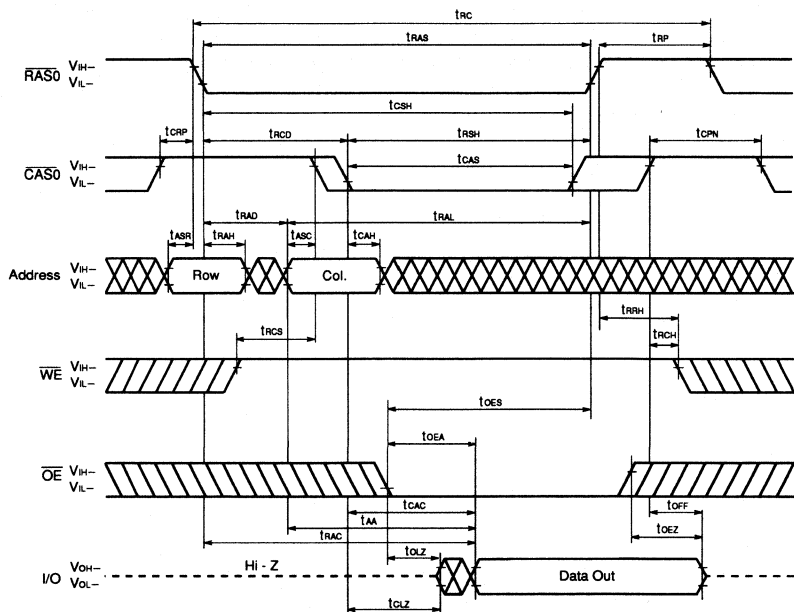
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_a = 0$ to 70°C) is assured.
8. In random read cycle, the access time is changed by the conditions of trAD and trCD as follows.

CONDITION	ACCESS TIME
$\text{trAD} \leq \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\text{trAD} (\text{MAX.}) < \text{trAD}$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$
$\text{trCD} (\text{MAX.}) < \text{trCD}$	$\text{tCAC} (\text{MAX.})$

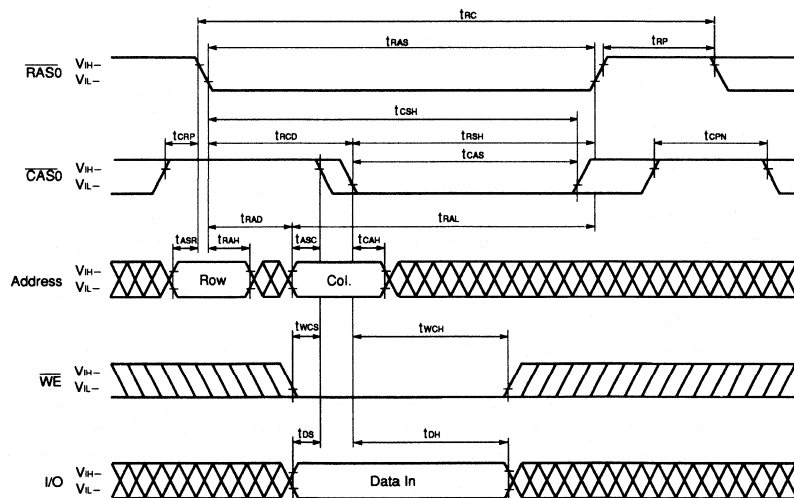
$\text{trAD} (\text{MAX.})$ and $\text{trCD} (\text{MAX.})$ indicate the points which the access time changes and are not the limits of operation.

9. Loading conditions are 2 TTL and 100 pF.
10. $\text{toFF} (\text{MAX.})$ and $\text{toEZ} (\text{MAX.})$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL} .
11. $\text{tCRP} (\text{MIN.})$ requirement should be applicable for $\overline{\text{RAS}} / \overline{\text{CAS}}$ cycles preceded by any cycles.
12. Either $\text{trCH} (\text{MIN.})$ or $\text{trRH} (\text{MIN.})$ must be satisfied for a read cycle.
13. $\text{tWP} (\text{MIN.})$ is applicable for late write cycle or read modify write cycle. In early write cycles, $\text{twCH} (\text{MIN.})$ should be satisfied.
14. This specification is referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{WE}}$ falling edge in late write or read modify write cycles.
15. If $\text{twCS} \geq \text{twCS} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{trWD} \geq \text{trWD} (\text{MIN.})$, $\text{tcWD} \geq \text{tcWD} (\text{MIN.})$, $\text{tAWD} \geq \text{tAWD} (\text{MIN.})$, $\text{tcpWD} \geq \text{tcpWD} (\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above condition is met, the condition of the data out is indeterminate.

Read Cycle

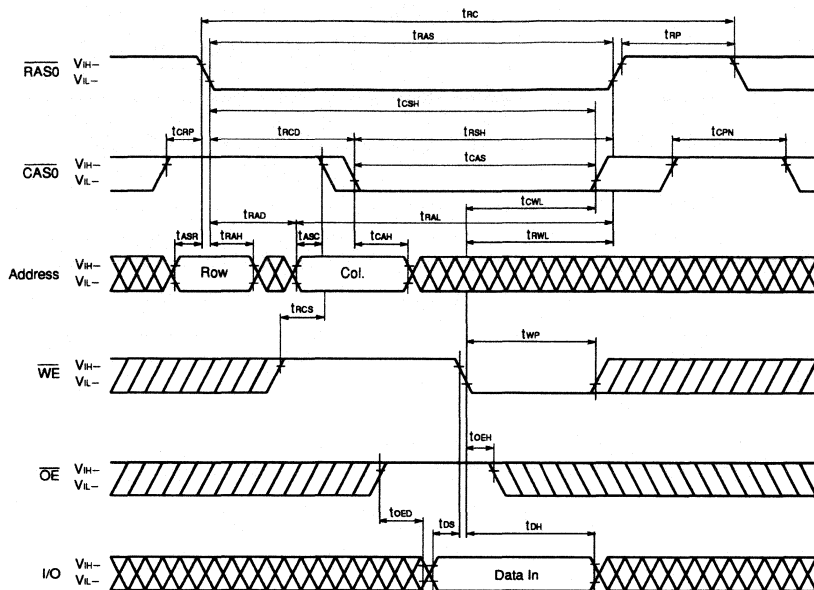


Early Write Cycle

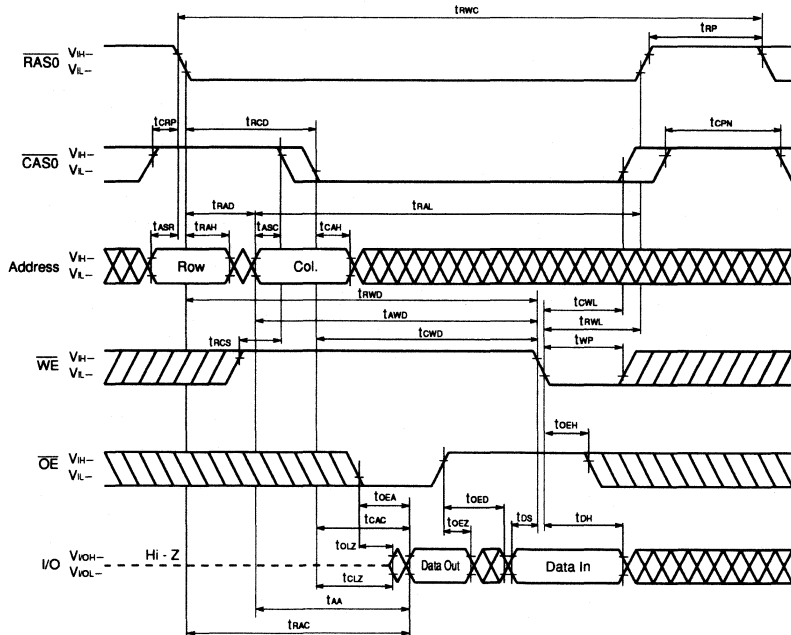


Remark $\overline{OE}$ = Don't Care

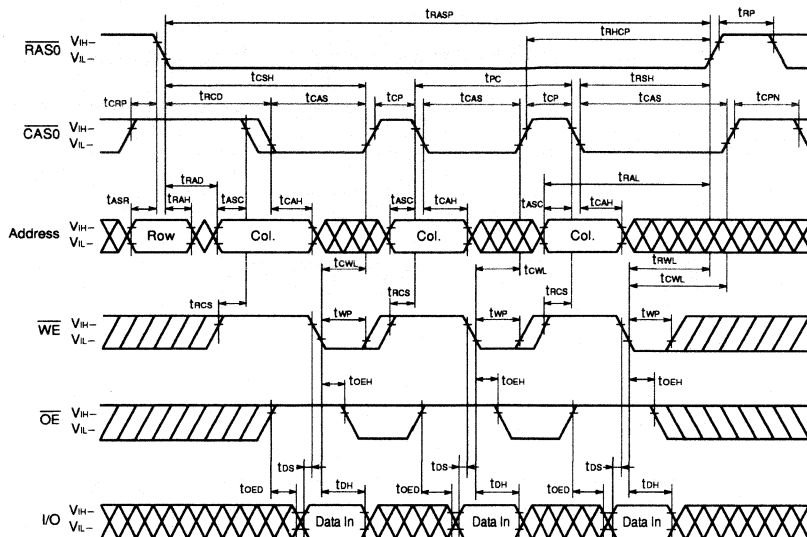
Late Write Cycle



Read Modify Write Cycle

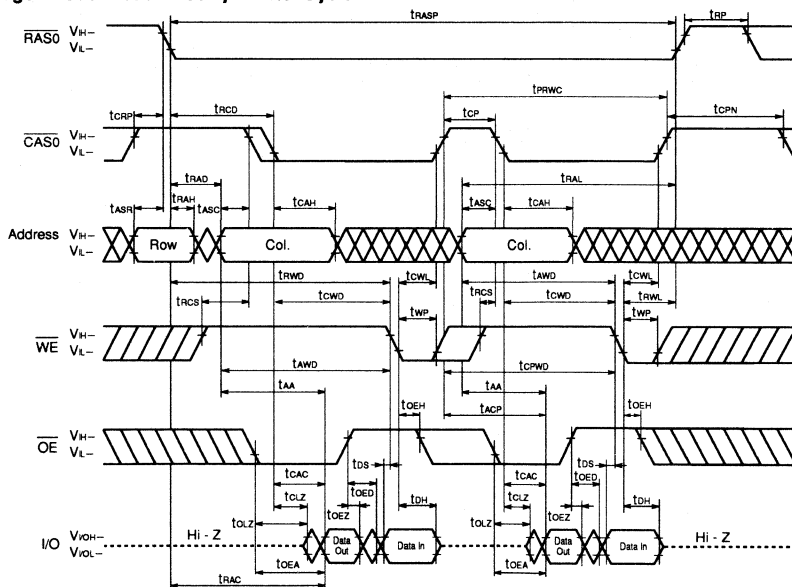


Fast Page Mode Late Write Cycle



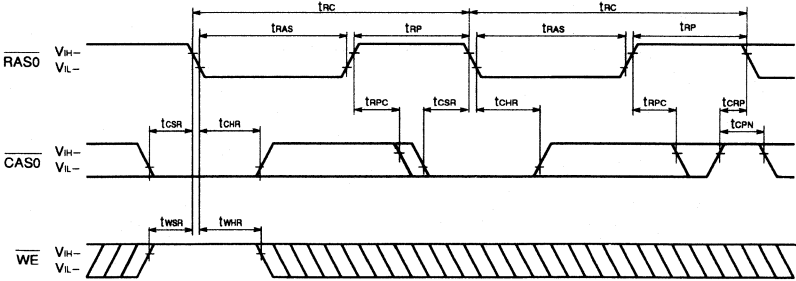
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Read Modify Write Cycle



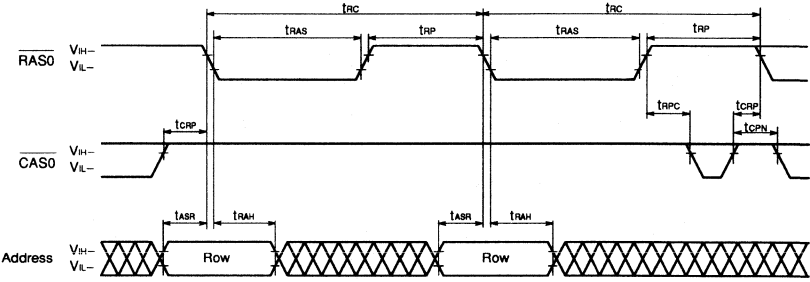
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



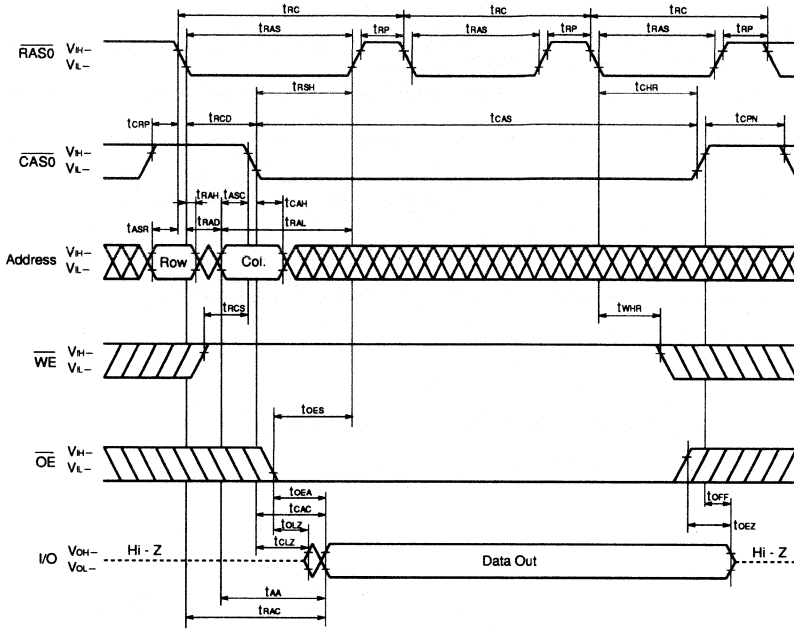
Remark Address, $\overline{\text{OE}}$ = Don't care I/O = Hi - Z

RAS Only Refresh Cycle



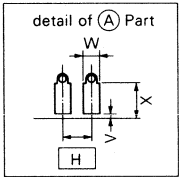
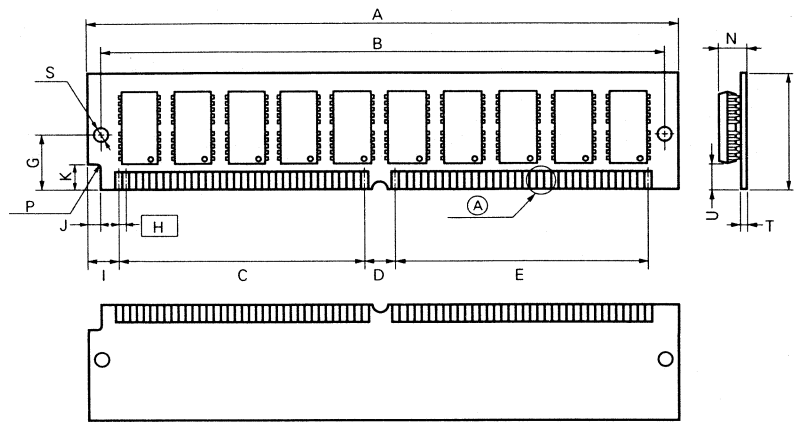
Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$ = Don't care I/O = Hi - Z

Hidden Refresh Cycle



Package Drawing

MC-421000AA40B, 421000AA40F
72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



M72B-50A26-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	φ3.18	φ0.125
T	1.27 ^{+0.10} _{-0.08}	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

MOS INTEGRATED CIRCUIT

MC-421000A32, 421000A36 SERIES

1 M-WORD BY 32-BIT, 1 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000A32 series is a 1 048 576 words by 32 bits dynamic RAM module on which 8 pieces of 4 M DRAM : μ PD424400 are assembled.

The MC-421000A36 series is a 1 048 576 words by 36 bits dynamic RAM module on which 8 pieces of 4 M DRAM : μ PD424400 and 4 pieces of 1 M DRAM : μ PD421000 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1 048 576 words by 32 bits organization (MC-421000A32 series)
- 1 048 576 words by 36 bits organization (MC-421000A36 series)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000A32-60	60 ns	120 ns	5 040 mW	42 mW (CMOS level input)
MC-421000A32-70	70 ns	140 ns	4 200 mW	
MC-421000A32-80	80 ns	160 ns	3 780 mW	
MC-421000A32-10	100 ns	190 ns	3 360 mW	
MC-421000A36-60	60 ns	120 ns	6 510 mW	63 mW (CMOS level input)
MC-421000A36-70	70 ns	140 ns	5 880 mW	
MC-421000A36-80	80 ns	160 ns	5 250 mW	
MC-421000A36-10	100 ns	190 ns	4 620 mW	

- 1 024 refresh cycles/16 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V $\pm$ 5 % power supply
- Access time can be distinguished with characteristics of PD-pins(PD0 to PD3)

The information in this document is subject to change without notice.

The mark ★ shows revised points.

★ Ordering Information

[MC-421000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	8 pieces of μ PD424400LA (300 mil SOJ) (Single side)
MC-421000A32B-70	70 ns		
MC-421000A32B-80	80 ns		
MC-421000A32B-10	100 ns		
MC-421000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-421000A32F-70	70 ns		
MC-421000A32F-80	80 ns		
MC-421000A32F-10	100 ns		

[MC-421000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A36B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	8 pieces of μ PD424400LA (300 mil SOJ) 4 pieces of μ PD421000GX (6 mm $\times$ 16 mm TSOP (II)) (Single side)
MC-421000A36B-70	70 ns		
MC-421000A36B-80	80 ns		
MC-421000A36B-10	100 ns		
MC-421000A36F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-421000A36F-70	70 ns		
MC-421000A36F-80	80 ns		
MC-421000A36F-10	100 ns		
MC-421000A36BE-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	8 pieces of μ PD424400LA (300 mil SOJ) 4 pieces of μ PD421000LA (300 mil SOJ) (Double side)
MC-421000A36BE-70	70 ns		
MC-421000A36BE-80	80 ns		
MC-421000A36BE-10	100 ns		
MC-421000A36FE-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-421000A36FE-70	70 ns		
MC-421000A36FE-80	80 ns		
MC-421000A36FE-10	100 ns		
MC-421000A36BJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	8 pieces of μ PD424400LA (300 mil SOJ) 4 pieces of μ PD421000LA (300 mil SOJ) (Single side)
MC-421000A36BJ-70	70 ns		
MC-421000A36BJ-80	80 ns		
MC-421000A36BJ-10	100 ns		
MC-421000A36FJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-421000A36FJ-70	70 ns		
MC-421000A36FJ-80	80 ns		
MC-421000A36FJ-10	100 ns		

Quality Grade

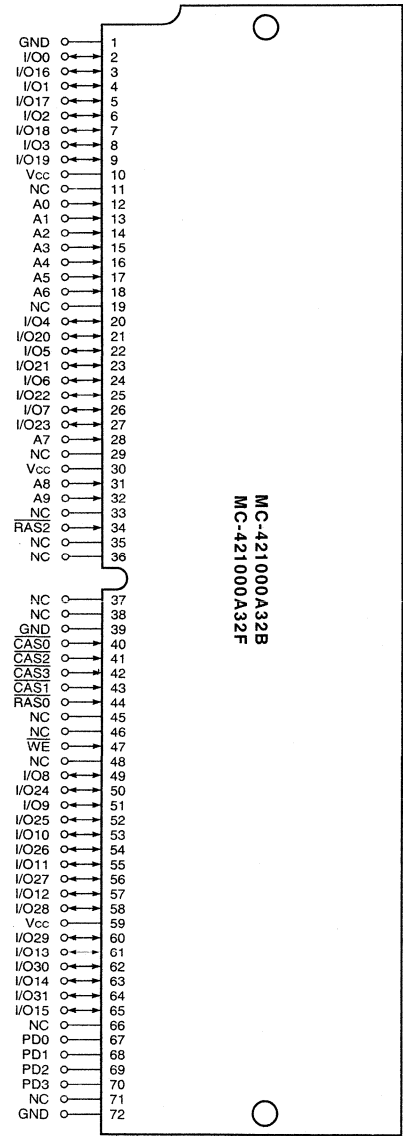
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number 1E1-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ Pin Configurations

[MC-421000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder Coating, Gold Plating)



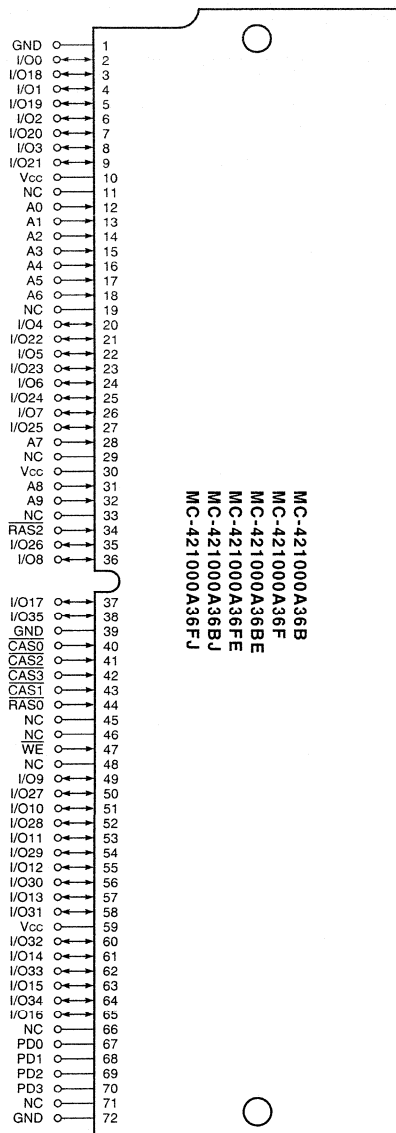
- A0-A9 : Address Inputs
- I/O0-I/O31 : Data Inputs/Outputs
- CAS0-CAS3 : Column Address Strobe
- RAS0, RAS2 : Row Address Strobe
- WE : Write Enable
- Vcc : Power Supply
- GND : Ground
- NC : No connection

The internal connection of PD pins (PD0 - PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

[MC-421000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder Coating, Gold Plating)



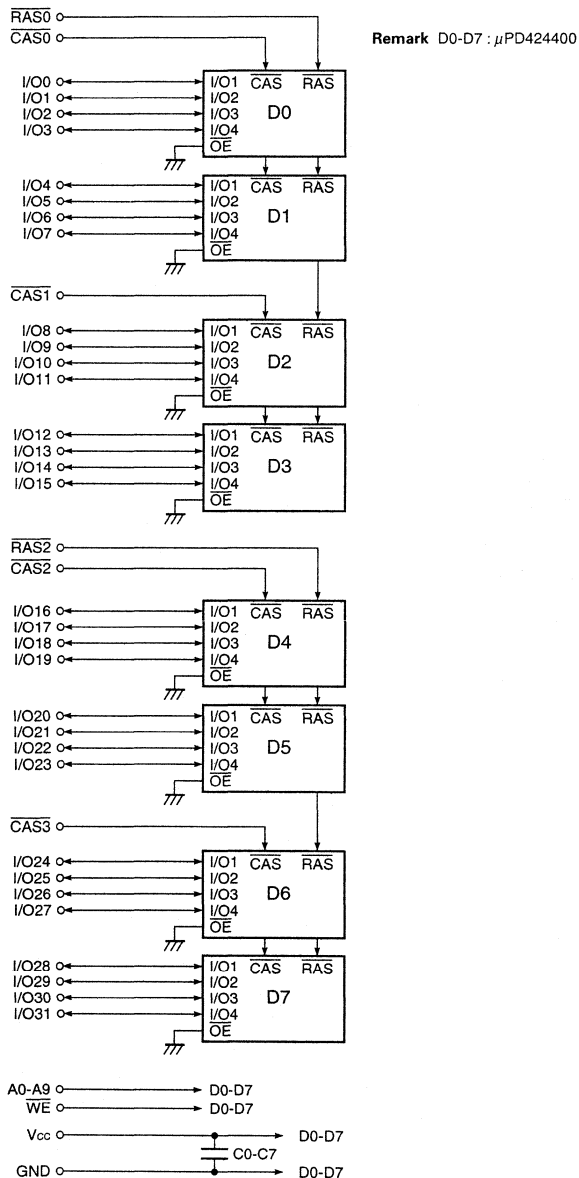
- A0-A9 : Address Inputs
 I/O0-I/O35 : Data Inputs/Outputs
 CAS0-CAS3 : Column Address Strobe
 RAS0, RAS2 : Row Address Strobe
 WE : Write Enable
 Vcc : Power Supply
 GND : Ground
 NC : No connection

The internal connection of PD pins (PD0 - PD3) depends on access time.

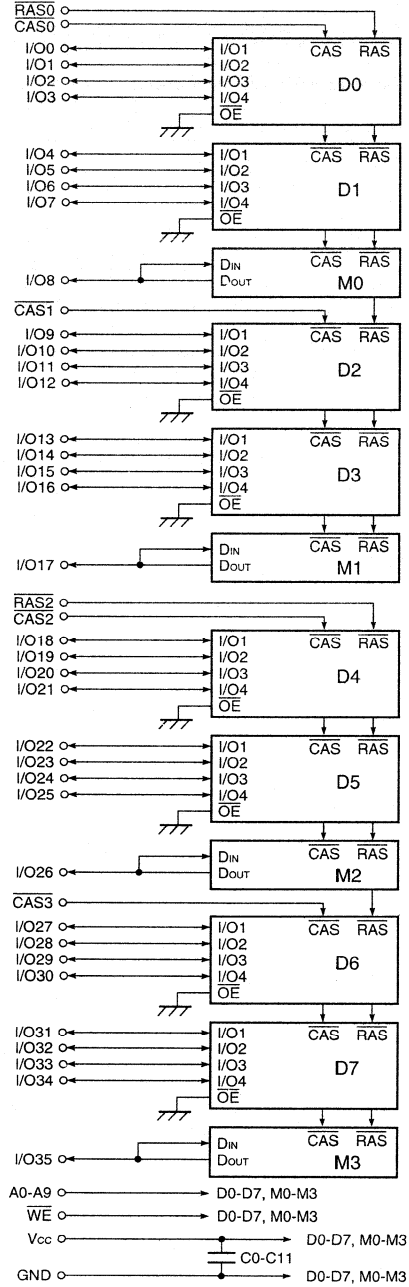
Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

Block Diagram

[MC-421000A32 series]



[MC-421000A36 series]



Remark D0-D7 : μ PD424400
M0-M3 : μ PD421000

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-421000A32	8	W
		MC-421000A36	12	
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance ($T_a = +25^\circ\text{C}$, $f = 1\text{ MHz}$)

[MC-421000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{i1}	A0 - A9			68	pF
	C_{i2}	$\overline{WE}$			76	
	C_{i3}	$\overline{RAS0}$, $\overline{RAS2}$			43	
	C_{i4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output capacitance	$C_{i/O}$	I/O0 - I/O31			17	pF

[MC-421000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{i1}	A0 - A9			88	pF
	C_{i2}	$\overline{WE}$			104	
	C_{i3}	$\overline{RAS0}$, $\overline{RAS2}$			57	
	C_{i4}	$\overline{CAS0}$ - $\overline{CAS3}$			36	
Data Input/Output capacitance	$C_{i/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			17	pF
	$C_{i/O2}$	I/O8 - I/O17, I/O26, I/O35			22	

DC Characteristics (Recommended Operating Conditions unless otherwise noted)
[MC-421000A32 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trAC} = 60 \text{ ns}$	960	mA	3,4,7
			$\text{trAC} = 70 \text{ ns}$	800		
			$\text{trAC} = 80 \text{ ns}$	720		
			$\text{trAC} = 100 \text{ ns}$	640		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq \text{V}_{\text{IH}}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$		16	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq \text{V}_{\text{CC}} - 0.2 \text{ V}$ $\text{I}_\text{O} = 0 \text{ mA}$		8		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq \text{V}_{\text{IH}}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trAC} = 60 \text{ ns}$	960	mA	3,4, 5,7
			$\text{trAC} = 70 \text{ ns}$	800		
			$\text{trAC} = 80 \text{ ns}$	720		
			$\text{trAC} = 100 \text{ ns}$	640		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq \text{V}_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trAC} = 60 \text{ ns}$	720	mA	3,4,6
			$\text{trAC} = 70 \text{ ns}$	640		
			$\text{trAC} = 80 \text{ ns}$	560		
			$\text{trAC} = 100 \text{ ns}$	480		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trAC} = 60 \text{ ns}$	960	mA	3,4
			$\text{trAC} = 70 \text{ ns}$	800		
			$\text{trAC} = 80 \text{ ns}$	720		
			$\text{trAC} = 100 \text{ ns}$	640		
Input leakage current	I _{I(L)}	$\text{V}_\text{I} = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	$\text{V}_\text{O} = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage	V _{OH}	$\text{I}_\text{O} = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$\text{I}_\text{O} = +4.2 \text{ mA}$		0.4	V	

[MC-421000A36 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	trac = 60 ns	1 240	mA	3,4,7
			trac = 70 ns	1 120		
			trac = 80 ns	1 000		
			trac = 100 ns	880		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq \text{V}_{\text{IH}}(\text{MIN.})$	I _O = 0 mA	24	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq \text{V}_{\text{CC}} - 0.2 \text{ V}$	I _O = 0 mA	12		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq \text{V}_{\text{IH}}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	trac = 60 ns	1 240	mA	3,4,5,7
			trac = 70 ns	1 120		
			trac = 80 ns	1 000		
			trac = 100 ns	880		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq \text{V}_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	trac = 60 ns	1 040	mA	3,4,6
			trac = 70 ns	920		
			trac = 80 ns	800		
			trac = 100 ns	680		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	trac = 60 ns	1 240	mA	3,4
			trac = 70 ns	1 120		
			trac = 80 ns	1 000		
			trac = 100 ns	880		
Input leakage current	I _{I(L)}	V _I = 0 to 5.5 V all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	V _O = 0 to 5.5 V Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage	V _{OH}	I _O = -5.0 mA	2.4		V	
Low level output voltage	V _{OL}	I _O = +4.2 mA		0.4	V	

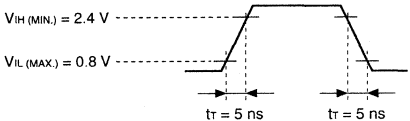
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t _{TRAC} = 60 ns		t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		t _{TRAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	120		140		160		190		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		60		ns	
Access Time from RAS	t _{TRAC}		60		70		80		100	ns	10,11
Access Time from $\overline{\text{CAS}}$	MC-421000A32 MC-421000A36	t _{TCAC}	15	20	20	20	25	25	25	ns	10,11
			20								
Access Time from Column Address	t _{TAA}		30		35		40		50	ns	10,11
Access Time from CAS Precharge	t _{TACP}		35		40		45		55	ns	11
RAS to Column Address Delay Time	t _{TRAD}	15	30	15	35	17	40	17	50	ns	10
CAS to Data Setup Time	t _{TCLZ}	0		0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	t _{TOFF}	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)	t _{TR}	3	50	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{TRP}	50		60		70		80		ns	
RAS Pulse Width	t _{TRAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
RAS Pulse Width (Fast Page Mode)	t _{TRASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
RAS Hold Time	t _{TRSH}	20		20		20		25		ns	
CAS Pulse Width	t _{TCAS}	20	10 000	20	10 000	20	10 000	25	10 000	ns	
CAS Hold Time	t _{TCSH}	60		70		80		100		ns	
RAS to CAS Delay Time	t _{TRCD}	20	40	20	50	25	60	25	75	ns	10
CAS to RAS Precharge Time	t _{TCRP}	10		10		10		10		ns	13
CAS Precharge Time	t _{TCPN}	10		10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	t _{TCP}	10		10		10		10		ns	
RAS Precharge CAS Hold Time	t _{TRPC}	10		10		10		10		ns	
RAS Hold Time from CAS Precharge	t _{TRHCP}	35		40		45		55		ns	
Row Address Setup Time	t _{TASR}	0		0		0		0		ns	
Row Address Hold Time	t _{TRAH}	10		10		12		12		ns	
Column Address Setup Time	t _{TASC}	0		0		0		0		ns	
Column Address Hold Time	MC-421000A32 MC-421000A36	t _{TCAH}	15	15	15		20		20	ns	
				17	20						
Column Address Lead Time Referenced to RAS	t _{TRAL}	30		35		40		50		ns	
Read Command Setup Time	t _{TRCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{TRRH}	10		10		10		10		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{TRCH}	0		0		0		0		ns	14
WE Hold Time Referenced to CAS	t _{TWCH}	15		15		15		20		ns	15
Data-in Setup Time	t _{TDS}	0		0		0		0		ns	16
Data-in Hold Time	MC-421000A32 MC-421000A36	t _{TDH}	15	15	15		20		20	ns	16
					20						
Write Command Setup Time	t _{TWCS}	0		0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	t _{TCSR}	10		10		10		10		ns	
CAS Hold Time (CAS before RAS Refresh)	t _{TCHR}	15		15		15		20		ns	
WE Setup Time	t _{TWSR}	10		10		10		10		ns	
WE Hold Time	t _{TWHR}	15		15		15		20		ns	
Refresh Time	t _{TREF}		16		16		16		16	ms	

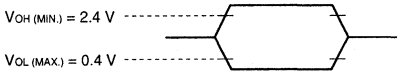
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on cycles rates (trc and tpc).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq \text{V}_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq \text{V}_{\text{IH}}$ (MIN.).
8. AC measurements assume $\text{tr} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification

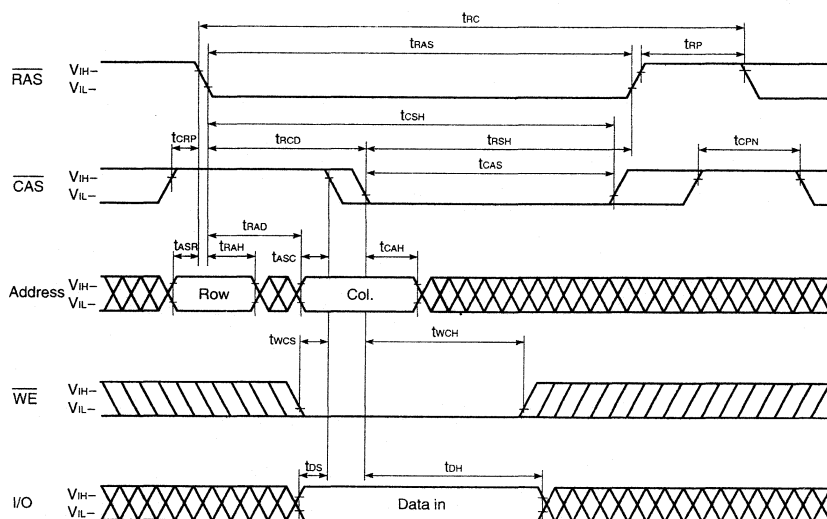
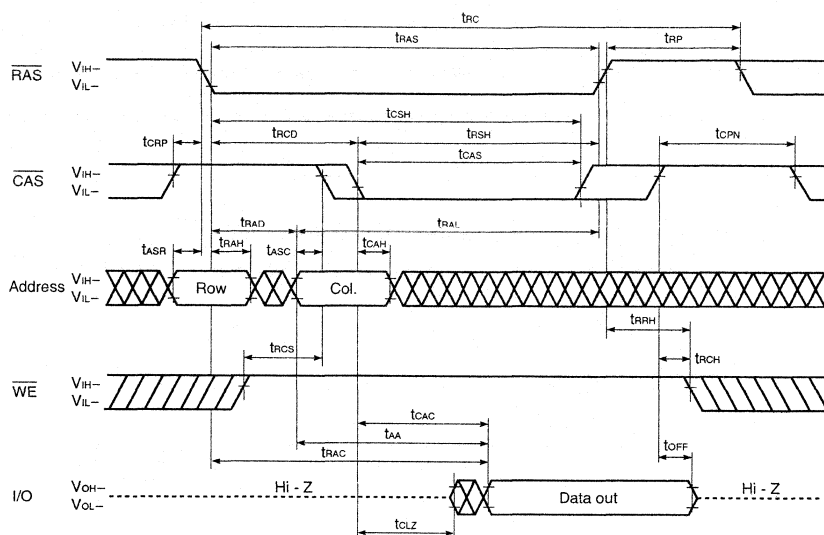


10. For read cycles, access time is defined as follows :

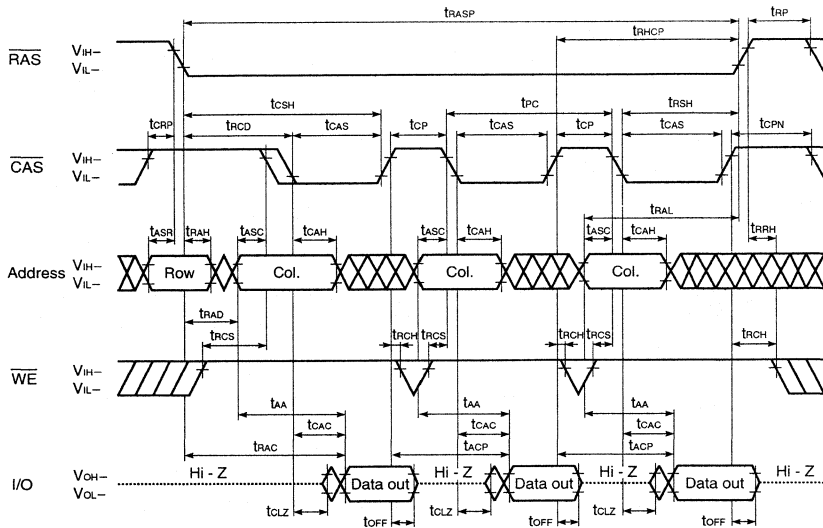
Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\text{trAD} > \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$	$\text{trAD} + \text{tAA} (\text{MAX.})$
$\text{trCD} > \text{trCD} (\text{MAX.})$	$\text{tCAC} (\text{MAX.})$	$\text{trCD} + \text{tCAC} (\text{MAX.})$

$\text{trAD} (\text{MAX.})$ and $\text{trCD} (\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD} (\text{MAX.})$ and $\text{trCD} \geq \text{trCD} (\text{MAX.})$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. $\text{tOFF} (\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $\text{tCRP} (\text{MIN.})$ requirement should be applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles preceded by any cycles.
14. Either $\text{trCH} (\text{MIN.})$ or $\text{trRH} (\text{MIN.})$ should be met in read cycles.
15. In early write cycles, $\text{twCH} (\text{MIN.})$ should be met.
16. $\text{tDS} (\text{MIN.})$ and $\text{tDH} (\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $\text{twCS} \geq \text{twCS} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

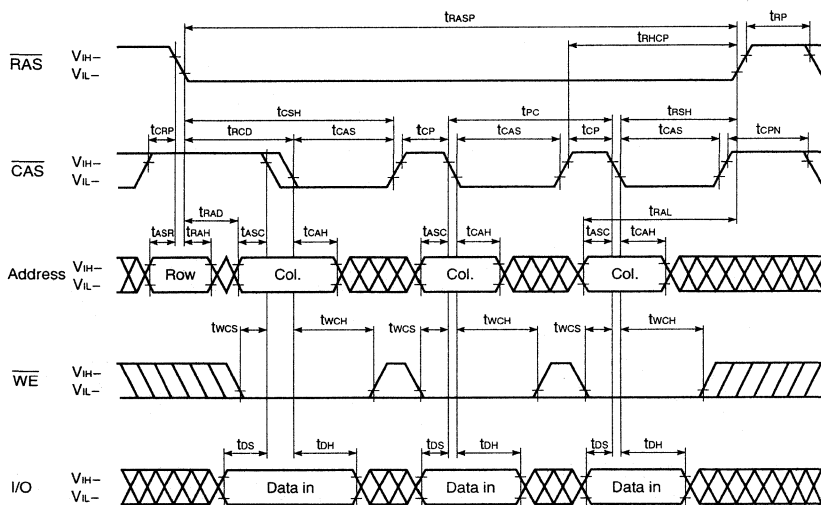


Fast Page Mode Read Cycle



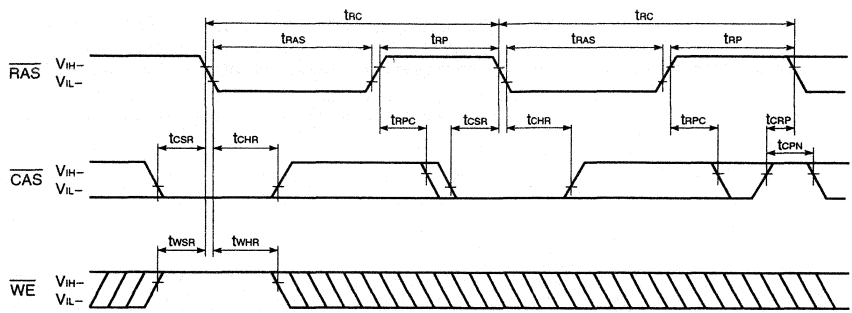
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



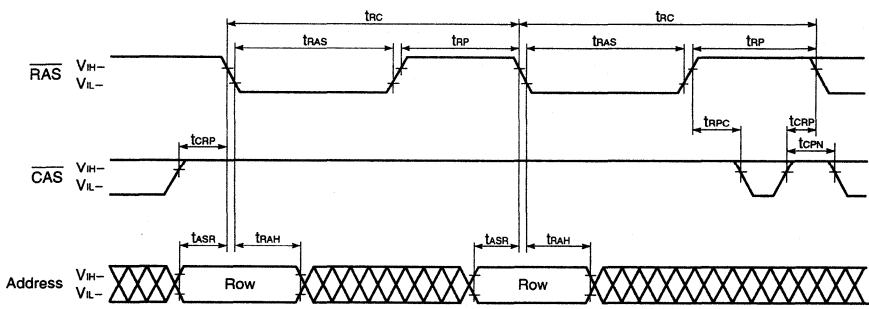
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



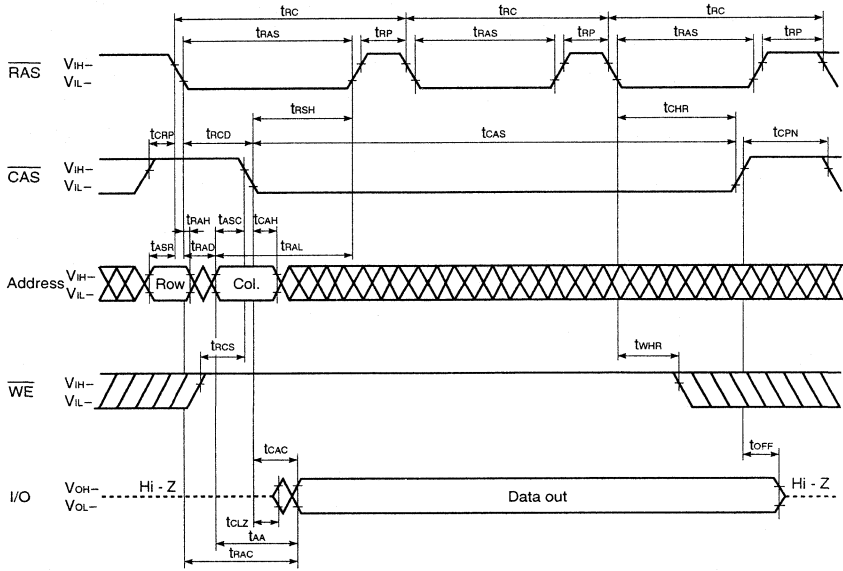
Remark Address = Don't care I/O = Hi - Z

RAS Only Refresh Cycle



Remark $\overline{\text{WE}}$ = Don't care I/O = Hi - Z

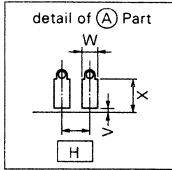
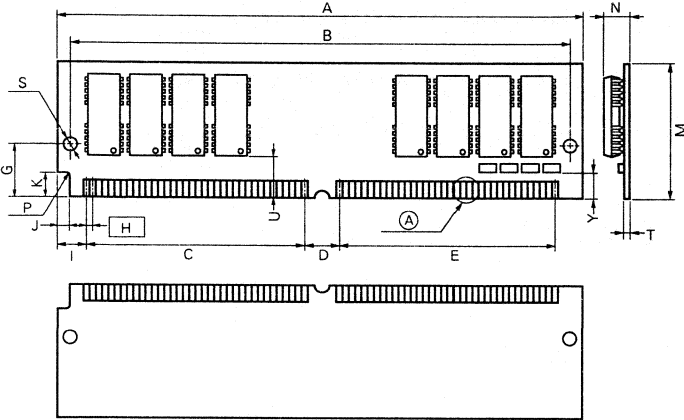
Hidden Refresh Cycle



Package Drawings

MC-421000A32B, 421000A32F

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)

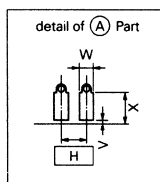
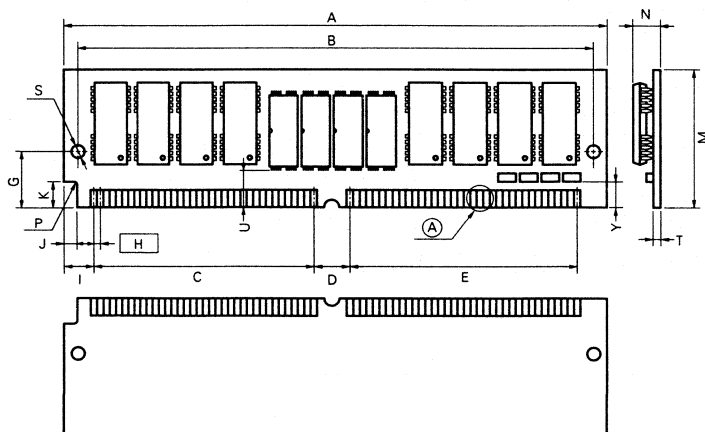


M72B-50A21-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	Φ3.18	Φ0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	6.5 MIN.	0.255 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

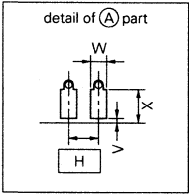
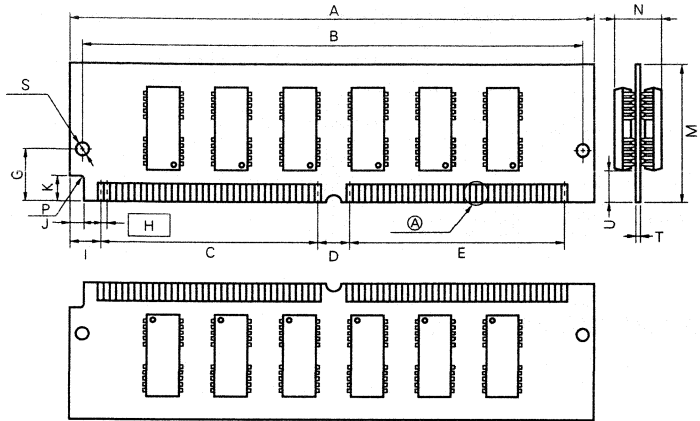
MC-421000A36B, 421000A36F

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



M72B-50A19-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	Ø3.18	Ø0.125
T	1.27 ^{+0.08} _{-0.08}	0.050±0.004
U	5.32 MIN.	0.209 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

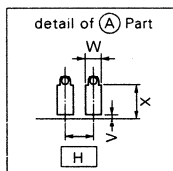
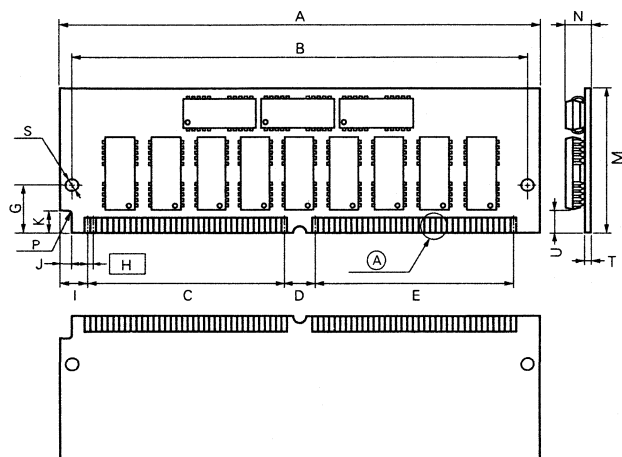
MC-421000A36BE, 421000A36FE**72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)**

M72B-50A33-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R 1.57	R 0.062
S	Ø3.18	Ø0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	6.0 MIN.	0.236 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

MC-421000A36BJ, 421000A36FJ

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



M72B-50A23-2

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	Ø3.18	Ø0.125
T	1.27 ^{+0.13} _{-0.08}	0.050±0.004
U	3.78 MIN.	0.148 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

MOS INTEGRATED CIRCUIT

MC-421000A32BA, 421000A32FA

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-421000A32BA, 421000A32FA are 1,048,576 words by 32 bits dynamic RAM module on which 2 pieces of 16 M DRAM: μ PD4218160 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 32 bits organization
- Fast access and cycle time

★

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000A32-60	60 ns	110 ns	1,760 mW	11 mW (CMOS level input)
MC-421000A32-70	70 ns	130 ns	1,650 mW	
MC-421000A32-80	80 ns	150 ns	1,540 mW	

- 1,024 refresh cycles/16 ms
- CAS before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ± 0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

★

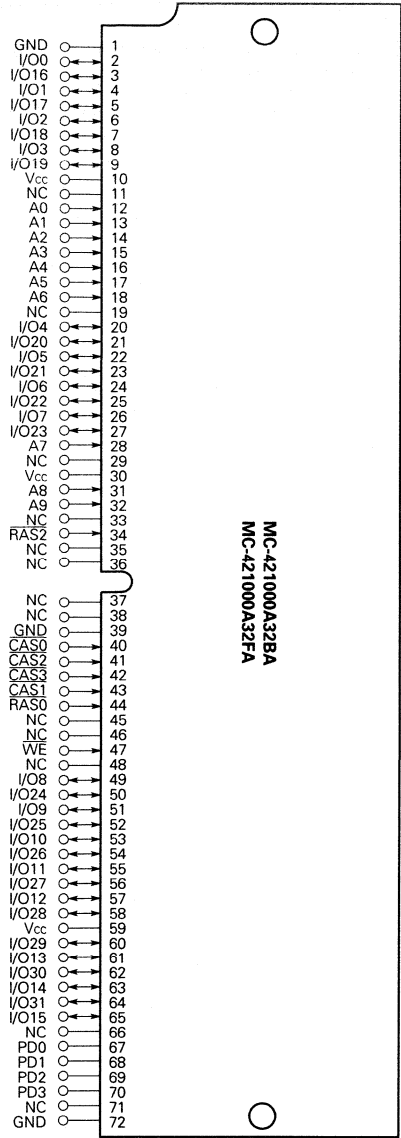
The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A32BA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	2 pieces of μ PD4218160LE (400 mil SOJ) [Single side]
MC-421000A32BA-70	70 ns		
MC-421000A32BA-80	80 ns		
MC-421000A32FA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A32FA-70	70 ns		
MC-421000A32FA-80	80 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



- A0 - A9 : Address Inputs
I/O0 - I/O31 : Data Inputs/Outputs
CAS0 - CAS3 : Column Address Strobe
RAS0, RAS2 : Row Address Strobe
WE : Write Enable
Vcc : Power Supply
GND : Ground
NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	GND	GND	GND
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

Block Diagram



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		17	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			30	pF
	C_{I2}	$\overline{WE}$			34	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			22	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			22	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling				
		t _{RC} = t _{RC} (MIN.)				
		I _O = 0 mA				
		t _{RAC} = 60 ns		320		
		t _{RAC} = 70 ns		300		
		t _{RAC} = 80 ns		280		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH}$ (MIN.)	I _O = 0 mA		4	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2$ V	I _O = 0 mA		2	
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling				
		$\overline{\text{CAS}} \geq V_{IH}$ (MIN.)				
		t _{RC} = t _{RC} (MIN.)				
		I _O = 0 mA				
		t _{RAC} = 60 ns		320		
		t _{RAC} = 70 ns		300		
		t _{RAC} = 80 ns		280		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{IL}$ (MAX.), $\overline{\text{CAS}}$ Cycling				
		t _{PC} = t _{PC} (MIN.)				
		I _O = 0 mA				
		t _{RAC} = 60 ns		180		
		t _{RAC} = 70 ns		160		
		t _{RAC} = 80 ns		140		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling				
		t _{RC} = t _{RC} (MIN.)				
		I _O = 0 mA				
		t _{RAC} = 60 ns		320		
		t _{RAC} = 70 ns		300		
		t _{RAC} = 80 ns		280		
Input leakage current	I _I (L)	V _I = 0 to 5.5 V All other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _O (L)	V _O = 0 to 5.5 V Output is disabled (Hi-Z)	-10	+10	μA	
★ High level output voltage	V _{OH}	I _O = -2.5 mA	2.4		V	
★ Low level output voltage	V _{OL}	I _O = +2.1 mA		0.4	V	

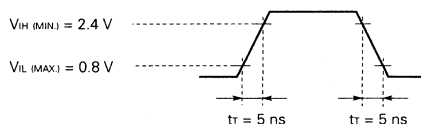
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15		18		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	45	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	5		5		5		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		16		16		16	ms	

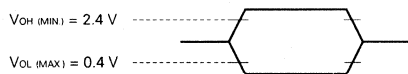
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on cycle rates (trc and tpc).
4. Specified values are obtained with outputs unloaded.
5. Icc3 is measured assuming that all column address inputs are held at either high or low.
6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.).
8. AC measurements assume $\text{tr} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

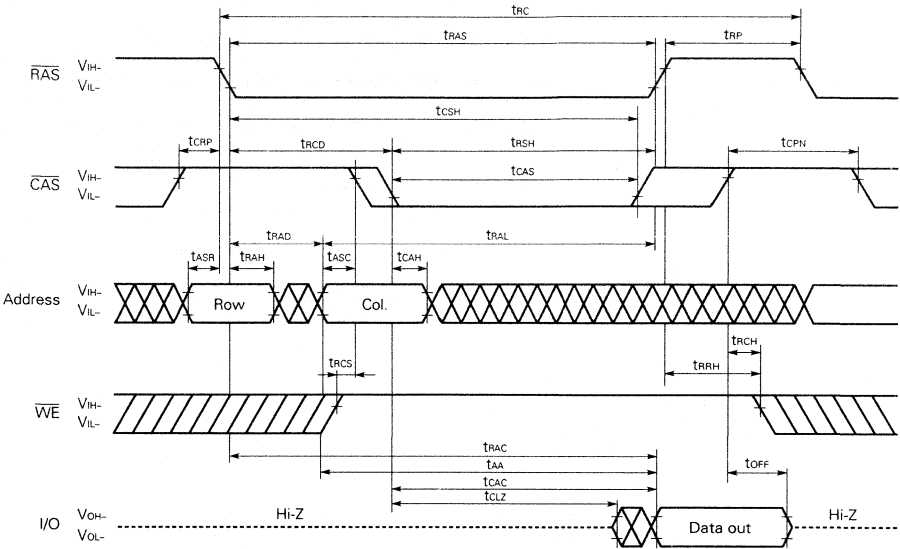
Input Conditions	Access Time	Access Time from RAS
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

trAD (MAX.) and trCD (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

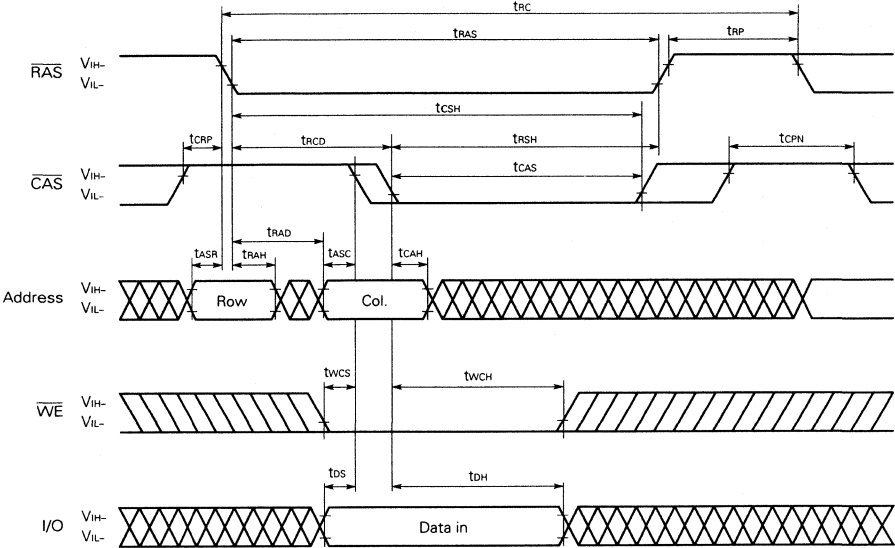
★

11. Loading conditions are 1 TTL and 100 pF.
12. tOFF (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. tCRP (MIN.) requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either trCH (MIN.) or trRH (MIN.) should be met in read cycles.
15. In early write cycles, twCH (MIN.) should be met.
16. tDS (MIN.) and tDH (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $\text{twCS} \geq \text{twCS (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

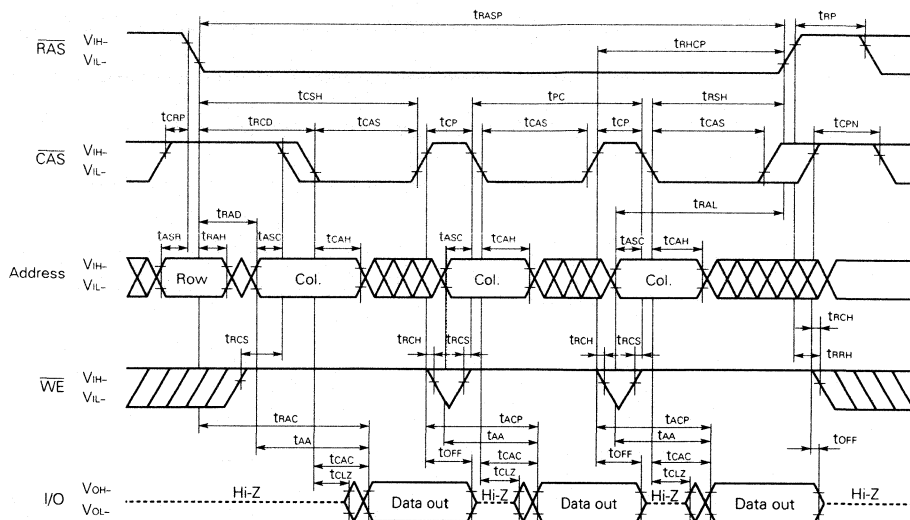
Read Cycle



Early Write Cycle

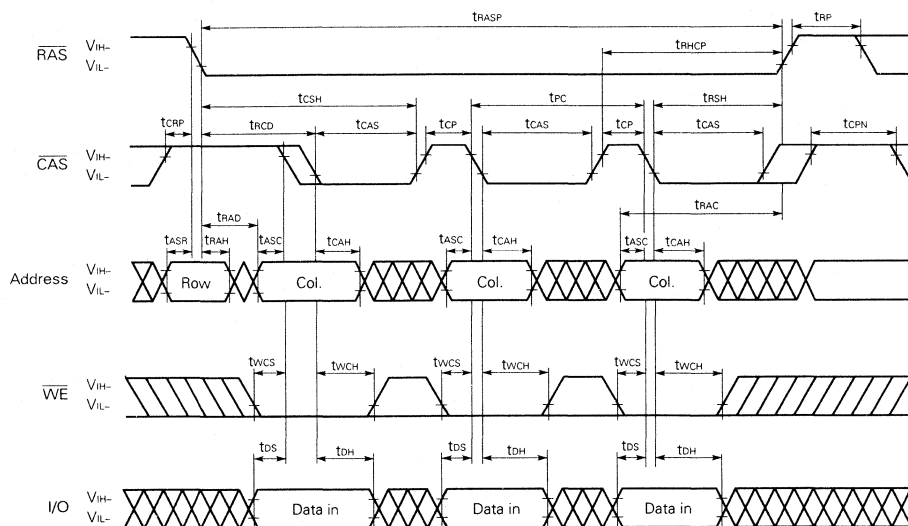


Fast Page Mode Read Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

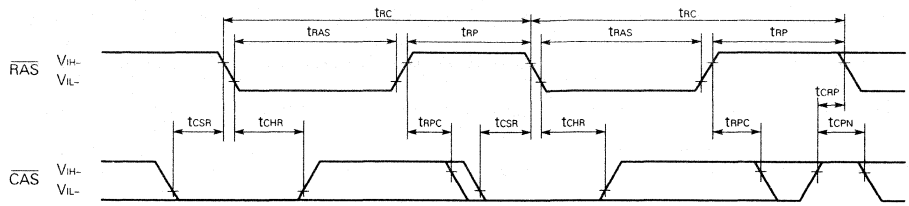
Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

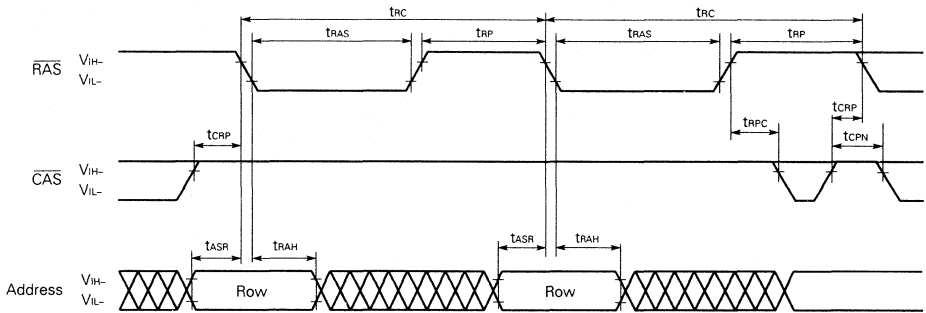


CAS Before RAS Refresh Cycle



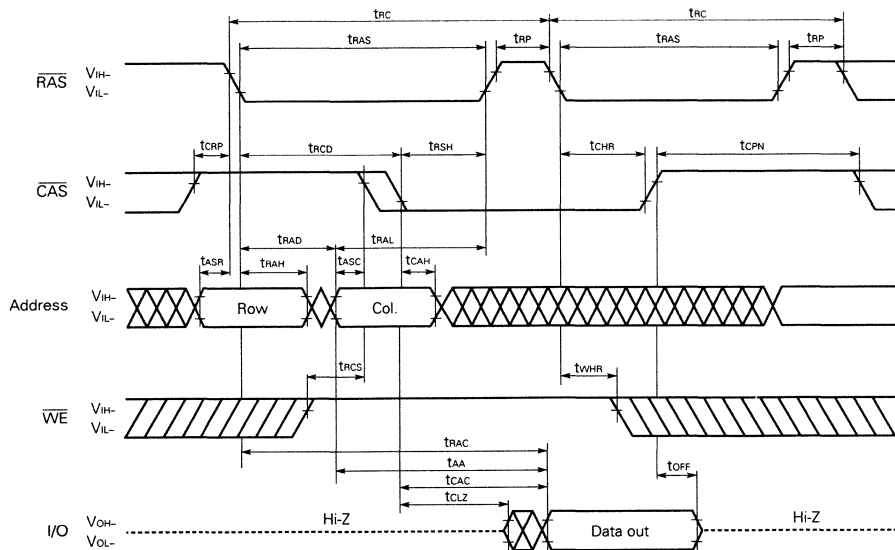
Remark Address, $\overline{WE}$: Don't care I/O: Hi-Z

RAS Only Refresh Cycle



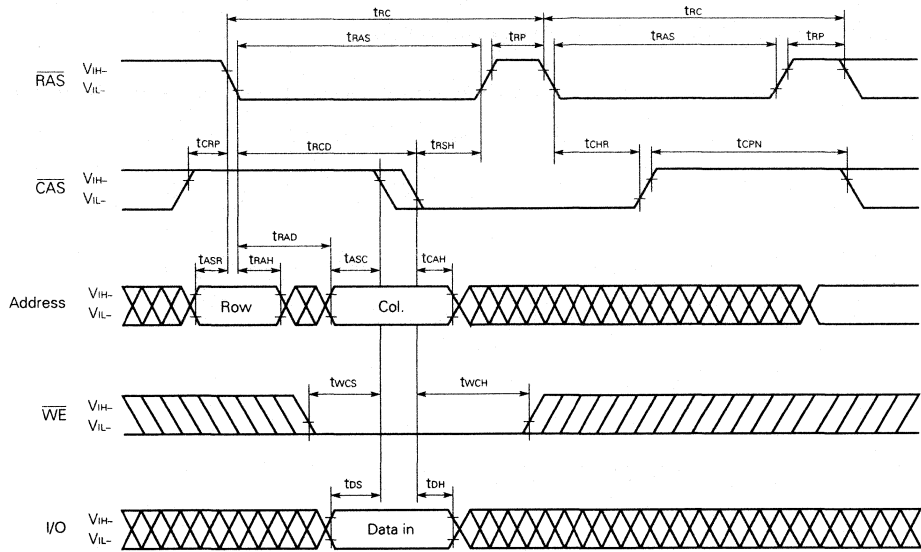
Remark $\overline{WE}$: Don't care I/O: Hi-Z

★ Hidden Refresh Cycle (Read)



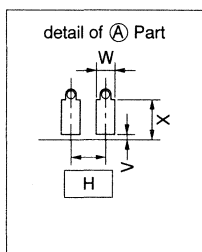
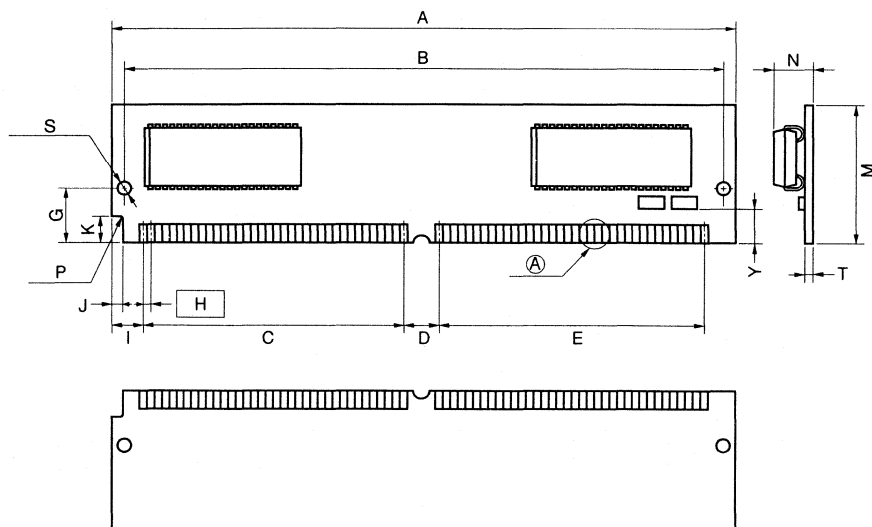
Hidden Refresh Cycle (Write)

★



Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
S	φ3.18	φ0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A46

MOS INTEGRATED CIRCUIT

MC-424000A8 SERIES

4 M-WORD BY 8-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-424000A8 is a 4 194 304 words by 8 bits dynamic RAM module on which 8 pieces of 4M DRAM (μ PD424100) are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4 194 304 words by 8 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000A8-60	60 ns	120 ns	5 280 mW	44 mW (CMOS level input)
MC-424000A8-70	70 ns	140 ns	4 400 mW	
MC-424000A8-80	80 ns	160 ns	3 960 mW	
MC-424000A8-10	100 ns	190 ns	3 520 mW	

- 1 024 refresh cycles/16 ms
- Three refresh methods can be applied : $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 30-pin single in-line memory module (Pin pitch = 2.54 mm)
- All inputs and outputs TTL compatible
- Single +5.0 V $\pm$ 10 % power supply

The information in this document is subject to change without notice.

The mark ★ shows revised points.

Ordering Information

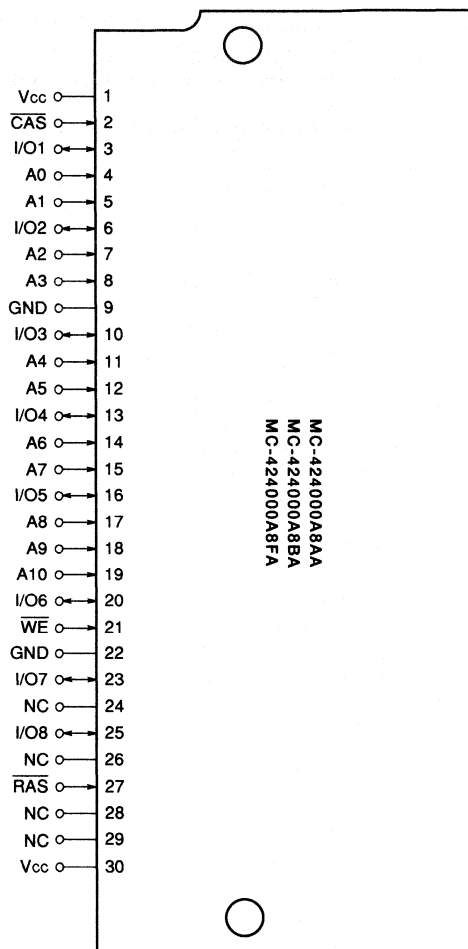
Part number	Access time (MAX.)	Package	Mounted devices
MC-424000A8AA-60	60 ns	30-pin Single In-line Memory Module (Lead Type)	8 pieces of μ PD424100LA (300 mil SOJ) (Single side)
MC-424000A8AA-70	70 ns		
MC-424000A8AA-80	80 ns		
MC-424000A8AA-10	100 ns		
MC-424000A8BA-60	60 ns	30-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	
MC-424000A8BA-70	70 ns		
MC-424000A8BA-80	80 ns		
MC-424000A8BA-10	100 ns		
MC-424000A8FA-60	60 ns	30-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-424000A8FA-70	70 ns		
MC-424000A8FA-80	80 ns		
MC-424000A8FA-10	100 ns		

Quality Grade

Standard

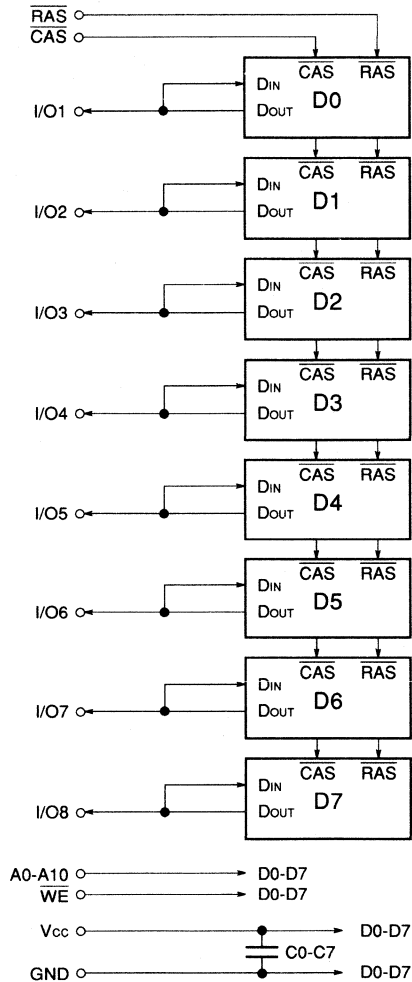
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration (Front view)



- A0-A10 : Address Inputs
- I/O1-I/O8 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- Vcc : Supply Voltage
- GND : Ground
- NC : No Connection

★ Block Diagram



Remark D0 - D7 : $\mu\text{PD424100LA}$

Electrical Specifications Notes 1, 2**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		8	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	A0 - A10, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$			60	pF
Data Input/Output capacitance	$C_{I/O}$	I/O 1-I/O8			15	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	960	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	800		
			$t_{\text{RAC}} = 80 \text{ ns}$	720		
			$t_{\text{RAC}} = 100 \text{ ns}$	640		
Standby current	I _{CC2}	$V_{\text{IH(MIN.)}} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$	$I_o = 0 \text{ mA}$	16	mA	
		$V_{\text{CC}} - 0.2 \text{ V} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$	$I_o = 0 \text{ mA}$	8		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $V_{\text{IH(MIN.)}} \leq \overline{\text{CAS}}$ $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	960	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	800		
			$t_{\text{RAC}} = 80 \text{ ns}$	720		
			$t_{\text{RAC}} = 100 \text{ ns}$	640		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{CAS}}$ Cycling $\text{RAS} \leq V_{\text{IL(MAX.)}}$ $t_{\text{PC}} = t_{\text{PC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	720	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	640		
			$t_{\text{RAC}} = 80 \text{ ns}$	560		
			$t_{\text{RAC}} = 100 \text{ ns}$	480		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	960	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	800		
			$t_{\text{RAC}} = 80 \text{ ns}$	720		
			$t_{\text{RAC}} = 100 \text{ ns}$	640		
Input leakage current	I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	Outputs are disabled (Hi-Z) $V_o = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	

AC Characteristics

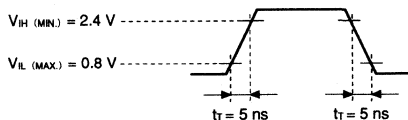
(Recommended Operating Conditions unless otherwise noted) Notes 5, 6

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		$t_{RAC} = 80 \text{ ns}$		$t_{RAC} = 100 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t_{RC}	120		140		160		190		ns	7
Fast Page Mode Cycle Time (Read or Write)	t_{PC}	40		45		50		60		ns	7
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	8, 9
Access Time from $\overline{CAS}$ (Falling Edge)	t_{CAC}		15		20		20		25	ns	8, 9
Access Time from Column Address	t_{AA}		30		35		40		50	ns	8, 9
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45		55	ns	9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	17	50	ns	8
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay Time ($\overline{CAS}$)	t_{OFF}	0	15	0	15	0	20	0	25	ns	10
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ Pulse Width (Random Read, Write Cycle)	t_{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		20		20		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	25	75	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		10		ns	11
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		50		ns	
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	12
Write Command Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		20		ns	13
Data-in Setup Time	t_{DS}	0		0		0		0		ns	14
Data-in Hold Time	t_{DH}	15		15		15		20		ns	14
$\overline{WE}$ Command Setup Time	t_{WCS}	0		0		0		0		ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CHR}	15		15		15		20		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		20		ns	
Refresh Time	t_{REF}		16		16		16		16	ms	

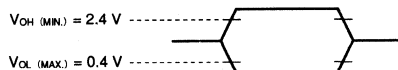
Notes

1. All voltages are referenced to GND.
2. An initial pause of 100 μ s is required after power up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles are required.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on trc and tpc . Specified values are obtained with outputs open.
4. Address can be changed once or less while $\text{RAS} = \text{VIL}$ and $\text{CAS} = \text{VIH}$.
5. AC measurements assume $\text{tr} = 5$ ns.
6. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



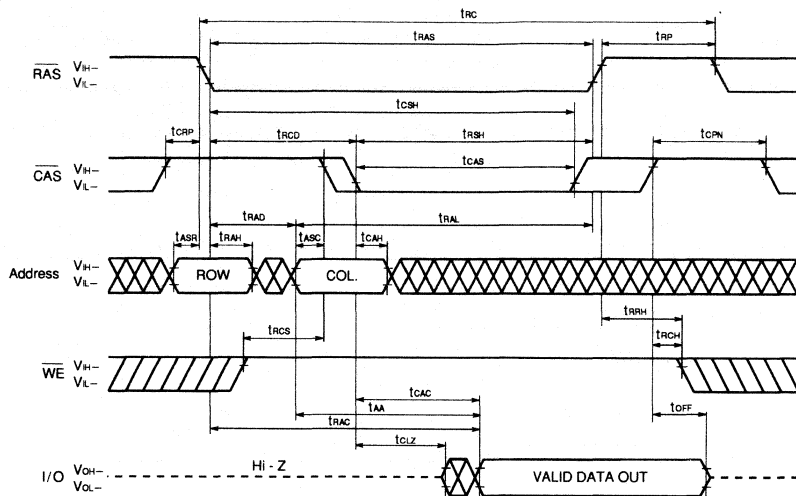
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_a = 0$ to 70°C) is assured.
8. In random read cycle, the access time is changed by the conditions of trAD and trCD as follows.

Condition	Access Time
$\text{trAD} \leq \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\text{trAD} (\text{MAX.}) \leq \text{trAD}$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$
$\text{trCD} (\text{MAX.}) \leq \text{trCD}$	$\text{tCAC} (\text{MAX.})$

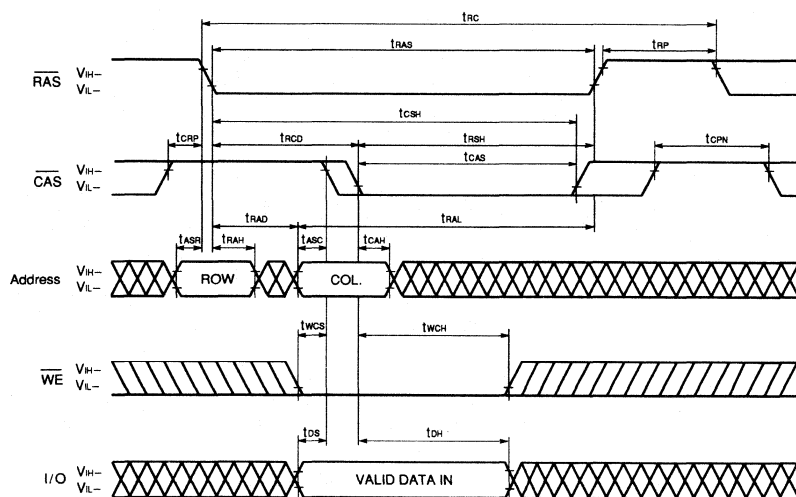
$\text{trAD} (\text{MAX.})$ and $\text{trCD} (\text{MAX.})$ indicate the points which the access time changes and are not the limits of operation.

9. Loading conditions are 2 TTL and 100 pF.
10. $\text{toFF} (\text{MAX.})$ defines the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL} .
11. $\text{tcRP} (\text{MIN.})$ requirement should be applicable for $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycles preceded by any cycles.
12. Either $\text{trCH} (\text{MIN.})$ or $\text{trRH} (\text{MIN.})$ must be satisfied for a read cycle.
13. In early write cycles, $\text{twCH} (\text{MIN.})$ should be satisfied.
14. This specification is referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{WE}}$ falling edge in late write or read modify write cycles.
15. twCS is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $\text{twCS} (\text{MIN.}) \leq \text{twCS}$, the cycle is an early write cycle and the data out pins will remain Hi-Z through the entire cycle.

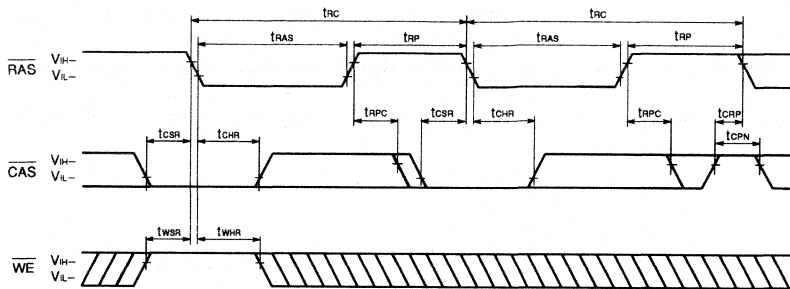
READ CYCLE



EARLY WRITE CYCLE

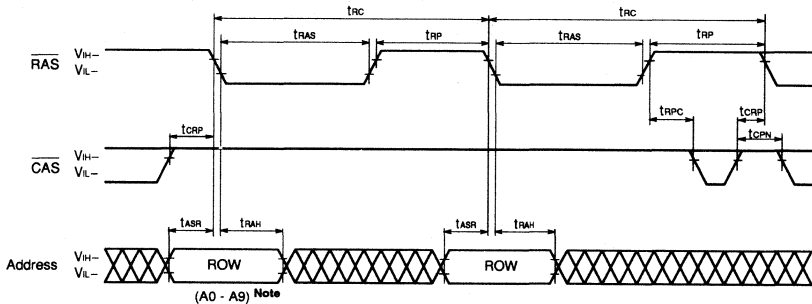


CAS BEFORE RAS REFRESH CYCLE



Remark Address = Don't care I/O = Hi - Z

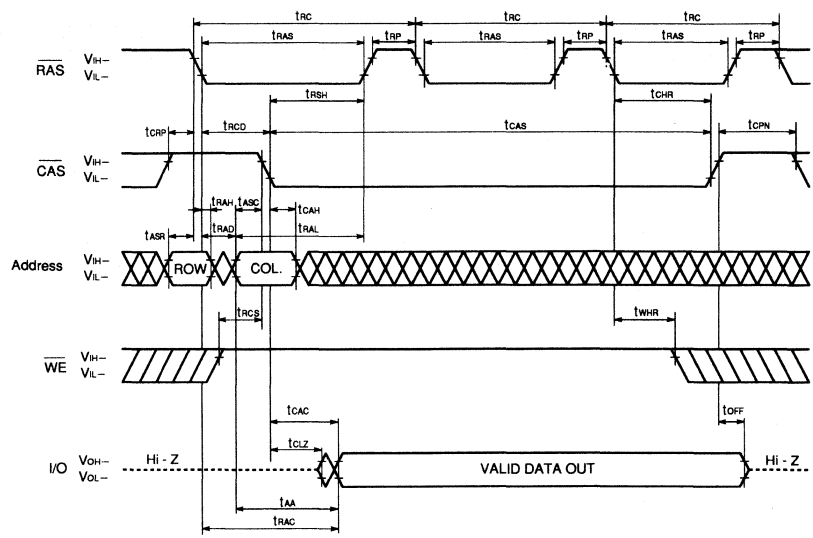
RAS ONLY REFRESH CYCLE



Note Although A10 is not necessary for refreshing, the specifications of both tASR and tRAH are defined in RAS only refresh cycle.

Remark WE = Don't care I/O = Hi - Z

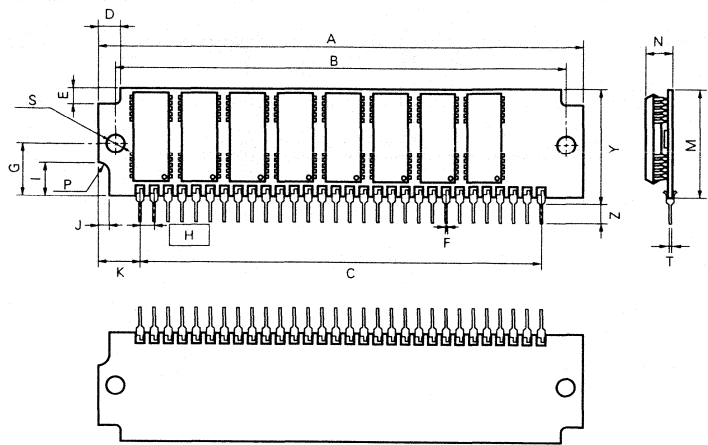
HIDDEN REFRESH CYCLE





Package Drawings
MC-424000A8AA

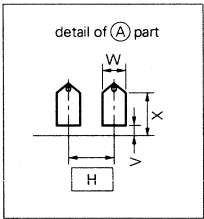
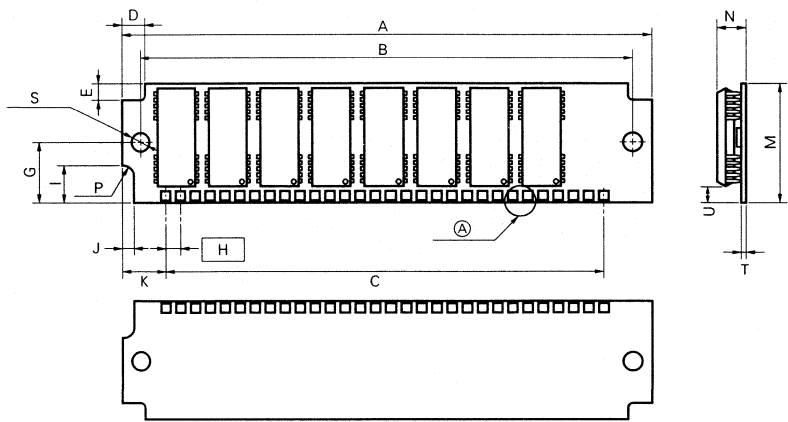
30 PIN SINGLE IN-LINE MODULE (LEAD TYPE)



M30A-100A3-1

ITEM	MILLIMETERS	INCHES
A	88.9±0.13	3.500±0.006
B	82.14	3.234
C	73.66	2.900
D	3.56	0.140
E	3.5	0.138
F	0.5	0.020
G	10.16	0.400
H	2.54 (T.P.)	0.100 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	7.62	0.300
M	20.3	0.799
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	Ø3.18	Ø0.125
T	0.25	0.010
Y	22.26 MAX.	0.877 MAX.
Z	3.4±0.5	0.134±0.020

MC-424000A8BA, 424000A8FA
30 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



M30B-100A3-2

ITEM	MILLIMETERS	INCHES
A	88.9±0.13	3.500±0.006
B	82.14	3.234
C	73.66	2.900
D	3.56	0.140
E	3.5	0.138
G	10.16	0.400
H	2.54 (T.P.)	0.100 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	7.62	0.300
M	20.3	0.799
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	φ3.18	φ0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	2.54 MIN.	0.100 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.8±0.05	0.071 ^{+0.002} _{-0.003}
X	2.1 MIN.	0.082 MIN.

MOS INTEGRATED CIRCUIT

MC-42512A32 SERIES

512 K-WORD BY 32-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-42512A32 is a 524 288 words by 32 bits dynamic RAM module on which 4 pieces of 4M DRAM (μ PD424260) are assembled. ★

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 524 288 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42512A32-70	70 ns	130 ns	1 995 mW	21 mW
MC-42512A32-80	80 ns	150 ns	1 838 mW	(CMOS level input)

- 512 refresh cycle/8 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch=1.27 mm)
- Single +5.0 V $\pm$ 5 % power supply
- Access time can be distinguished with characteristics of PD-pins (PD0-PD3)

The information in this document is subject to change without notice.

The mark ★ shows revised points.

★ Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42512A32BA-70	70 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	4 pieces of μ PD424260LE (400 mil SOJ) [Double side]
MC-42512A32BA-80	80 ns		
MC-42512A32FA-70	70 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-42512A32FA-80	80 ns		

Quality Grade

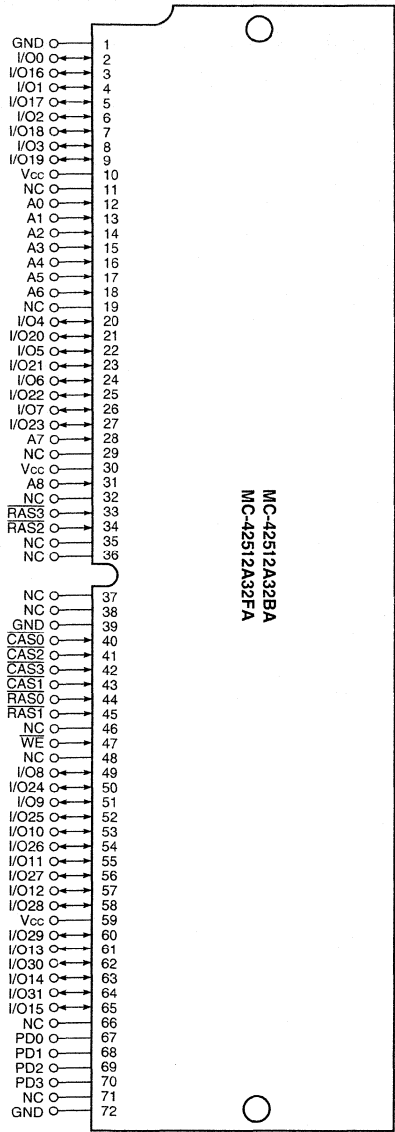
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration



72-pin Single In-line Memory Module Socket Type (Edge Connector: Solder coating, Gold plating)

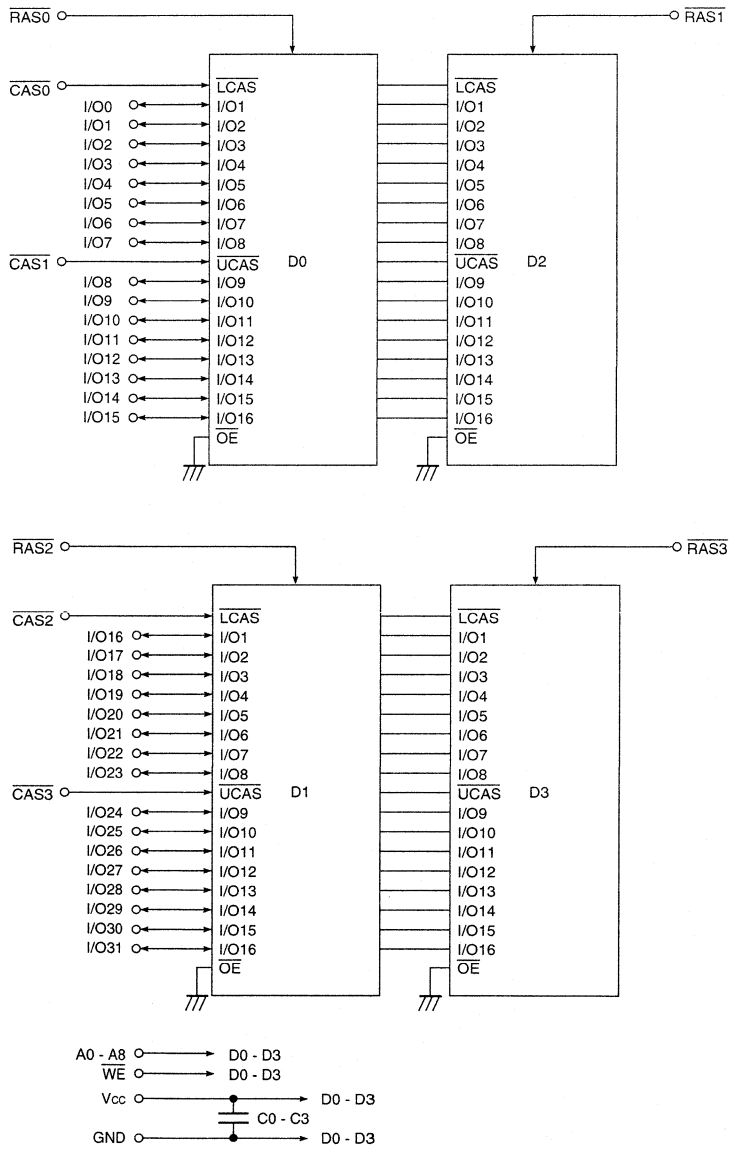


- A0-A8 : Address Inputs
- I/O0-I/O31 : Data Inputs/Outputs
- CAS0-CAS3 : Column Address Strobe
- RAS0-RAS3 : Row Address Strobe
- WE : Write Enable
- Vcc : Power Supply
- GND : Ground
- NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time	
		70 ns	80 ns
PD0	67	NC	NC
PD1	68	GND	GND
PD2	69	GND	NC
PD3	70	NC	GND

★ Block Diagram



Remark D0 - D3 : μ PD424260LE

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		4	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.75	5.0	5.25	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	A0 to A8			40	pF
	C_{I2}	$\overline{WE}$			48	
	C_{I3}	$RAS0 - RAS3$			22	
	C_{I4}	$CAS0 - CAS3$			29	
Data Input/Output Capacitance	$C_{I/O}$	I/O			24	pF

★ DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc} (\text{MIN.})$ $\text{I}_\text{o} = 0 \text{ mA}$	$\text{trAC} = 70 \text{ ns}$		380	mA	3, 4, 7
			$\text{trAC} = 80 \text{ ns}$		350		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq \text{V}_{\text{IH}} (\text{MIN.})$ $\overline{\text{RAS}}, \overline{\text{CAS}} \geq \text{V}_{\text{CC}} - 0.2 \text{ V}$	$\text{I}_\text{o} = 0 \text{ mA}$		8	mA	
			$\text{I}_\text{o} = 0 \text{ mA}$		4		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq \text{V}_{\text{IH}} (\text{MIN.})$ $\text{trc} = \text{trc} (\text{MIN.})$ $\text{I}_\text{o} = 0 \text{ mA}$	$\text{trAC} = 70 \text{ ns}$		380	mA	3,4,5,7
			$\text{trAC} = 80 \text{ ns}$		350		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq \text{V}_{\text{IL}} (\text{MAX.})$ $\overline{\text{CAS}}$ Cycling $\text{trPC} = \text{trPC} (\text{MIN.})$ $\text{I}_\text{o} = 0 \text{ mA}$	$\text{trAC} = 70 \text{ ns}$		340	mA	3, 4, 6
			$\text{trAC} = 80 \text{ ns}$		320		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc} (\text{MIN.})$ $\text{I}_\text{o} = 0 \text{ mA}$	$\text{trAC} = 70 \text{ ns}$		380	mA	3, 4
			$\text{trAC} = 80 \text{ ns}$		350		
Input leakage current	I _{I (L)}	$\text{V}_\text{I} = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V		-10	+10	μA	
Output leakage current	I _{O (L)}	Output is disabled (Hi-Z) $\text{V}_\text{O} = 0 \text{ to } 5.5 \text{ V}$		-10	+10	μA	
High level output voltage	V _{OH}	$\text{I}_\text{o} = -5.0 \text{ mA}$		2.4		V	
Low level output voltage	V _{OL}	$\text{I}_\text{o} = 4.2 \text{ mA}$			0.4	V	

AC Characteristics

(Recommended Operating Conditions unless otherwise noted) Notes 8, 9

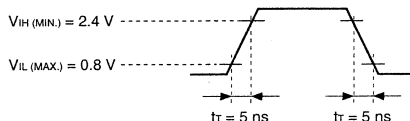
Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	45		50		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		70	80		ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		20	20		ns	10, 11
Access Time from Column Address	t _{AA}		35	40		ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		40	45		ns	11
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RS}	70	10 000	80	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RSP}	70	125 000	80	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20		20		ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	70		80		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	20	10 000	20	10 000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	50	20	60	ns	10
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	35	15	40	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		ns	13
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		ns	
Row Address Setup Time	t _{ASR}	0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		ns	
Column Address Setup Time	t _{ASC}	0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		ns	15
Data-in Setup Time	t _{DS}	0		0		ns	16
Data-in Hold Time	t _{DH}	15		20		ns	16
Write Command Setup Time	t _{WCS}	0		0		ns	17
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	10		10		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	15		15		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40		45		ns	
Refresh Time	t _{REF}		8		8	ms	

★

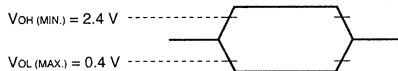
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on cycle rates (trc and tpc).
4. Specified values are obtained with outputs unloaded.
5. Icc3 is measured assuming that all column address inputs are held at either high or low.
6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.).
8. AC measurements assume $\text{tr} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



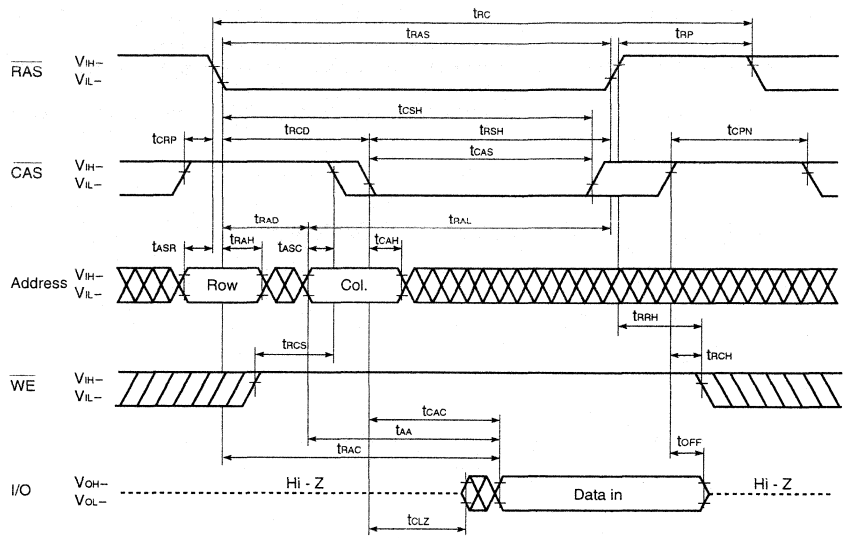
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD}(\text{MAX.})$ and $\text{trCD} \leq \text{trCD}(\text{MAX.})$	$\text{trAC}(\text{MAX.})$	$\text{trAC}(\text{MAX.})$
$\text{trAD} > \text{trAD}(\text{MAX.})$ and $\text{trCD} \leq \text{trCD}(\text{MAX.})$	$\text{tAA}(\text{MAX.})$	$\text{trAD} + \text{tAA}(\text{MAX.})$
$\text{trCD} > \text{trCD}(\text{MAX.})$	$\text{tCAC}(\text{MAX.})$	$\text{trCD} + \text{tCAC}(\text{MAX.})$

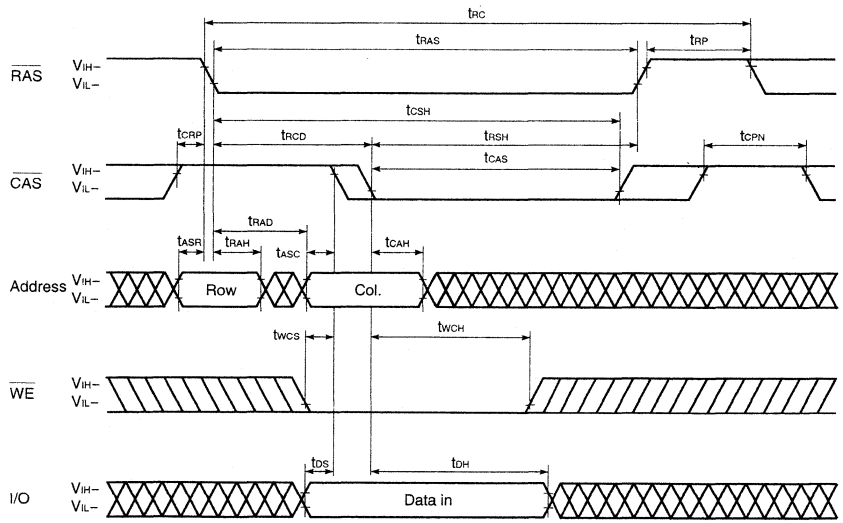
$\text{trAD}(\text{MAX.})$ and $\text{trCD}(\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD}(\text{MAX.})$ and $\text{trCD} \geq \text{trCD}(\text{MAX.})$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. $\text{tOFF}(\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $\text{tCRP}(\text{MIN.})$ requirement should be applied for $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycles preceded by any cycles.
14. Either $\text{trCH}(\text{MIN.})$ or $\text{trRH}(\text{MIN.})$ should be met in read cycles.
15. In early write cycles, $\text{twCH}(\text{MIN.})$ should be met.
16. $\text{tDS}(\text{MIN.})$ and $\text{tDH}(\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $\text{twCS} \geq \text{twCS}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

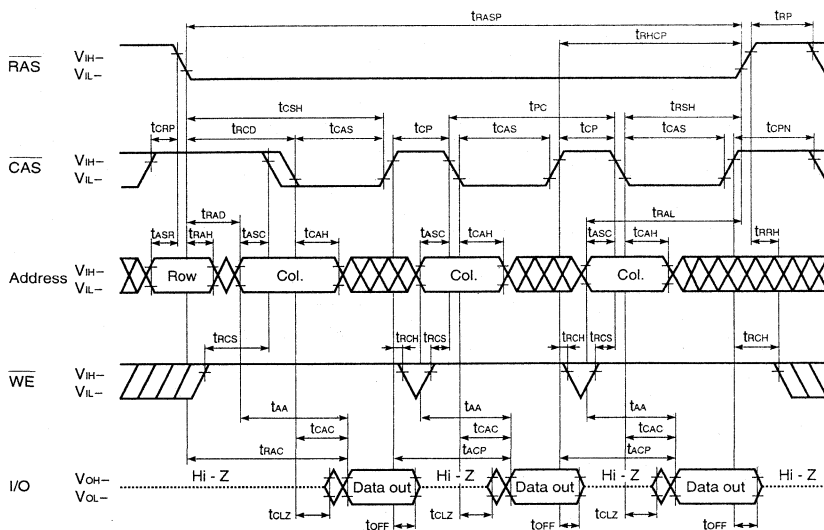
Read Cycle



Early Write Cycle

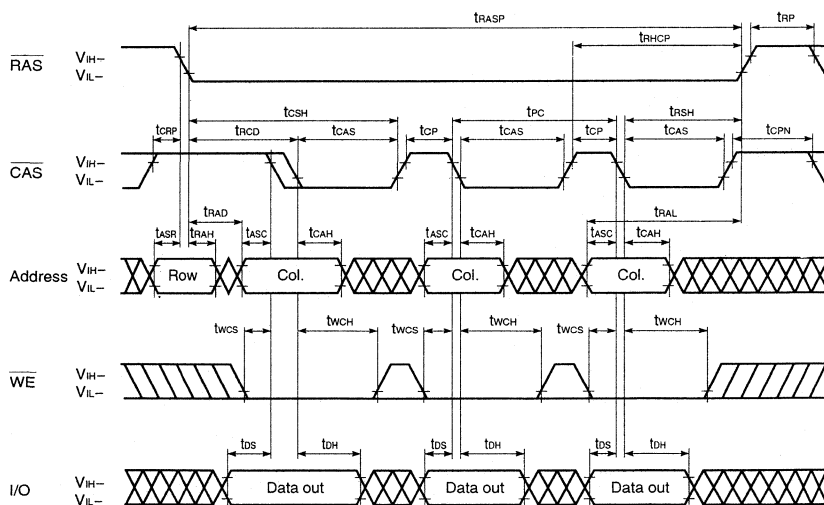


Fast Page Mode Read Cycle



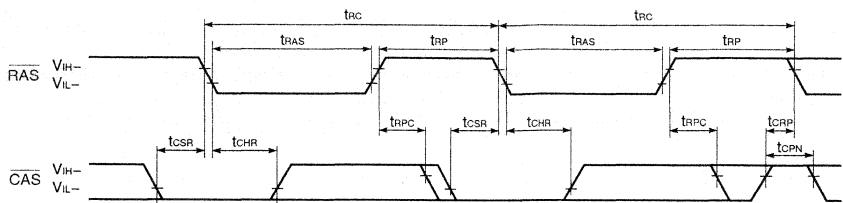
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



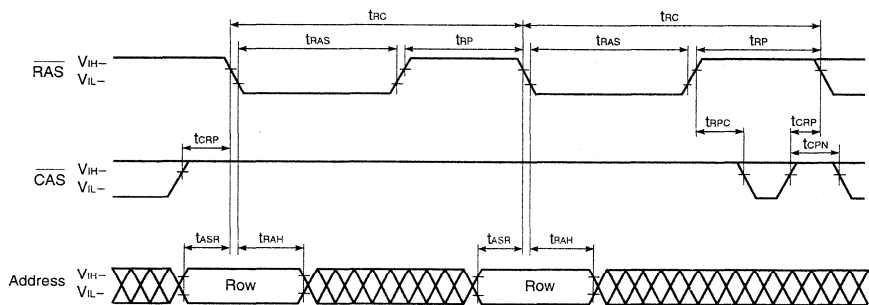
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



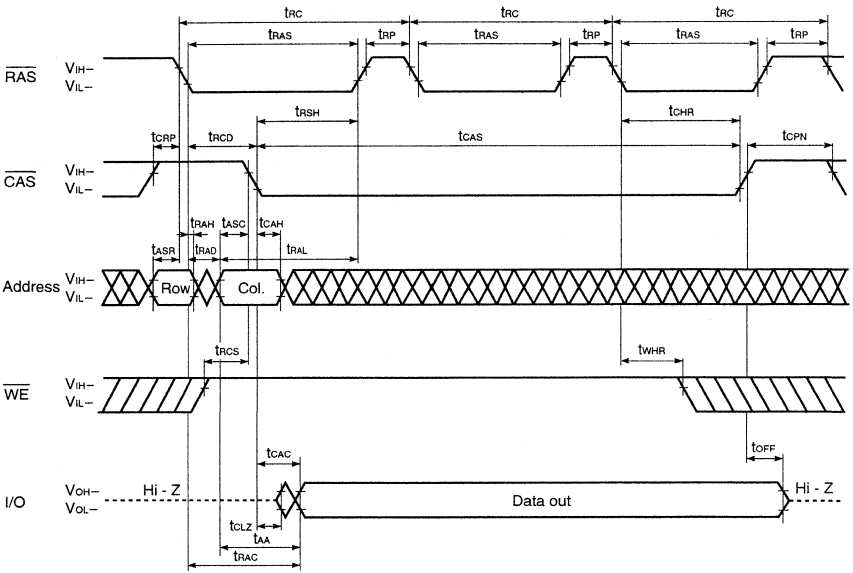
Remark Address, $\overline{\text{WE}}$ = Don't care I/O = Hi - Z

RAS Only Refresh Cycle



Remark $\overline{\text{WE}}$ = Don't care I/O = Hi - Z

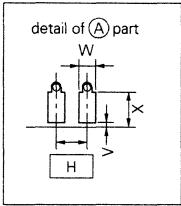
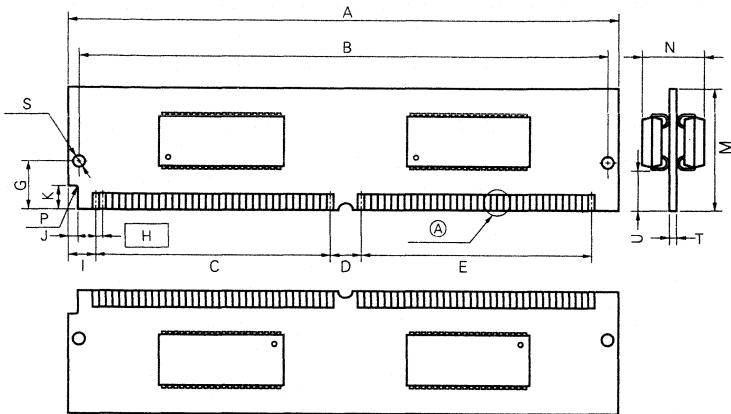
Hidden Refresh Cycle



Package Drawing



MC-42512A32BA, 42512A32FA
72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



M72B-50A39-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R 1.57	R 0.062
S	Ø3.18	Ø0.125
T	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	8.5 MIN.	0.334 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

MOS INTEGRATED CIRCUIT

MC-421000A8, 421000A9 SERIES

1 M-WORD BY 8-BIT, 1 M-WORD BY 9-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000A8 is a 1 048 576 words by 8 bits dynamic RAM module on which 2 pieces of 4 M DRAM (μ PD424400LA) are assembled.

The MC-421000A9 is a 1 048 576 words by 9 bits dynamic RAM module on which 2 pieces of 4 M DRAM (μ PD424400LA) and 1 piece of 1 M DRAM (μ PD421000LA) are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1 048 576 words by 8 bits organization (MC-421000A8)
- 1 048 576 words by 9 bits organization (MC-421000A9)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000A8-60	60 ns	120 ns	1 320 mW	11 mW (CMOS level input)
MC-421000A8-70	70 ns	140 ns	1 100 mW	
MC-421000A8-80	80 ns	160 ns	990 mW	
MC-421000A8-100	100 ns	190 ns	880 mW	
MC-421000A9-60	60 ns	120 ns	1 815 mW	16.5 mW (CMOS level input)
MC-421000A9-70	70 ns	140 ns	1 540 mW	
MC-421000A9-80	80 ns	160 ns	1 375 mW	
MC-421000A9-100	100 ns	190 ns	1 210 mW	

- 1 024 refresh cycles/16 ms
- Three refresh modes are available: $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 30-pin single in-line memory module (Pin pitch=2.54 mm)
- All inputs and outputs are TTL compatible
- Single +5.0 V $\pm$ 10 % power supply

The information in this document is subject to change without notice.

The mark ★ shows revised points.

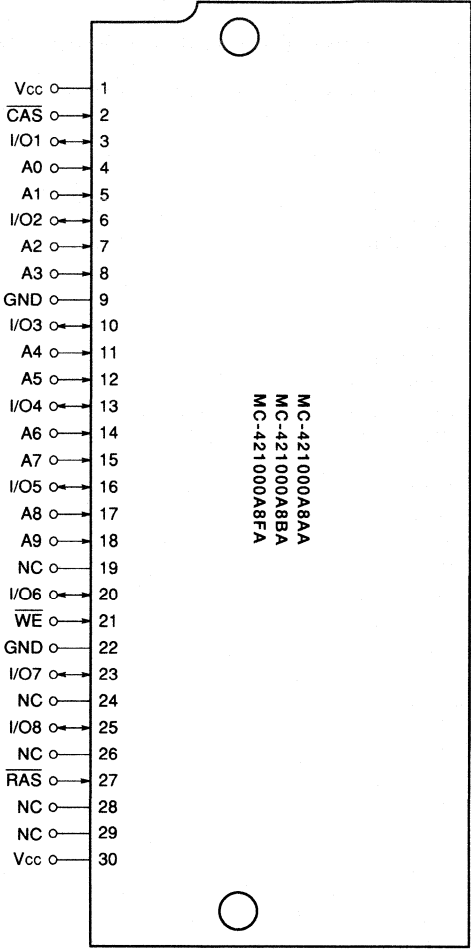
★ **Ordering Information**

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A8AA-60	60 ns	30-pin Single In-line Memory Module (Lead Type)	2 pieces of μ PD424400LA (300 mil SOJ) [Single side]
MC-421000A8AA-70	70 ns		
MC-421000A8AA-80	80 ns		
MC-421000A8AA-10	100 ns		
MC-421000A8BA-60	60 ns	30-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	
MC-421000A8BA-70	70 ns		
MC-421000A8BA-80	80 ns		
MC-421000A8BA-10	100 ns		
MC-421000A8FA-60	60 ns	30-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A8FA-70	70 ns		
MC-421000A8FA-80	80 ns		
MC-421000A8FA-10	100 ns		
MC-421000A9AA-60	60 ns	30-pin Single In-line Memory Module (Lead Type)	2 pieces of μ PD424400LA (300 mil SOJ) 1 piece of μ PD421000LA (300 mil SOJ) [Single side]
MC-421000A9AA-70	70 ns		
MC-421000A9AA-80	80 ns		
MC-421000A9AA-10	100 ns		
MC-421000A9BA-60	60 ns	30-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	
MC-421000A9BA-70	70 ns		
MC-421000A9BA-80	80 ns		
MC-421000A9BA-10	100 ns		
MC-421000A9FA-60	60 ns	30-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A9FA-70	70 ns		
MC-421000A9FA-80	80 ns		
MC-421000A9FA-10	100 ns		

Quality Grade

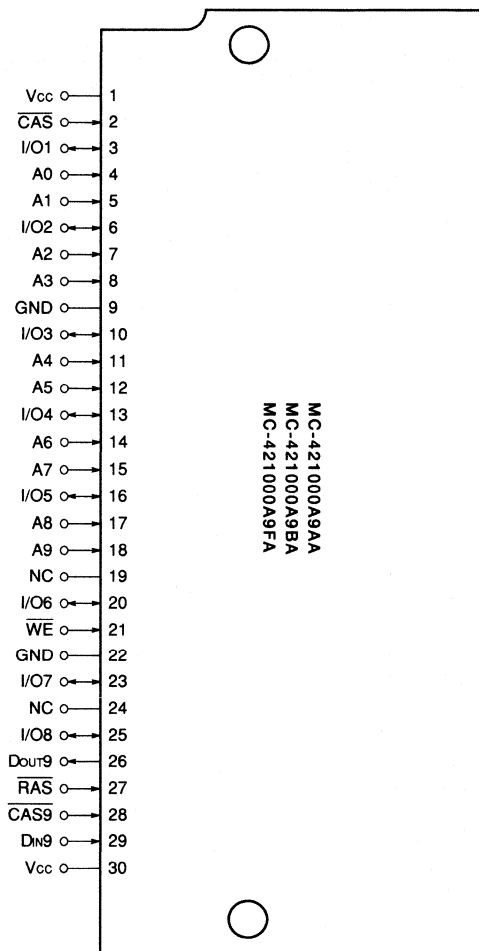
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number 1EI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Front View)**[MC-421000A8 series]**

- A0-A9 : Address Inputs
I/O1-I/O8 : Data Inputs/Outputs
 $\overline{\text{RAS}}$: Row Address Strobe
 $\overline{\text{CAS}}$: Column Address Strobe
 $\overline{\text{WE}}$: Write Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

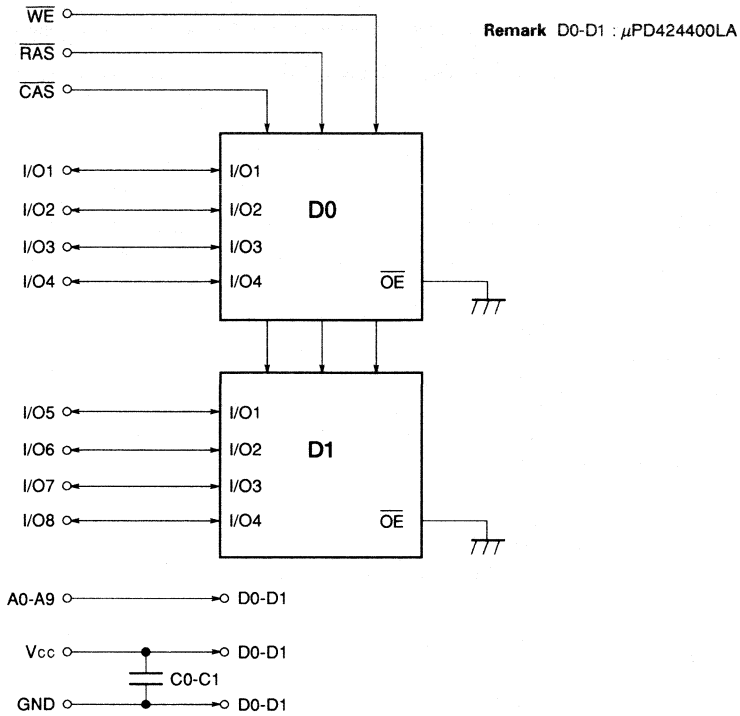
[MC-421000A9 series]



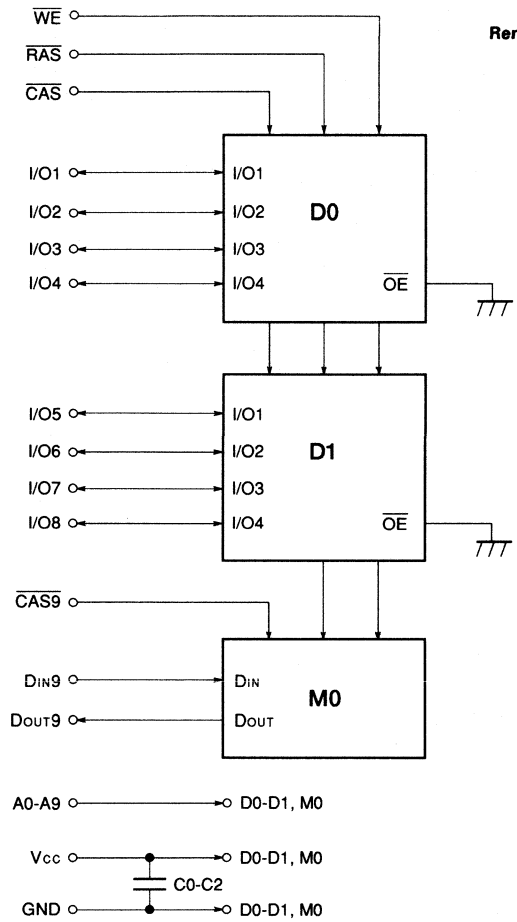
A0-A9 : Address Inputs
 I/O1-I/O8 : Data Inputs/Outputs
 DIN9 : Data Input
 DOUT9 : Data Output
 $\overline{\text{RAS}}$: Row Address Strobe
 $\overline{\text{CAS}}$, $\overline{\text{CAS9}}$: Column Address Strobe
 $\overline{\text{WE}}$: Write Enable
 Vcc : Power Supply
 GND : Ground
 NC : No Connection

Block Diagrams

[MC-421000A8 series]



[MC-421000A9 series]



Remark D0-D1 : μ PD424400LA
M0 : μ PD421000LA

Electrical Specifications Notes1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-421000A8	2	W
		MC-421000A9	3	
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

[MC-421000A8 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	A0-A9, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$			24	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1-I/O8			12	pF

[MC-421000A9 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0-A9, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$			31	pF
	C_{I2}	$\overline{\text{CAS9}}$, D_{IN9}			17	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1-I/O8			12	pF
Data Output capacitance	C_O	D_{OUT9}			17	pF

★ **DC Characteristics (Recommended Operating Conditions unless otherwise noted)**
[MC-421000A8 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}, \overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	240	mA	3,4
			$t_{RAC} = 70 \text{ ns}$	200		
			$t_{RAC} = 80 \text{ ns}$	180		
			$t_{RAC} = 100 \text{ ns}$	160		
Standby current	I_{CC2}	$V_{IH(MIN.)} \leq \overline{RAS}, \overline{CAS}$ $I_O = 0 \text{ mA}$		4	mA	
		$V_{CC} - 0.2 \text{ V} \leq \overline{RAS}, \overline{CAS}$ $I_O = 0 \text{ mA}$		2		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $V_{IH(MIN.)} \leq \overline{CAS}$ $t_{RC} = t_{RC(MIN.)}$ $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	240	mA	3,4
			$t_{RAC} = 70 \text{ ns}$	200		
			$t_{RAC} = 80 \text{ ns}$	180		
			$t_{RAC} = 100 \text{ ns}$	160		
Operating current (Fast page mode)	I_{CC4}	$\overline{CAS}$ Cycling $\overline{RAS} \leq V_{IL(MAX.)}$ $t_{PC} = t_{PC(MIN.)}$ $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	180	mA	3,4
			$t_{RAC} = 70 \text{ ns}$	160		
			$t_{RAC} = 80 \text{ ns}$	140		
			$t_{RAC} = 100 \text{ ns}$	120		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	240	mA	3,4
			$t_{RAC} = 70 \text{ ns}$	200		
			$t_{RAC} = 80 \text{ ns}$	180		
			$t_{RAC} = 100 \text{ ns}$	160		
Input leakage current	$I_{I(L)}$	$V_I = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	$I_{O(L)}$	I/O1-I/O8 are disabled (Hi-Z) $V_O = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V_{OH}	$I_O = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V_{OL}	$I_O = +4.2 \text{ mA}$		0.4	V	

[MC-421000A9 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	330	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	280		
			$t_{\text{RAC}} = 80 \text{ ns}$	250		
			$t_{\text{RAC}} = 100 \text{ ns}$	220		
Standby current	I _{CC2}	$V_{\text{IH(MIN.)}} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$	$I_O = 0 \text{ mA}$	6	mA	
		$V_{\text{CC}} - 0.2 \text{ V} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$	$I_O = 0 \text{ mA}$	3		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $V_{\text{IH(MIN.)}} \leq \overline{\text{CAS}}$ $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	330	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	280		
			$t_{\text{RAC}} = 80 \text{ ns}$	250		
			$t_{\text{RAC}} = 100 \text{ ns}$	220		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{CAS}}$ Cycling $\overline{\text{RAS}} \leq V_{\text{IL(MAX.)}}$ $t_{\text{PC}} = t_{\text{PC(MIN.)}}$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	260	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	230		
			$t_{\text{RAC}} = 80 \text{ ns}$	200		
			$t_{\text{RAC}} = 100 \text{ ns}$	170		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	330	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	280		
			$t_{\text{RAC}} = 80 \text{ ns}$	250		
			$t_{\text{RAC}} = 100 \text{ ns}$	220		
Input leakage current	I _{I(L)}	$V_I = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	$I/O1\text{-}I/O8, D_{out9}$ are disabled (Hi-Z) $V_O = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V _{OH}	$I_O = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_O = +4.2 \text{ mA}$		0.4	V	

★ AC Characteristics

(Recommended Operating Conditions unless otherwise noted) Notes 5, 6

[MC-421000A8 series]

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	120		140		160		190		ns	7
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40		45		50		60		ns	7
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80		100	ns	8, 9
Access Time from $\overline{\text{CAS}}$ (Falling Edge)	t _{CAC}		15		20		20		25	ns	8, 9
Access Time from Column Address	t _{AA}		30		35		40		50	ns	8, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45		55	ns	9
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	17	50	ns	8
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay Time ($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	15	0	20	0	25	ns	10
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	50		60		70		80		ns	
$\overline{\text{RAS}}$ Pulse Width (Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20		20		20		25		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		100		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	25	75	ns	8
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		10		10		ns	11
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		10		10		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		50		ns	
Read Command Setup Time	t _{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		0		ns	12
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		15		20		ns	13
Data-in Setup Time	t _{DS}	0		0		0		0		ns	14
Data-in Hold Time	t _{DH}	15		15		15		20		ns	14
$\overline{\text{WE}}$ Command Setup Time	t _{WCS}	0		0		0		0		ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	t _{CSR}	10		10		10		10		ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	t _{CHR}	15		15		15		20		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		20		ns	
Refresh Time	t _{REF}		16		16		16		16	ms	

[MC-421000A9 series]

(1/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	120		140		160		190		ns	7
Read Write Cycle Time	t _{RWC}	145		155		190		225		ns	7
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40		45		50		60		ns	7
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	65		70		75		90		ns	7
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80		100	ns	8, 9
Access Time from $\overline{\text{CAS}}$ (Falling Edge)	t _{CAC}		20		20		20		25	ns	8, 9
Access Time from Column Address	t _{AA}		30		35		45		50	ns	8, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45		55	ns	9
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	17	50	ns	8
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay Time ($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	15	0	20	0	25	ns	10
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	50		60		70		80		ns	
$\overline{\text{RAS}}$ Pulse Width (Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20		20		20		25		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	20	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		100		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	25	75	ns	8
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		10		10		ns	11
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		10		10		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		17		20		20		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		45		50		ns	
Read Command Setup Time	t _{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		0		ns	12
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		15		20		ns	13
Write Command Pulse Width	t _{WP}	15		15		15		20		ns	13
Data-in Setup Time	t _{DS}	0		0		0		0		ns	14
Data-in Hold Time	t _{DH}	15		15		20		20		ns	14
$\overline{\text{WE}}$ Command Setup Time	t _{WCS}	0		0		0		0		ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	20		20		20		25		ns	15
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	60		70		80		100		ns	15

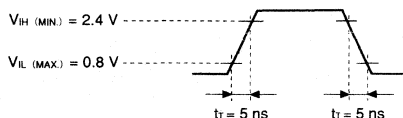
(2/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Precharge Delay Time Referenced to $\overline{\text{WE}}$ (Fast Page Mode)	t _{CPWD}	55		60		70		85		ns	15
Column Address Delay Time Referenced to $\overline{\text{WE}}$	t _{AWD}	30		35		45		50		ns	15
Write Command Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20		20		25		30		ns	
Write Command Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15		15		15		20		ns	
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	t _{CSR}	10		10		10		10		ns	
CAS Hold Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	t _{CHR}	15		15		15		20		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		20		ns	
Refresh Time	t _{REF}		16		16		16		16	ms	

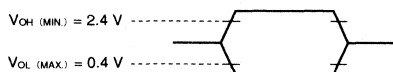
Notes

1. All voltages are referenced to GND.
2. After power-up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles to initialize the internal circuit.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on trc and tpc . Specified values are obtained with outputs open.
4. Address can be changed once or less while $\overline{\text{RAS}} = \text{VIL}$ and $\overline{\text{CAS}} = \text{VIH}$.
5. AC measurements assume $\text{tr} = 5$ ns.
6. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



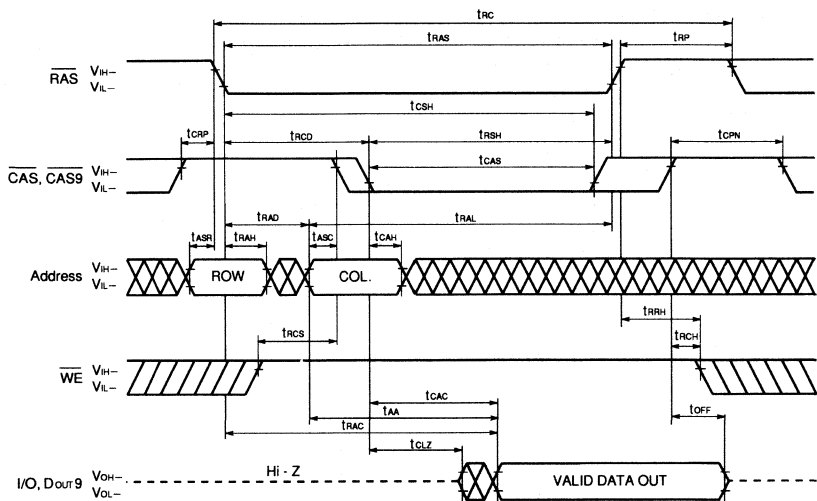
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_a = 0$ to 70°C) is assured.
8. In random read cycle, the access time is changed by the conditions of trAD and trCD as follows.

Condition	Access Time
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)

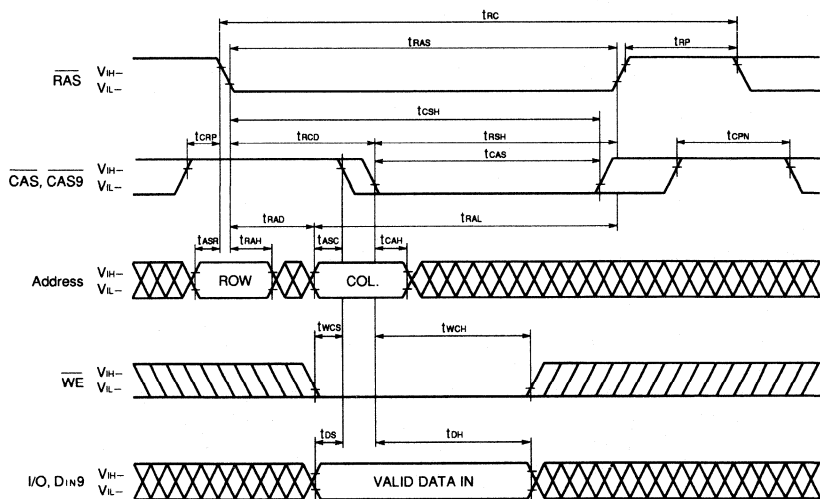
trAD (MAX.) and trCD (MAX.) indicate the points which the access time changes and are not the limits of operation.

9. Loading conditions are 2 TTL and 100 pF.
10. tOFF (MAX.) defines the time at which the output achieves the open-circuit condition and is not referenced to VOH or VOL .
11. tCRP (MIN.) requirement should be applicable for $\overline{\text{RAS}} / \overline{\text{CAS}}$ cycles preceded by any cycles.
12. Either trCH (MIN.) or trRH (MIN.) must be satisfied for a read cycle.
13. tWP (MIN.) is applicable for late write cycle or read modify write cycle. In early write cycles, twCH (MIN.) should be satisfied.
14. tDS (MIN.) and tDH (MIN.) are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{WE}}$ falling edge in late write or read modify write cycles.
15. If $\text{twCS} \geq \text{twCS (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{trWD} \geq \text{trWD (MIN.)}$, $\text{tcWD} \geq \text{tcWD (MIN.)}$, $\text{tAWD} \geq \text{tAWD (MIN.)}$ and $\text{tcpWD} \geq \text{tcpWD (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above condition is met, the state of the data out is indeterminate.

Read Cycle



Early Write Cycle

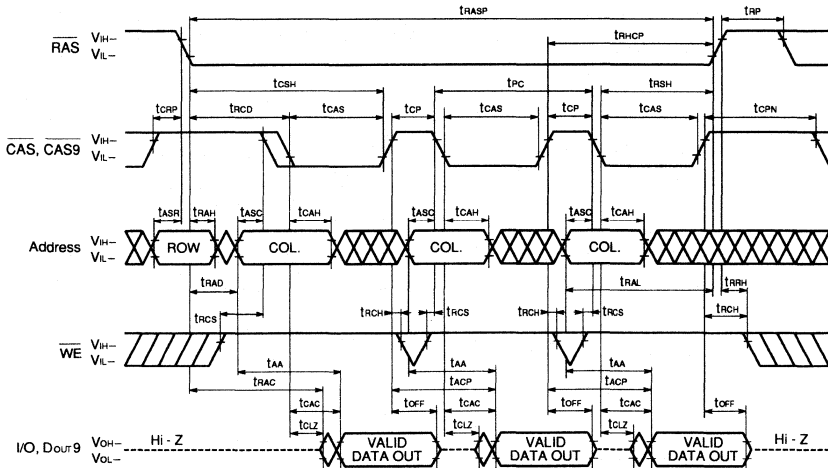


The timing diagram illustrates the relationship between several control and data signals for the 28C01 memory device. The signals shown are:

- RAS** (Row Address Strobe): Active low signal. Timing parameters include t_{RAS} (pulse width), t_{RCD} (delay from RAS to CAS), t_{RSH} (delay from RAS to CS), t_{RP} (delay from RAS to next RAS), and t_{RAD} (delay from RAS to data output).
- CAS9** (Column Address Strobe): Active low signal. Timing parameters include t_{CAS} (pulse width), t_{CWL} (delay from CAS to data output), and t_{CPN} (delay from CAS to next CAS).
- Address**: Data bus signal. It shows **ROW** (row address) and **COL** (column address) periods. Timing parameters include t_{ASR} (setup before RAS), t_{RAH} (hold after RAS), t_{ASC} (setup before CAS), t_{CAH} (hold after CAS), t_{RAL} (delay from RAS to data output), and t_{RWL} (delay from RAS to data output).
- WE** (Write Enable): Active low signal. Timing parameters include t_{RCS} (delay from RAS to WE) and t_{WP} (pulse width).
- DIN9** (Data Input/Output): Data bus signal. It shows **VALID DATA IN** period. Timing parameters include t_{OS} (delay from WE to data output) and t_{DH} (delay from WE to data output).

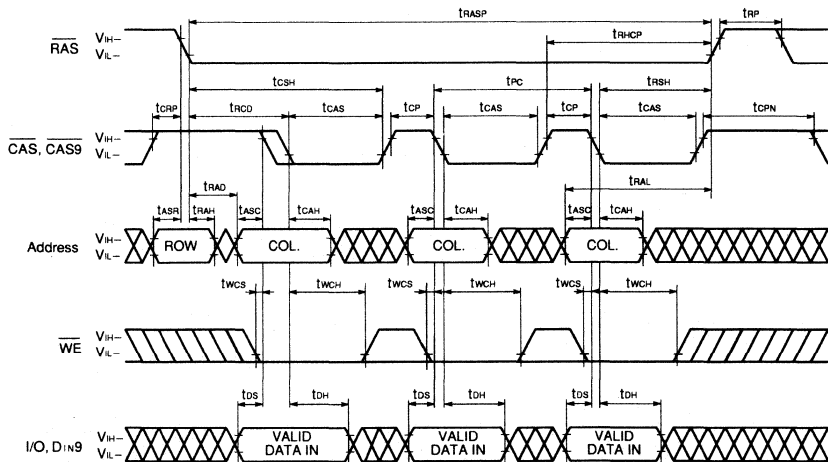
[illegible]

Fast Page Mode Read Cycle



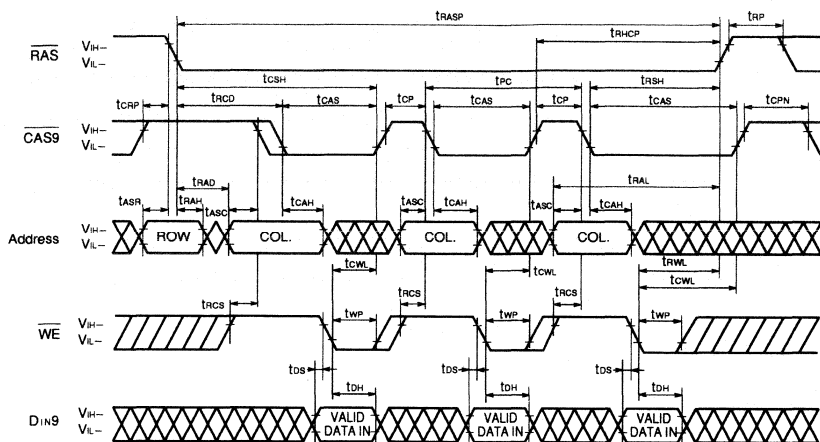
Remark In the fast page mode, read, write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same RAS cycle.

Fast Page Mode Early Write Cycle



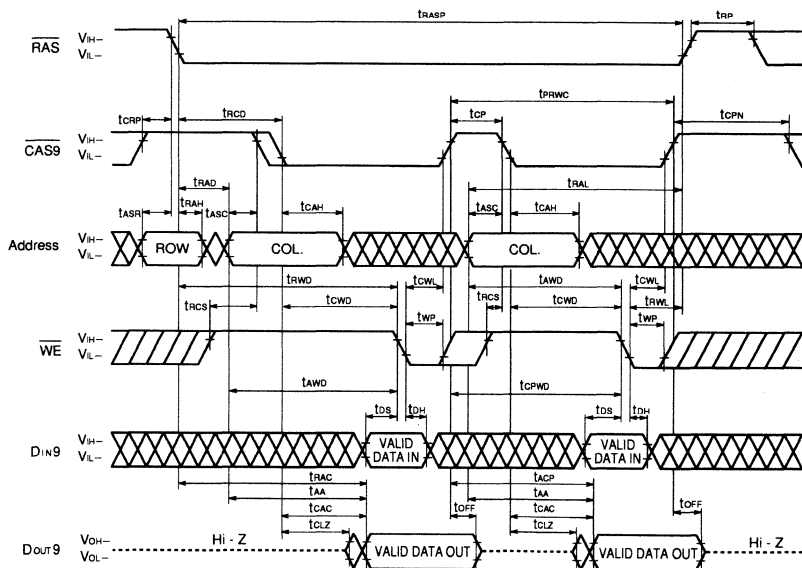
Remark In the fast page mode, read, write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same RAS cycle.

Fast Page Mode Late Write Cycle (Only for the MC-421000A9 series)



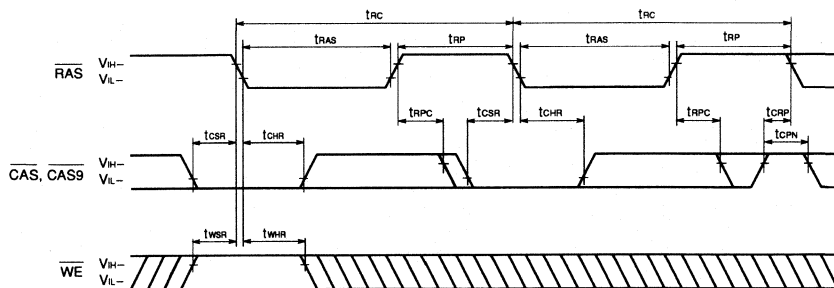
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Read Modify Write Cycle (Only for the MC-421000A9 series)



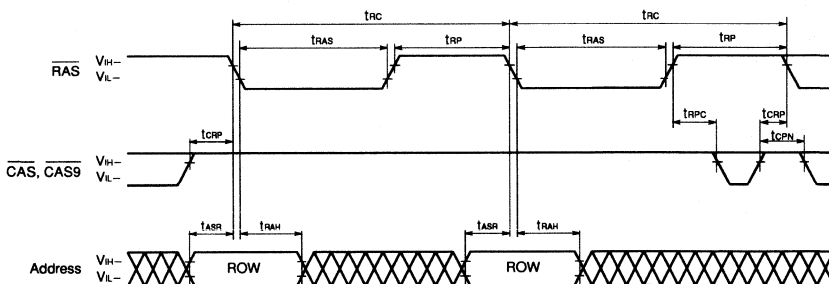
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

★ **CAS Before RAS Refresh Cycle**



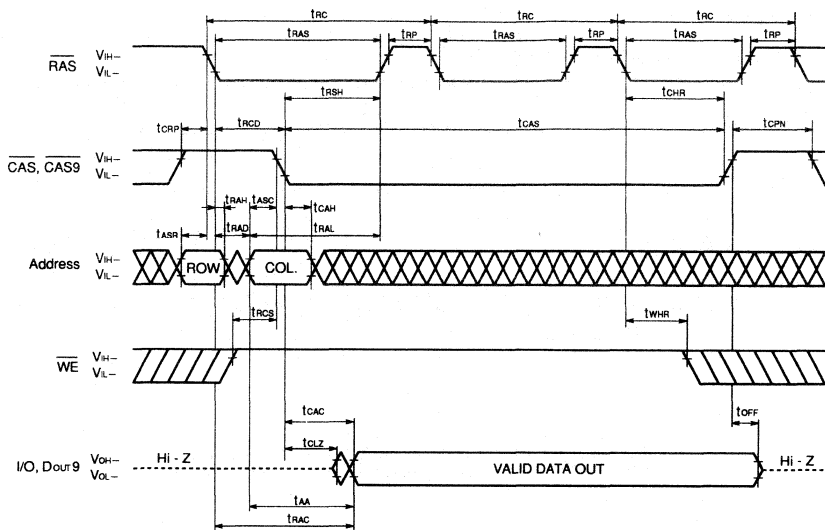
Remark Address, D_{in}9 = Don't care I/O, D_{out}9 = Hi - Z

★ **RAS Only Refresh Cycle**



Remark WE, D_{in}9 = Don't care I/O, D_{out}9 = Hi - Z

Hidden Refresh Cycle

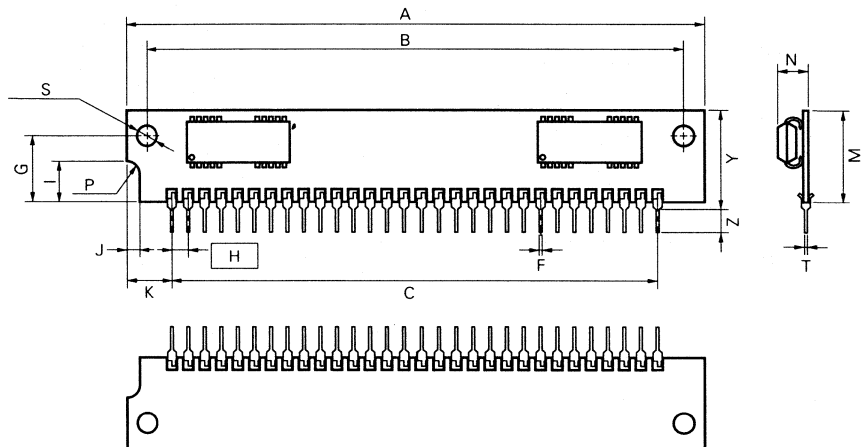


Remark Din9 = Don't care

Package Drawings

MC-421000A8AA

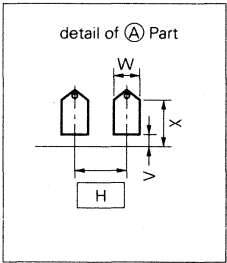
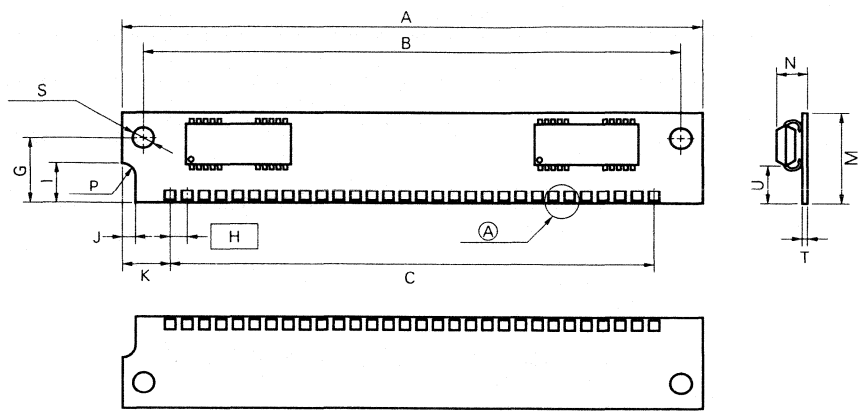
30 PIN SINGLE IN-LINE MODULE (LEAD TYPE)



M30A-100A4-2

ITEM	MILLIMETERS	INCHES
A	88.9±0.13	3.500±0.006
B	82.14	3.234
C	73.66	2.900
F	0.5	0.020
G	10.16	0.400
H	2.54 (T.P.)	0.100 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	7.62	0.300
M	16.51	0.65
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	Ø3.18	Ø0.125
T	0.25	0.010
Y	18.2 MAX.	0.717 MAX.
Z	3.4±0.5	0.134±0.020

MC-421000A8BA, 421000A8FA
30 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)

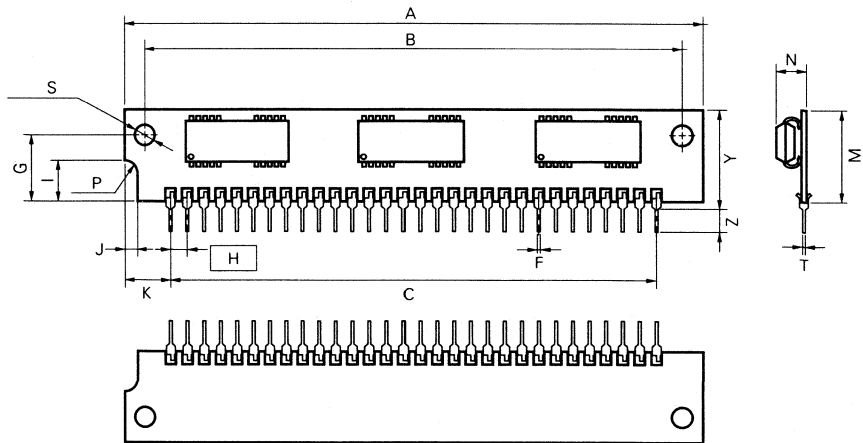


M30B-100A4-2

ITEM	MILLIMETERS	INCHES
A	88.9±0.13	3.500±0.006
B	82.14	3.234
C	73.66	2.900
G	10.16	0.400
H	2.54 (T.P.)	0.100 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	7.62	0.300
M	16.51	0.65
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	φ3.18	φ0.125
T	1.27±0.08	0.050±0.004
U	4.86 MIN.	0.191 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.8±0.05	0.071 ^{+0.002} _{-0.003}
X	2.1 MIN.	0.082 MIN.

MC-421000A9AA

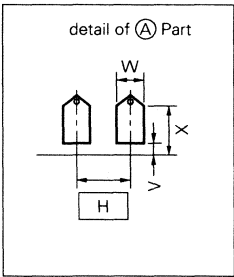
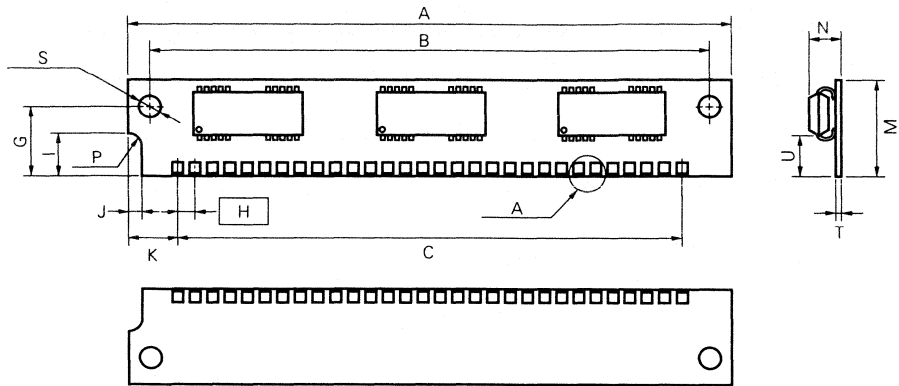
30 PIN SINGLE IN-LINE MODULE (LEAD TYPE)



M30A-100A5-2

ITEM	MILLIMETERS	INCHES
A	88.9±0.13	3.500±0.006
B	82.14	3.234
C	73.66	2.900
F	0.5	0.020
G	10.16	0.400
H	2.54 (T.P.)	0.100 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	7.62	0.300
M	16.51	0.65
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	Ø3.18	Ø0.125
T	0.25	0.010
Y	18.2 MAX	0.717 MAX.
Z	3.4±0.5	0.134±0.020

MC-421000A9BA, 421000A9FA
30 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



M30B-100A5-2

ITEM	MILLIMETERS	INCHES
A	88.9±0.13	3.500±0.006
B	82.14	3.234
C	73.66	2.900
G	10.16	0.400
H	2.54 (T.P.)	0.100 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	7.62	0.300
M	16.51	0.65
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	φ3.18	φ0.125
T	1.27±0.08	0.050±0.004
U	4.86 MIN.	0.191 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.8±0.05	0.071 ^{+0.002} _{-0.003}
X	2.1 MIN.	0.082 MIN.

MOS INTEGRATED CIRCUIT

MC-42S4000LAB32S SERIES

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S4000LAB32S series is a 4,194,304 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 16 M DRAM: μ PD42S17800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 4,194,304 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S4000LAB32S-A60	60 ns	110 ns	1,458 mW	4.32 mW (CMOS level input)
MC-42S4000LAB32S-A70	70 ns	130 ns	1,314 mW	
MC-42S4000LAB32S-A80	80 ns	150 ns	1,170 mW	

- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V $\pm$ 0.3 V power supply

Ordering Information

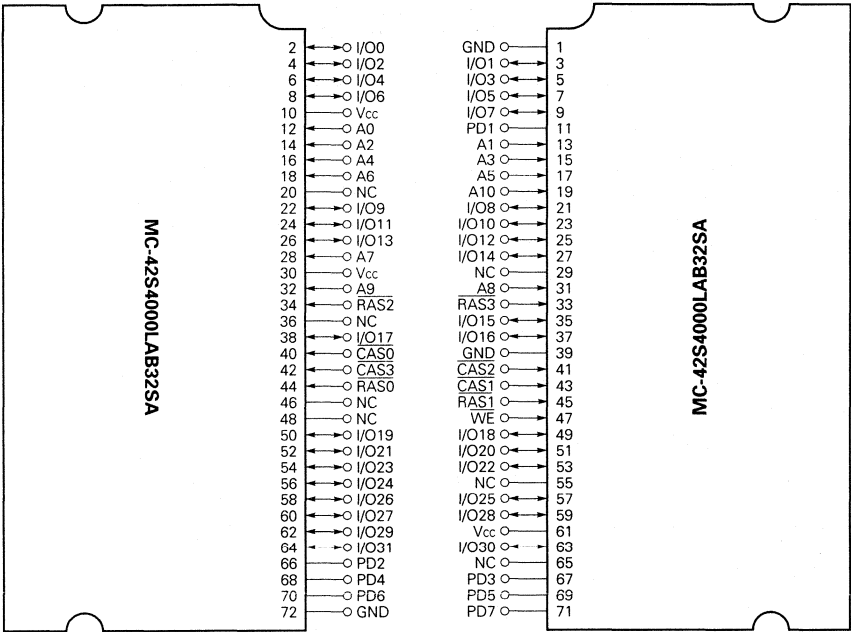
★

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S4000LAB32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μ PD42S17800LG5 (400 mil TSOP (II)) [Double side]
MC-42S4000LAB32SA-A70	70 ns		
MC-42S4000LAB32SA-A80	80 ns		

The information in this document is subject to change without notice.

Pin Configuration

★ 72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)

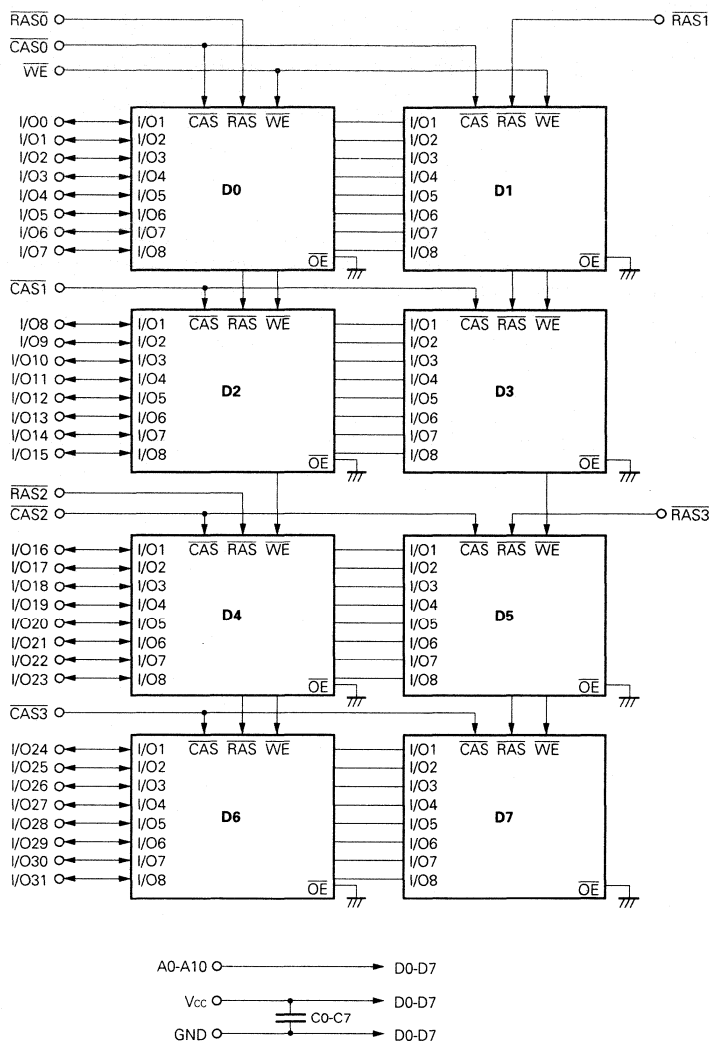


- A0 - A10 : Address Inputs
- I/O0 - I/O31 : Data Inputs/Outputs
- $\overline{\text{RAS0}}$ - $\overline{\text{RAS3}}$: Row Address Strobe
- $\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- PD1 - PD7 : Presence Detect Pins
- Vcc : Power Supply
- GND : Ground
- NC : No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	GND	GND	GND
PD2	66	NC	NC	NC
PD3	67	GND	GND	GND
PD4	68	GND	GND	GND
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram



Remark D0-D7 : μ PD42S17800LG5 (TSOP (III))

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

★ Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			55	pF
	C_{I2}	$\overline{WE}$			71	
	C_{I3}	RAS0 - RAS3			30	
	C_{I4}	CAS0 - CAS3			24	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			19	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	RAS, $\overline{\text{CAS}}$ Cycling	t _{RAC} = 60 ns		405	mA	3, 4, 7
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 70 ns		365		
		I _O = 0 mA	t _{RAC} = 80 ns		325		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.)	I _O = 0 mA		4.0	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	I _O = 0 mA		1.2		
RAS only refresh current	I _{CC3}	RAS Cycling	t _{RAC} = 60 ns		405	mA	3, 4, 5, 7
		$\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.)	t _{RAC} = 70 ns		365		
		t _{RC} = t _{RC} (MIN.) I _O = 0 mA	t _{RAC} = 80 ns		325		
Operating current (Fast page mode)	I _{CC4}	RAS $\leq V_{\text{IL}}$ (MAX.), $\overline{\text{CAS}}$ Cycling	t _{RAC} = 60 ns		285	mA	3, 4, 6
		t _{PC} = t _{PC} (MIN.)	t _{RAC} = 70 ns		245		
		I _O = 0 mA	t _{RAC} = 80 ns		205		
$\overline{\text{CAS}}$ before RAS refresh current	I _{CC5}	RAS Cycling	t _{RAC} = 60 ns		405	mA	3, 4
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 70 ns		365		
		I _O = 0 mA	t _{RAC} = 80 ns		325		
$\overline{\text{CAS}}$ before RAS long refresh current	I _{CC6}	$\overline{\text{CAS}}$ before RAS refresh: t _{RC} = 62.5 μ s $\overline{\text{RAS}}, \overline{\text{CAS}}$: V _{CC} - 0.2 V $\leq$ V _{IH} $\leq$ V _{IH} (MAX.) 0 V $\leq$ V _{IL} $\leq$ 0.2 V Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : V _{IH} or V _{IL} WE : V _{IH} I _O = 0 mA	t _{RAS} $\leq$ 1 μ s		1.6	mA	3, 4
$\overline{\text{CAS}}$ before RAS self refresh current	I _{CC7}	RAS, $\overline{\text{CAS}}$: t _{RAS} = 5 ms V _{CC} - 0.2 V $\leq$ V _{IH} $\leq$ V _{IH} (MAX.) 0 V $\leq$ V _{IL} $\leq$ 0.2 V I _O = 0 mA			1.2	mA	4
Input leakage current	I _{I (IL)}	V _I = 0 to 3.6 V All other pins not under test = 0 V		-5	+5	μ A	
Output leakage current	I _{O (IL)}	V _O = 0 to 3.6 V Output is disabled (Hi-Z)		-5	+5	μ A	
High level output voltage	V _{OH}	I _O = -2.0 mA		2.4		V	
Low level output voltage	V _{OL}	I _O = +2.0 mA			0.4	V	

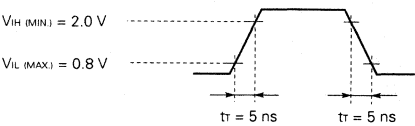
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from RAS	t _{RAC}		60		70		80	ns	10, 11
Access Time from CAS	t _{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45	ns	11
RAS to Column Address Delay Time	t _{RA}	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{RP}	40		50		60		ns	
RAS Pulse Width	t _{RA}	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RA} SP	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	t _{RS}	15		18		20		ns	
CAS Pulse Width	t _{CA}	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	t _{CS}	60		70		80		ns	
RAS to CAS Delay Time	t _{RC}	20	45	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to RAS Precharge Time	t _{CRP}	5		5		5		ns	13
CAS Precharge Time	t _{CP}	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
RAS Precharge CAS Hold Time	t _{RPC}	5		5		5		ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		ns	
Row Address Setup Time	t _{AS}	0		0		0		ns	
Row Address Hold Time	t _{AH}	10		10		12		ns	
Column Address Setup Time	t _{AS}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to RAS	t _{AL}	30		35		40		ns	
Read Command Setup Time	t _{RC}	0		0		0		ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	t _{CSR}	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10		10		10		ns	
RAS Pulse Width ($\overline{\text{CAS}}$ before RAS Self Refresh)	t _{RAS}	100		100		100		μ s	
RAS Precharge Time (CAS before RAS Self Refresh)	t _{RPS}	110		130		150		ns	
CAS Hold Time (CAS before RAS Self Refresh)	t _{CHS}	-50		-50		-50		ns	
$\overline{\text{WE}}$ Setup Time	t _{WS}	10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WH}	15		15		15		ns	
Refresh Time	t _{REF}		128		128		128	ms	

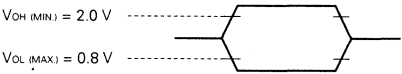
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
- 3. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC5} and I_{CC6} depend on cycle rates (trc and tpc).
- 4. Specified values are obtained with outputs unloaded.
- 5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
- 6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
- 7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq \text{V}_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq \text{V}_{\text{IH}}$ (MIN.).
- 8. AC measurements assume $\text{tr} = 5 \text{ ns}$.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



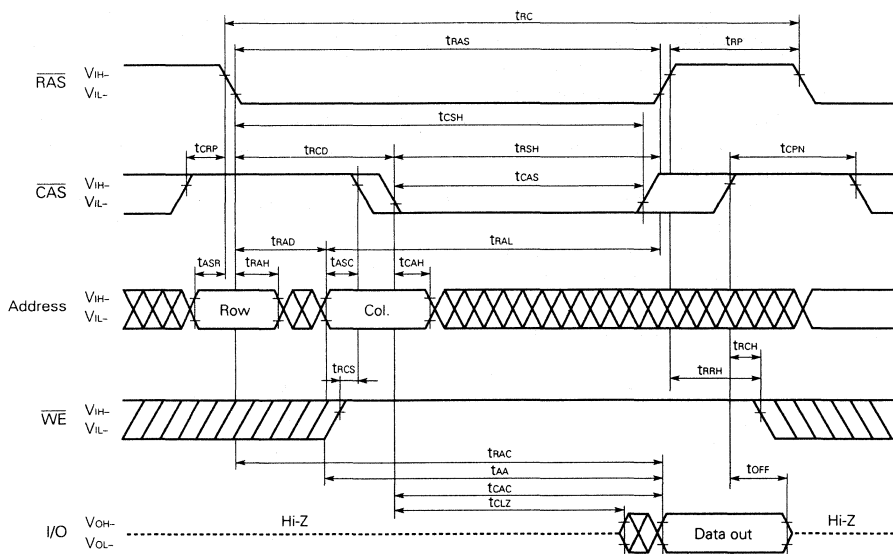
- 10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$\text{trAD} \leq \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\text{trAD} > \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$	$\text{trAD} + \text{tAA} (\text{MAX.})$
$\text{trCD} > \text{trCD} (\text{MAX.})$	$\text{tCAC} (\text{MAX.})$	$\text{trCD} + \text{tCAC} (\text{MAX.})$

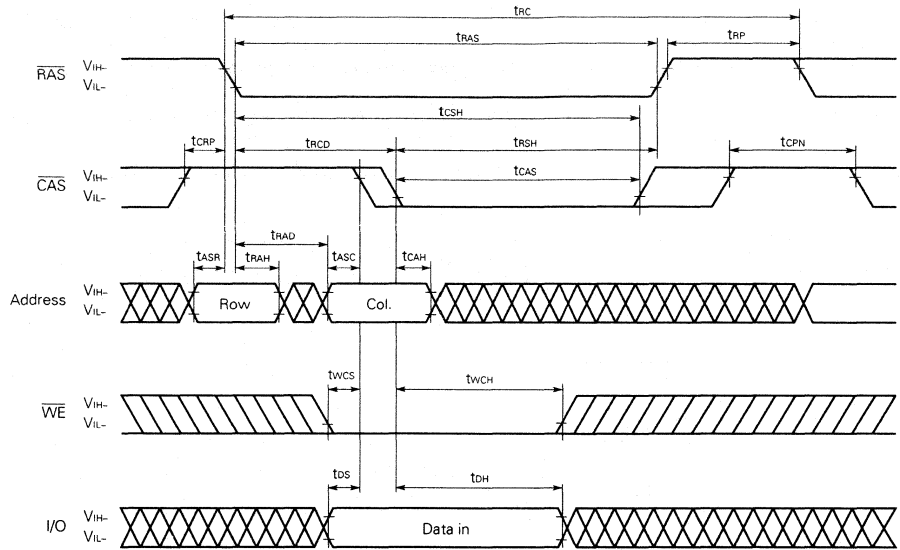
$\text{trAD} (\text{MAX.})$ and $\text{trCD} (\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD} (\text{MAX.})$ and $\text{trCD} \geq \text{trCD} (\text{MAX.})$ will not cause any operation problems.

- 11. Loading conditions are 1 TTL and 100 pF.
- 12. $\text{toff} (\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
- 13. $\text{tcrp} (\text{MIN.})$ requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
- 14. Either $\text{trCH} (\text{MIN.})$ or $\text{trRH} (\text{MIN.})$ should be met in read cycles.
- 15. In early write cycles, $\text{twCH} (\text{MIN.})$ should be met.
- 16. $\text{tDS} (\text{MIN.})$ and $\text{tDH} (\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
- 17. If $\text{twCS} \geq \text{twCS} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

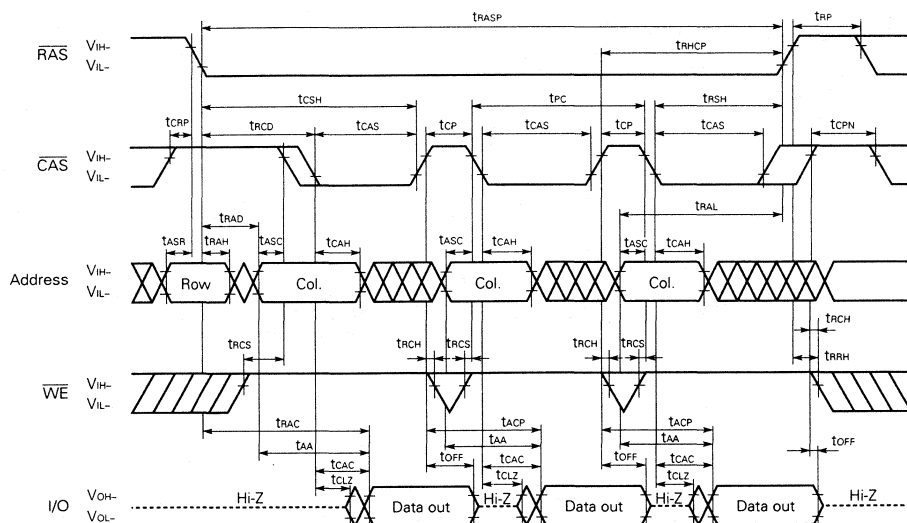
Read Cycle



Early Write Cycle

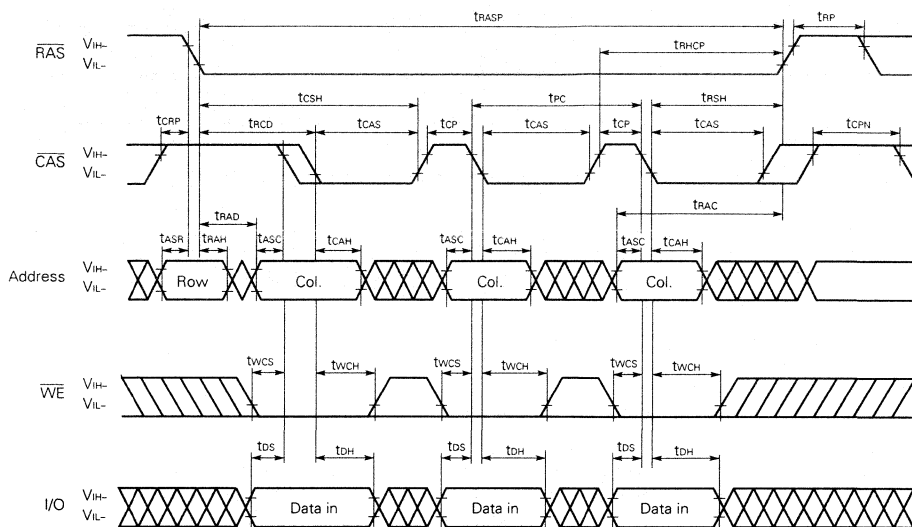


Fast Page Mode Read Cycle



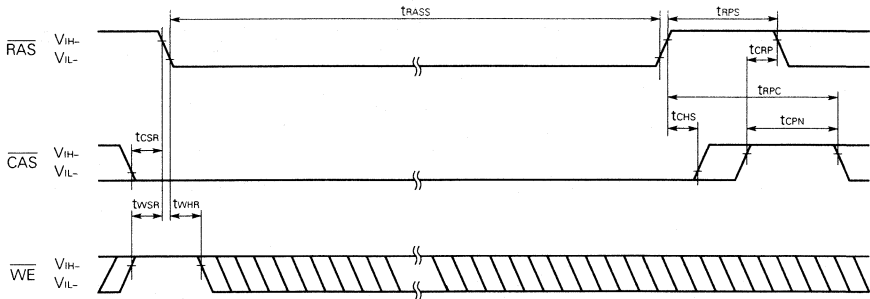
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle



Remark Address : Don't care I/O : Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

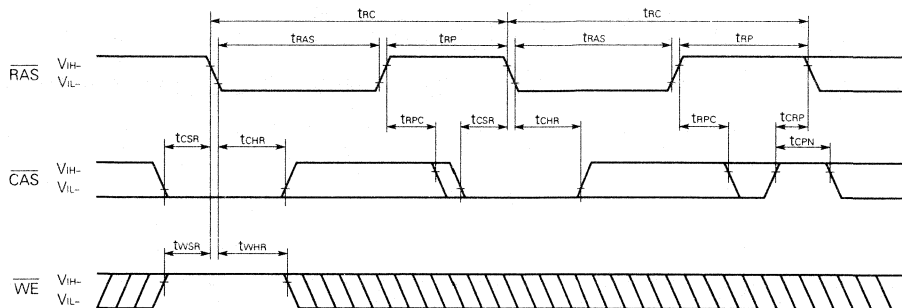
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

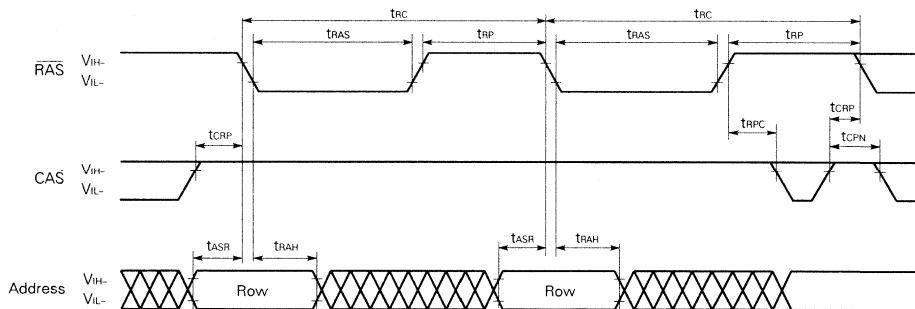
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



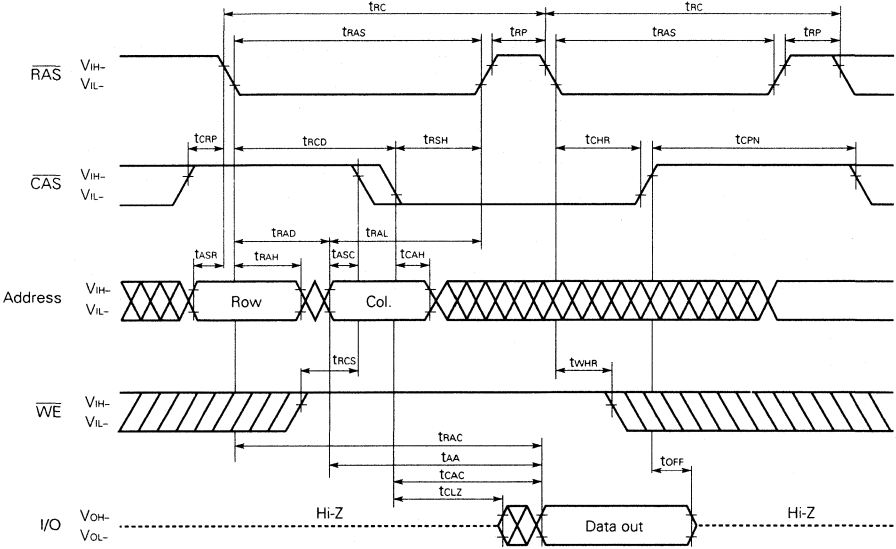
Remark Address : Don't care I/O: Hi-Z

RAS Only Refresh Cycle



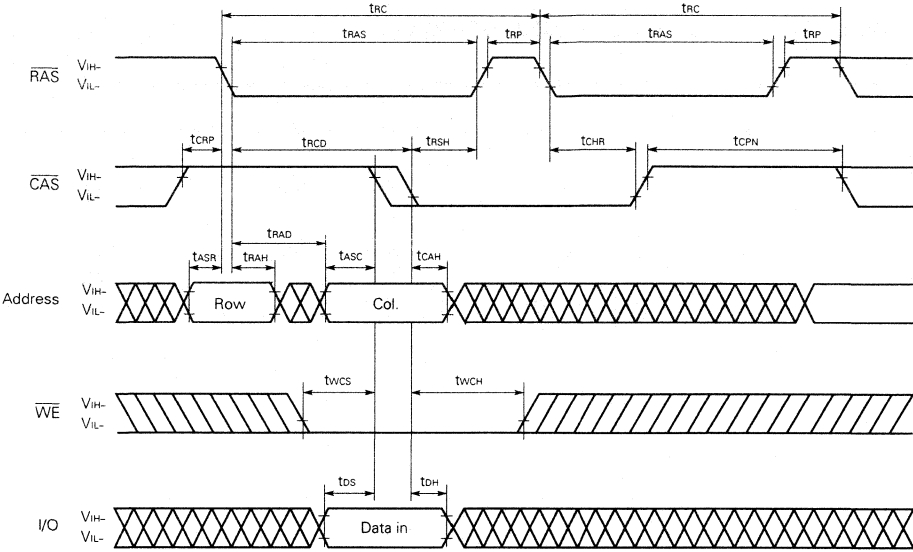
Remark $\overline{\text{WE}}$: Don't care I/O: Hi-Z

★ Hidden Refresh Cycle (Read)



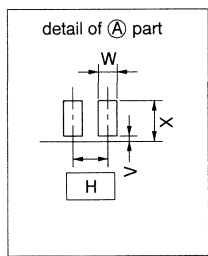
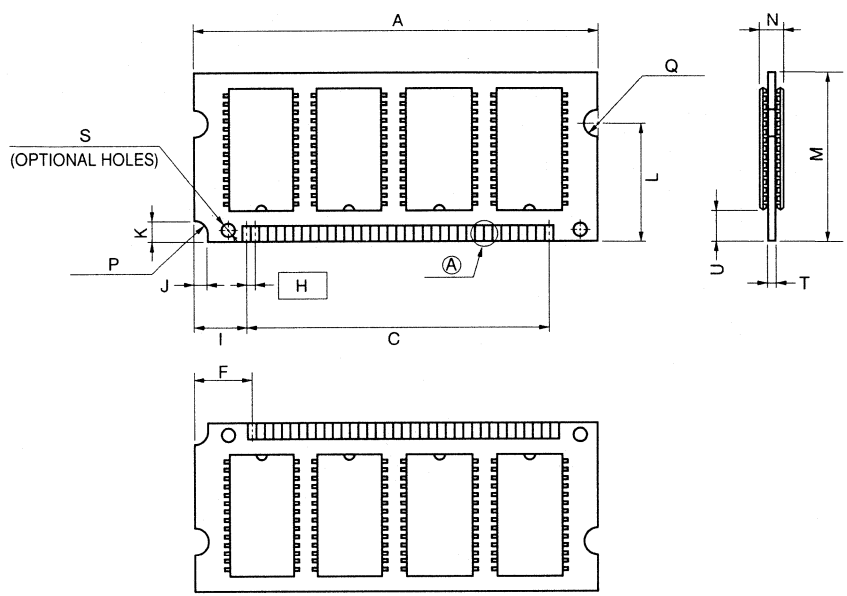
Hidden Refresh Cycle (Write)

★



★ Package Drawing

72PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.03	0.080
K	3.175	0.125
L	17.78	0.700
M	25.4	1.000
N	3.81 MAX.	0.150 MAX.
P	R1.57	R0.062
Q	R2.0	R0.079
S	φ1.8	φ0.071
T	1.016±0.1	0.04±0.004
U	3.175 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72S-50A2-1

MOS INTEGRATED CIRCUIT

MC-42S4000LAC32S SERIES

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S4000LAC32S series is a 4,194,304 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 16 M DRAM: μ PD42S17400LG3 (TSOP (II)) are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 4,194,304 words by 32 bits organization
- Fast access and cycle time

★

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S4000LAC32S-A60	60 ns	110 ns	2,880 mW	4.32 mW (CMOS level input)
MC-42S4000LAC32S-A70	70 ns	130 ns	2,592 mW	
MC-42S4000LAC32S-A80	80 ns	150 ns	2,304 mW	

- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V $\pm$ 0.3 V power supply

The information in this document is subject to change without notice.

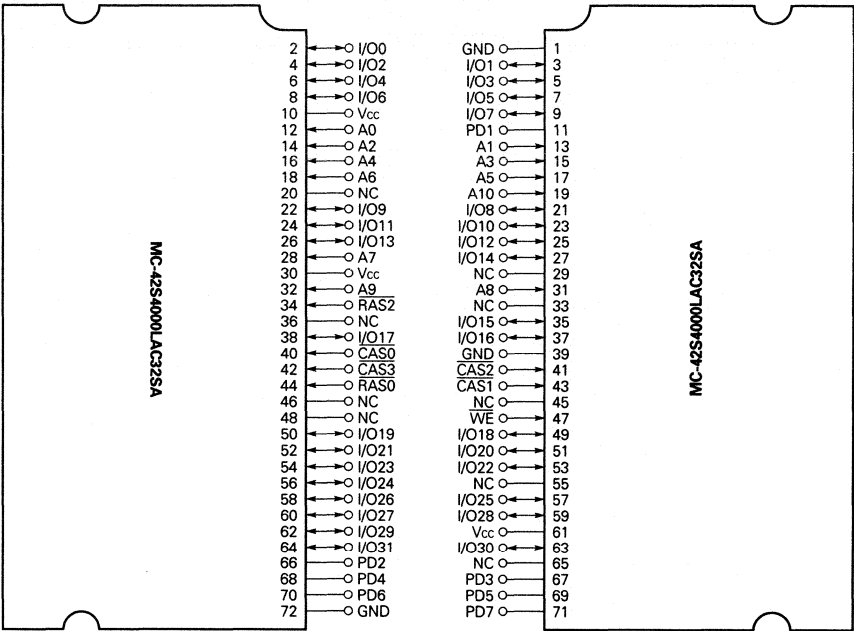
★ Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S4000LAC32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μ PD42S17400LG3 (300 mil TSOP (III)) [Double side]
MC-42S4000LAC32SA-A70	70 ns		
MC-42S4000LAC32SA-A80	80 ns		

Pin Configuration



72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



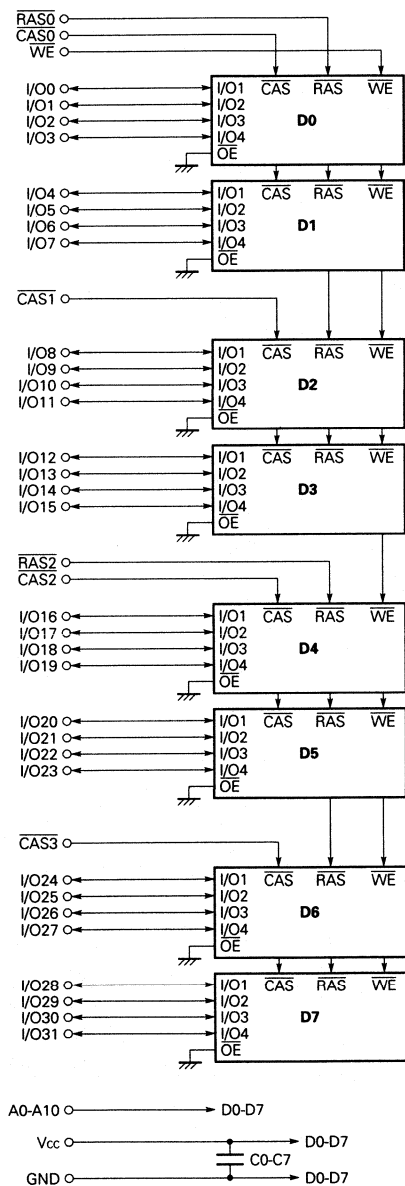
- A0 - A10 : Address Inputs
- I/O0 - I/O31 : Data Inputs/Outputs
- RAS0, RAS2 : Row Address Strobe
- CAS0 - CAS3 : Column Address Strobe
- WE : Write Enable
- PD1 - PD7 : Presence Detect Pins
- Vcc : Power Supply
- GND : Ground
- NC : No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	NC	NC	NC
PD2	66	NC	NC	NC
PD3	67	GND	GND	GND
PD4	68	NC	NC	NC
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram

Remark D0-07 : μ PD42S17400LG3 (TSOP (II))



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			55	pF
	C_{I2}	$\overline{WE}$			71	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			36	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			19	
Data Input/Output capacitance	C_{IO}	I/O0 - I/O31			10	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		800	mA	3, 4, 7
			$t_{\text{RAC}} = 70 \text{ ns}$		720		
			$t_{\text{RAC}} = 80 \text{ ns}$		640		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$I_o = 0 \text{ mA}$		4	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$I_o = 0 \text{ mA}$		1.2		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\text{CAS} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		800	mA	3, 4, 5, 7
			$t_{\text{RAC}} = 70 \text{ ns}$		720		
			$t_{\text{RAC}} = 80 \text{ ns}$		640		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		560	mA	3, 4, 6
			$t_{\text{RAC}} = 70 \text{ ns}$		480		
			$t_{\text{RAC}} = 80 \text{ ns}$		400		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		800	mA	3, 4
			$t_{\text{RAC}} = 70 \text{ ns}$		720		
			$t_{\text{RAC}} = 80 \text{ ns}$		640		
★ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current	I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: $t_{\text{RC}} = 62.5 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$: $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby: $\overline{\text{RAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : V_{IH} or V_{IL} $\overline{\text{WE}} : V_{\text{IH}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAS}} \leq 1 \mu\text{s}$		1.6	mA	3, 4
★ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh current	I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}$: $t_{\text{RAS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$			1.2	mA	4
Input leakage current	I _{I (IL)}	$V_i = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V		-5	+5	μA	
Output leakage current	I _{O (IL)}	$V_o = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)		-5	+5	μA	
High level output voltage	V _{OH}	$I_o = -2.0 \text{ mA}$		2.4		V	
Low level output voltage	V _{OL}	$I_o = +2.0 \text{ mA}$			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15		18		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RC_D}	20	40	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{APC}	5		5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	5		5		5		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10		10		10		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	t _{RASS}	100		100		100		μs	
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	t _{RPS}	110		130		150		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	t _{CHS}	-50		-50		-50		ns	
Refresh Time	t _{REF}		128		128		128	ms	

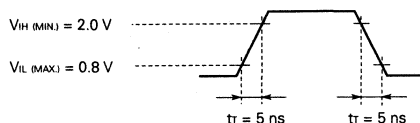
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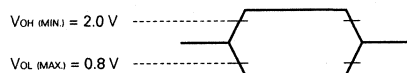
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.).
8. AC measurements assume $t_{\text{T}} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



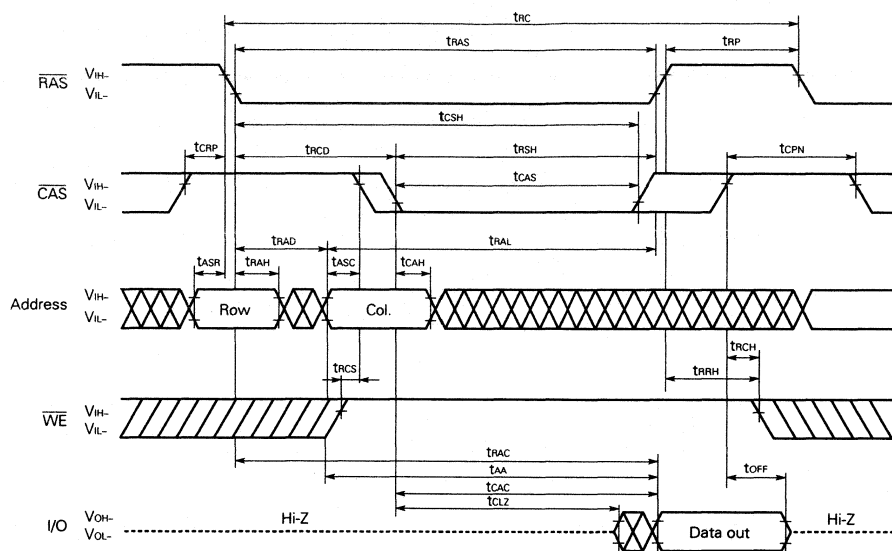
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX.})$	$t_{\text{RAC}} (\text{MAX.})$	$t_{\text{RAC}} (\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX.})$	$t_{\text{AA}} (\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}} (\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}} (\text{MAX.})$	$t_{\text{CAC}} (\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}} (\text{MAX.})$

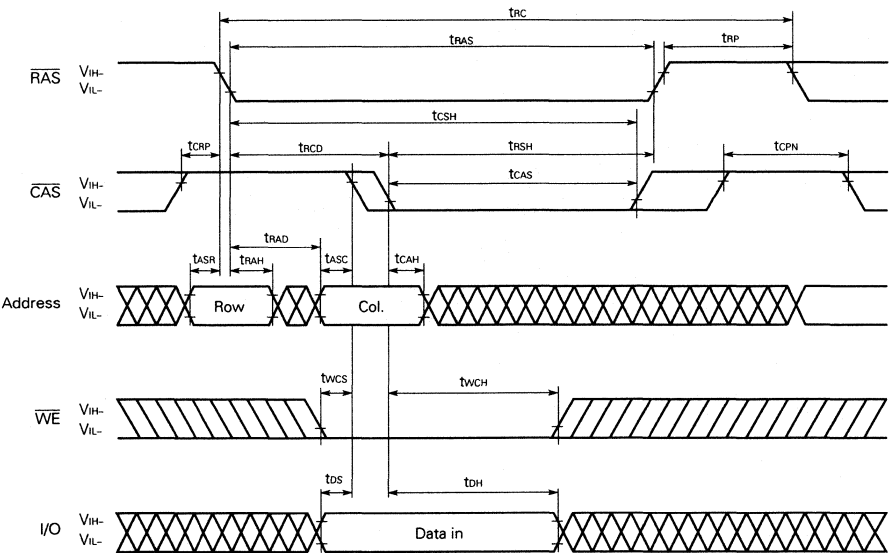
$t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} (\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{MAX.})$ will not cause any operation problems.

11. Loading conditions are 1 TTL and 100 pF.
12. $t_{\text{OFF}} (\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $t_{\text{CRP}} (\text{MIN.})$ requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either $t_{\text{RCH}} (\text{MIN.})$ or $t_{\text{RRH}} (\text{MIN.})$ should be met in read cycles.
15. In early write cycles, $t_{\text{WCH}} (\text{MIN.})$ should be met.
16. $t_{\text{DS}} (\text{MIN.})$ and $t_{\text{DH}} (\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Read Cycle



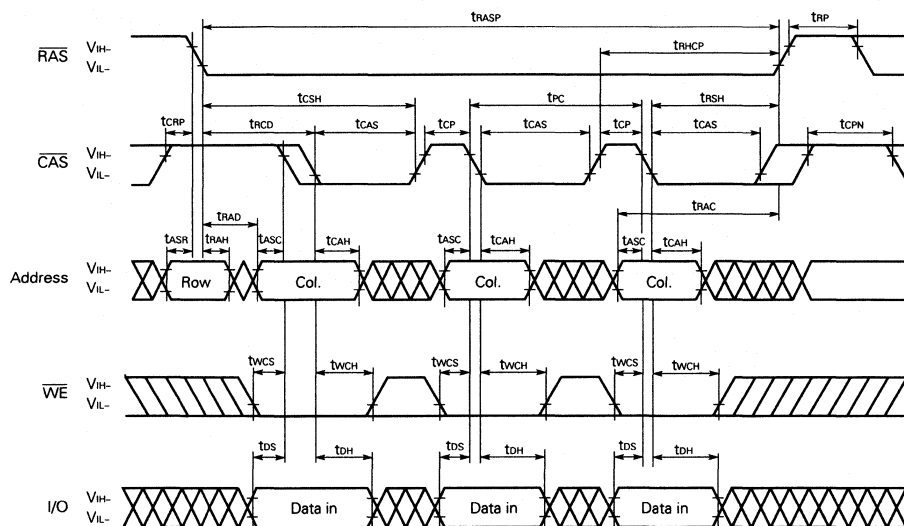
Early Write Cycle



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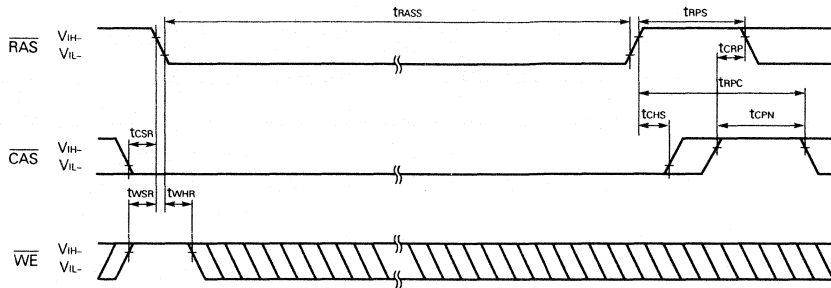
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Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh Cycle



Remark Address : Don't care I/O : Hi-Z

Cautions on Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh can be used independently when used in combination with distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh; However, when used in combination with burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh or with burst long $\overline{\text{RAS}}$ only refresh, the following cautions must be observed.

(1) Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Burst $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Long Refresh

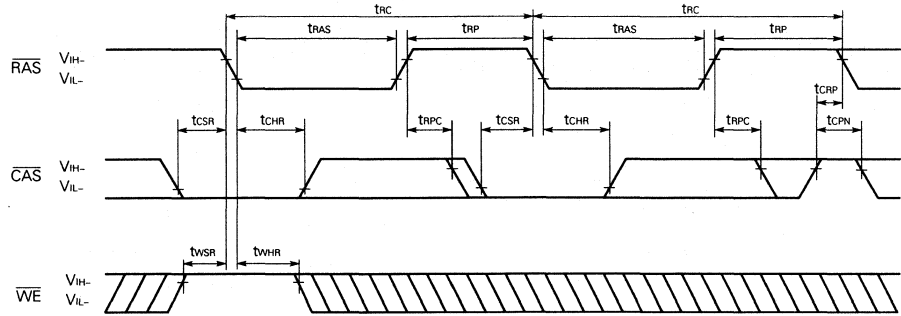
When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh are used in combination, please perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh 2,048 times within a 32 ms interval just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

(2) Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Burst Long $\overline{\text{RAS}}$ Only Refresh

When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{RAS}}$ only refresh are used in combination, please perform $\overline{\text{RAS}}$ only refresh 2,048 times within a 32 ms interval just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

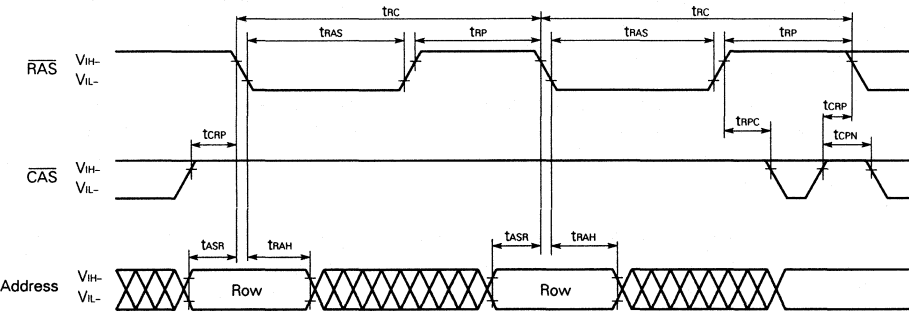
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



Remark Address: Don't care I/O: Hi-Z

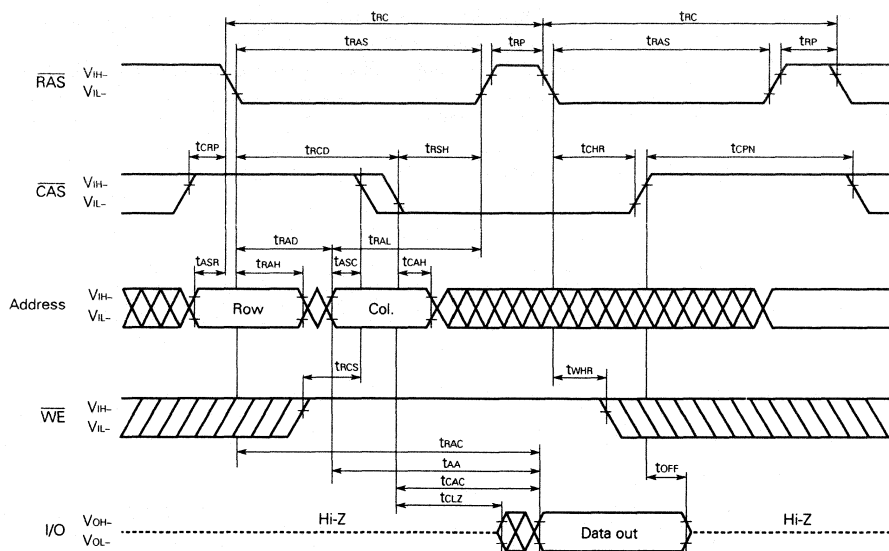
RAS Only Refresh Cycle



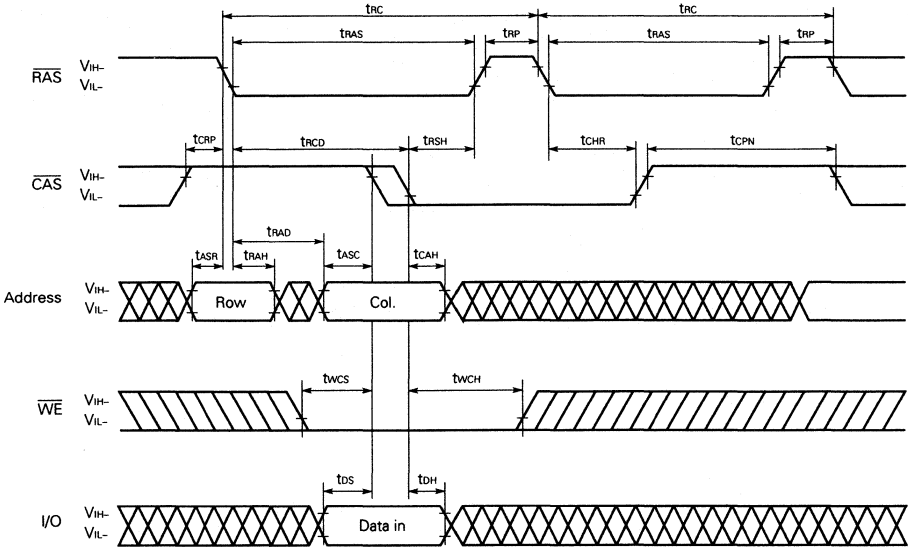
Remark $\overline{\text{WE}}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

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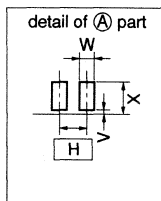
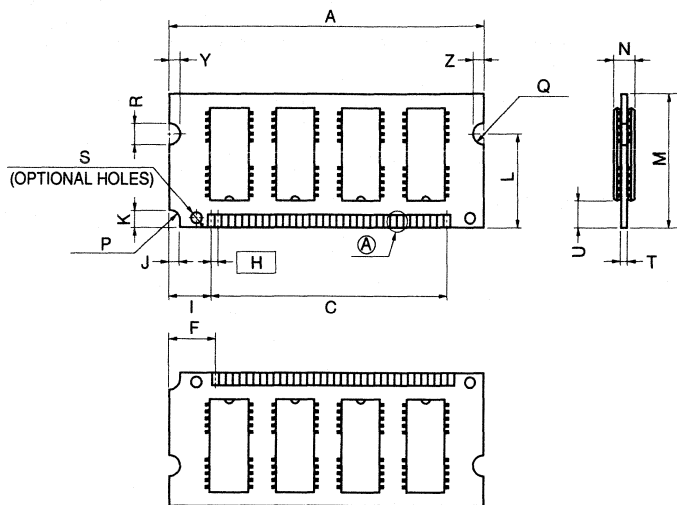


★ Hidden Refresh Cycle (Write)



Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.0	0.079
K	3.18	0.125
L	17.78	0.700
M	25.4	1.000
N	3.8 MAX.	0.150 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ1.8	φ0.071
T	1.0±0.1	0.039 ^{+0.005} _{-0.004}
U	3.18 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039 ^{+0.003} _{-0.002}
X	2.54 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.

M72S-50A5

MOS INTEGRATED CIRCUIT

MC-42S2000LAB32S SERIES

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM)

FAST PAGE MODE

Description

The MC-42S2000LAB32S series is a 2,097,152 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 4 pieces of 16 M DRAM: μ PD42S17800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S2000LAB32S-A60	60 ns	110 ns	1,440 mW	2.16 mW (CMOS level input)
MC-42S2000LAB32S-A70	70 ns	130 ns	1,296 mW	
MC-42S2000LAB32S-A80	80 ns	150 ns	1,152 mW	

- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V $\pm$ 0.3 V power supply

Ordering Information

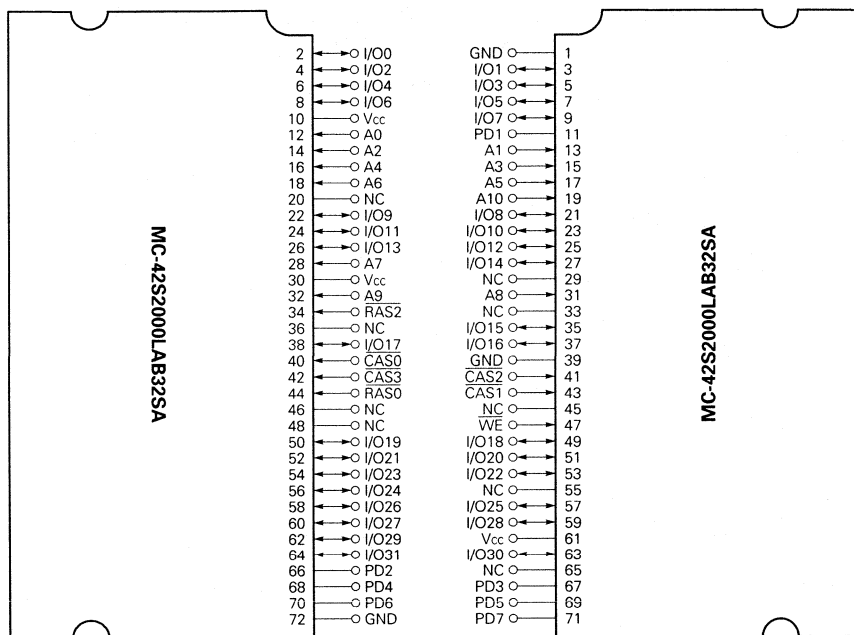
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Part number	Access time (MAX.)	Package	Mounted devices
MC-42S2000LAB32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μ PD42S17800LG5 (400 mil TSOP (III)) [Single side]
MC-42S2000LAB32SA-A70	70 ns		
MC-42S2000LAB32SA-A80	80 ns		

The information in this document is subject to change without notice.

Pin Configuration

★ 72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



A0 - A10 : Address Inputs
 I/O0 - I/O31 : Data Inputs/Outputs
 RAS0, RAS2 : Row Address Strobe
 CAS0 - CAS3 : Column Address Strobe
 WE : Write Enable
 PD1 - PD7 : Presence Detect Pins
 V_{cc} : Power Supply
 GND : Ground
 NC : No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	GND	GND	GND
PD2	66	NC	NC	NC
PD3	67	GND	GND	GND
PD4	68	NC	NC	NC
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

The diagram illustrates the internal structure of a 4-chip memory array. It consists of four memory chips, labeled D0, D1, D2, and D3, each with 8 data inputs (I/O0-I/O7) and 8 data outputs (I/O0-I/O7). The chips are connected to a common data bus (A0-A10) and a common address bus (Vcc and GND). The control signals (CAS, RAS, WE) are connected to the chips. The OE signal is connected to the chips and grounded.

Remark D0-D3 : μ PD42S17800LG5 (TSOP (II))

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		4	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

★

Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			35	pF
	C_{I2}	$\overline{WE}$			43	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			30	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			17	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			12	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	<u>RAS</u> , <u>CAS</u> Cycling	t _{RAC} = 60 ns	400	mA	3, 4, 7
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 70 ns	360		
		I _O = 0 mA	t _{RAC} = 80 ns	320		
Standby current	I _{CC2}	<u>RAS</u> , <u>CAS</u> ≥ V _{IH} (MIN.)	I _O = 0 mA	2.0	mA	
		<u>RAS</u> , <u>CAS</u> ≥ V _{CC} – 0.2 V	I _O = 0 mA	0.6		
<u>RAS</u> only refresh current	I _{CC3}	<u>RAS</u> Cycling	t _{RAC} = 60 ns	400	mA	3, 4, 5, 7
		<u>CAS</u> ≥ V _{IH} (MIN.)	t _{RAC} = 70 ns	360		
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 80 ns	320		
Operating current (Fast page mode)	I _{CC4}	<u>RAS</u> ≤ V _{IL} (MAX.), <u>CAS</u> Cycling	t _{RAC} = 60 ns	280	mA	3, 4, 6
		t _{PC} = t _{PC} (MIN.)	t _{RAC} = 70 ns	240		
		I _O = 0 mA	t _{RAC} = 80 ns	200		
<u>CAS</u> before <u>RAS</u> refresh current	I _{CC5}	<u>RAS</u> Cycling	t _{RAC} = 60 ns	400	mA	3, 4
		t _{RC} = t _{RC} (MIN.)	t _{RAC} = 70 ns	360		
		I _O = 0 mA	t _{RAC} = 80 ns	320		
<u>CAS</u> before <u>RAS</u> long refresh current	I _{CC6}	<u>CAS</u> before <u>RAS</u> refresh: t _{RC} = 62.5 μs <u>RAS</u> , <u>CAS</u> : V _{CC} – 0.2 V ≤ V _{IH} ≤ V _{IH} (MAX.) 0 V ≤ V _{IL} ≤ 0.2 V Standby: <u>RAS</u> , <u>CAS</u> ≥ V _{CC} – 0.2 V Address : V _{IH} or V _{IL} <u>WE</u> : V _{IH} I _O = 0 mA	t _{RAS} ≤ 1 μs	800	μA	3, 4
<u>CAS</u> before <u>RAS</u> self refresh current	I _{CC7}	<u>RAS</u> , <u>CAS</u> : t _{RAS} = 5 ms V _{CC} – 0.2 V ≤ V _{IH} ≤ V _{IH} (MAX.) 0 V ≤ V _{IL} ≤ 0.2 V I _O = 0 mA		600	μA	4
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V All other pins not under test = 0 V	–5	+5	μA	
Output leakage current	I _{O(L)}	V _O = 0 to 3.6 V Output is disabled (Hi-Z)	–5	+5	μA	
High level output voltage	V _{OH}	I _O = –2.0 mA	2.4		V	
Low level output voltage	V _{OL}	I _O = +2.0 mA		0.4	V	

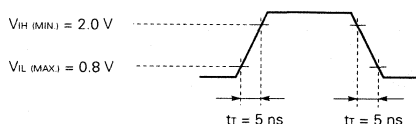
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t _{TRAC} = 60 ns		t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from RAS	t _{RAC}		60		70		80	ns	10, 11
Access Time from CAS	t _{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from CAS Precharge	t _{ACP}		35		40		45	ns	11
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	t _{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{RP}	40		50		60		ns	
RAS Pulse Width	t _{RA}	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	t _{RSH}	15		18		20		ns	
CAS Pulse Width	t _{CA}	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	t _{CSH}	60		70		80		ns	
RAS to CAS Delay Time	t _{RCO}	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	t _{CRP}	5		5		5		ns	13
CAS Precharge Time	t _{CPN}	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
RAS Precharge CAS Hold Time	t _{RPC}	5		5		5		ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	35		40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to RAS	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	t _{RCH}	0		0		0		ns	14
WE Hold Time Referenced to CAS	t _{WCH}	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	t _{CSR}	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10		10		10		ns	
RAS Pulse Width (CAS before RAS Self Refresh)	t _{RASS}	100		100		100		μs	
RAS Precharge Time (CAS before RAS Self Refresh)	t _{RPS}	110		130		150		ns	
CAS Hold Time (CAS before RAS Self Refresh)	t _{CHS}	-50		-50		-50		ns	
WE Setup Time	t _{WSR}	10		10		10		ns	
WE Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		128		128		128	ms	

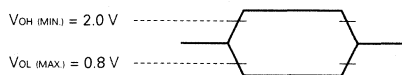
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. Icc1 , Icc3 , Icc4 , Icc5 and Icc6 depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. Icc3 is measured assuming that all column address inputs are held at either high or low.
6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}} (\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.})$.
8. AC measurements assume $t_{\text{r}} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



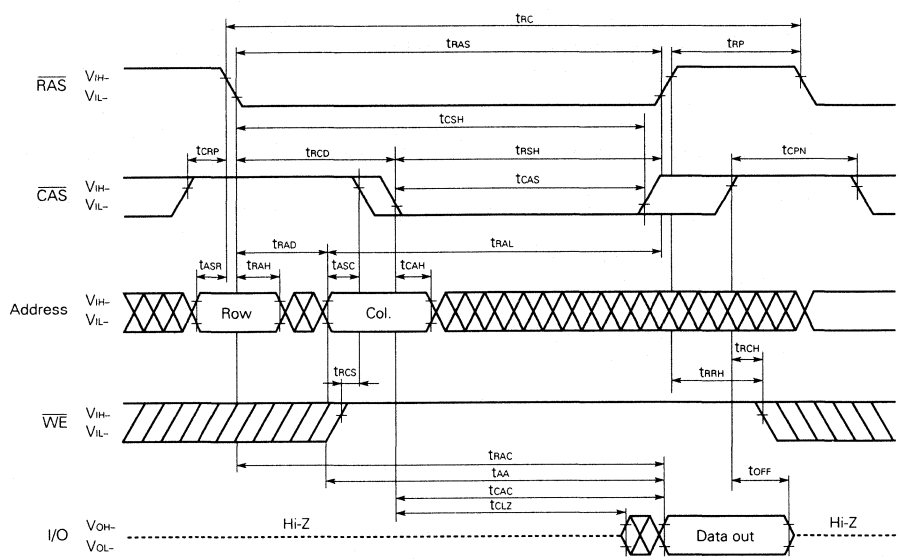
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX.})$	$t_{\text{RAC}} (\text{MAX.})$	$t_{\text{RAC}} (\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX.})$	$t_{\text{AA}} (\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}} (\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}} (\text{MAX.})$	$t_{\text{CAC}} (\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}} (\text{MAX.})$

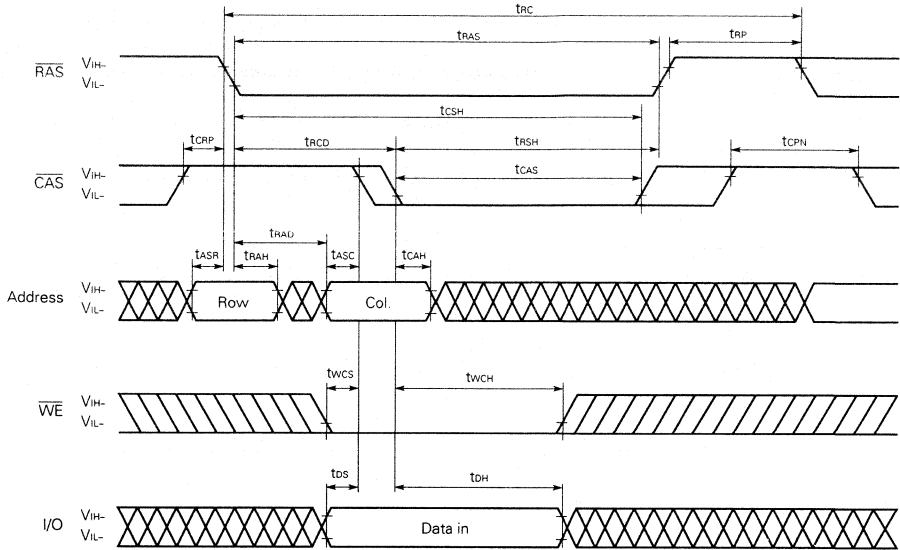
$t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} (\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{MAX.})$ will not cause any operation problems.

11. Loading conditions are 1 TTL and 100 pF.
12. $t_{\text{OFF}} (\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $t_{\text{CRP}} (\text{MIN.})$ requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either $t_{\text{RCH}} (\text{MIN.})$ or $t_{\text{RRH}} (\text{MIN.})$ should be met in read cycles.
15. In early write cycles, $t_{\text{WCH}} (\text{MIN.})$ should be met.
16. $t_{\text{DS}} (\text{MIN.})$ and $t_{\text{DH}} (\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

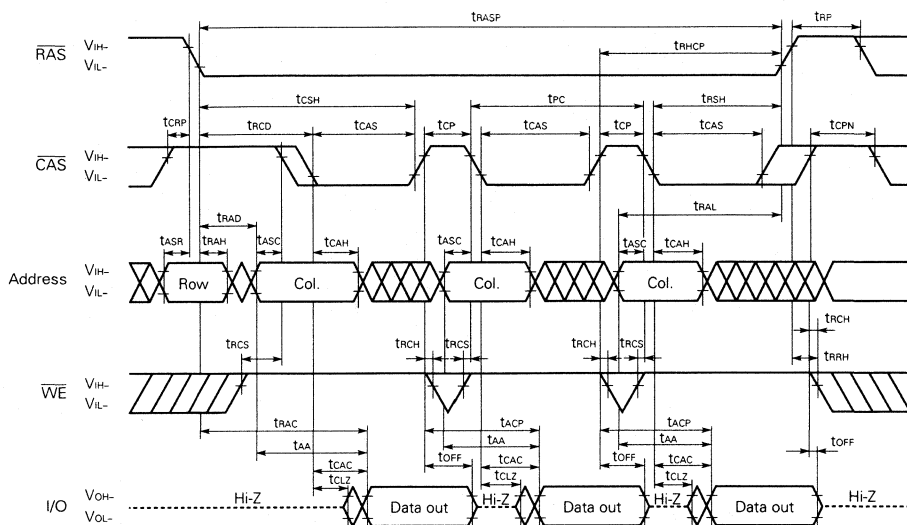
Read Cycle



Early Write Cycle

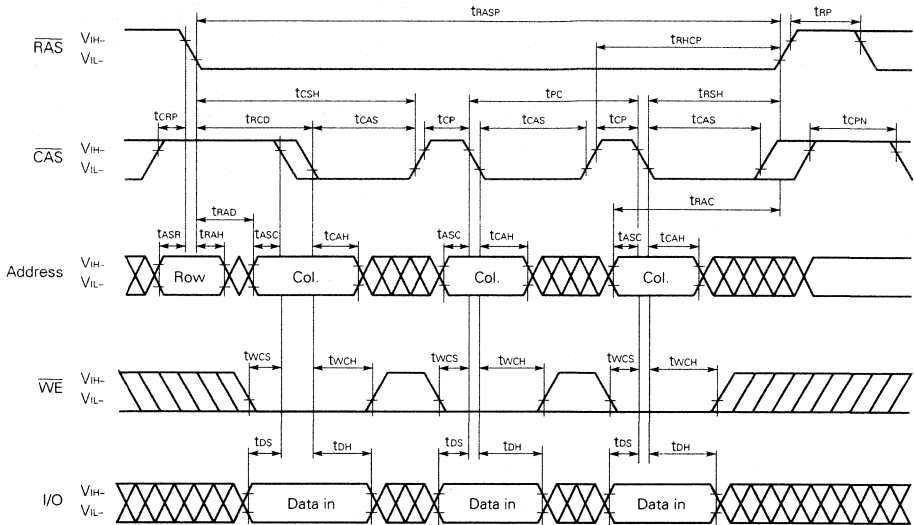


Fast Page Mode Read Cycle



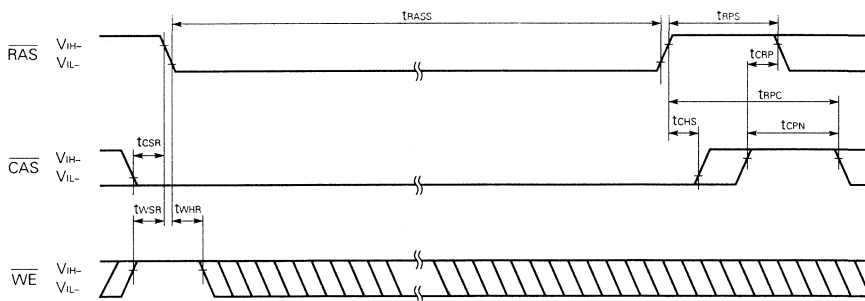
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

CAS Before RAS Self Refresh Cycle



Remark Address : Don't care I/O : Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

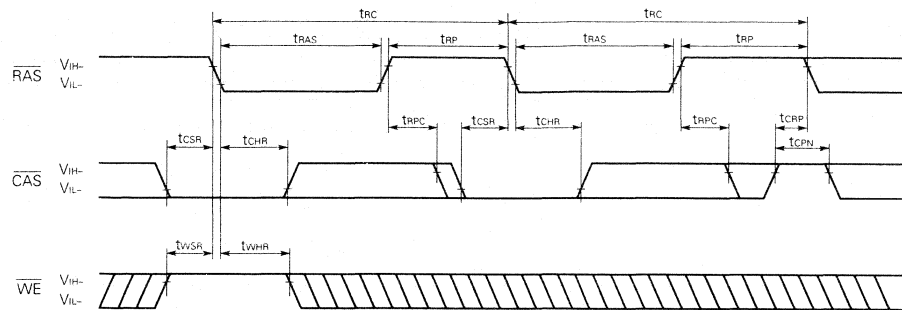
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

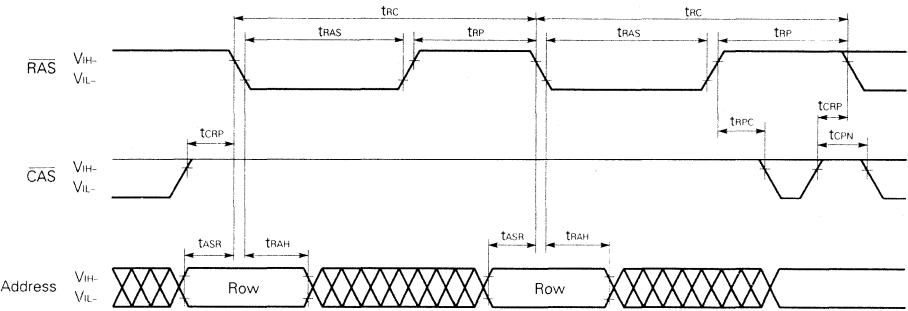
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



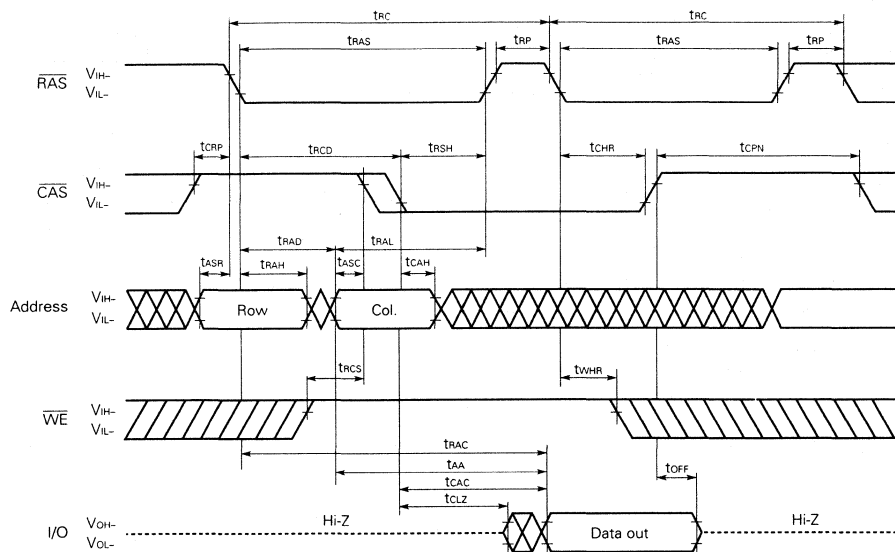
Remark Address : Don't care I/O: Hi-Z

RAS Only Refresh Cycle



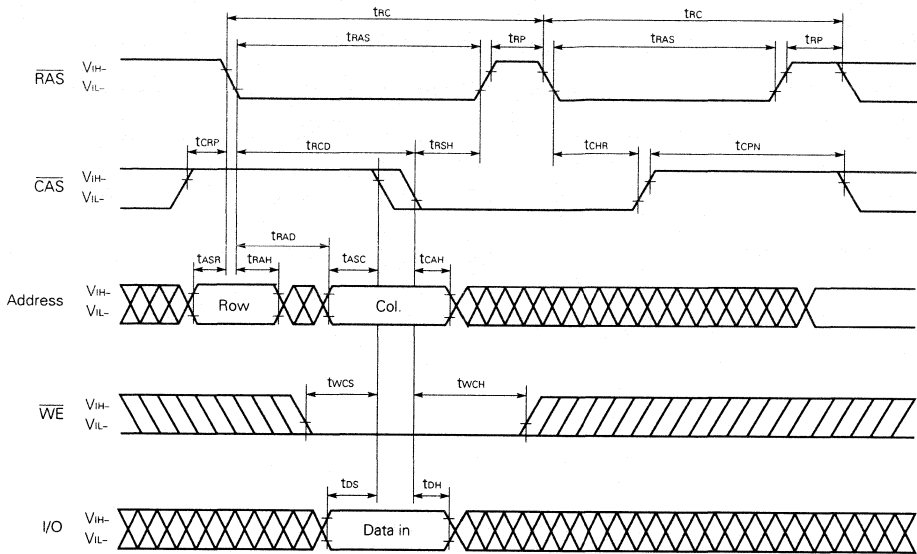
Remark WE: Don't care I/O: Hi-Z

★ Hidden Refresh Cycle (Read)



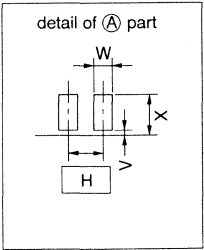
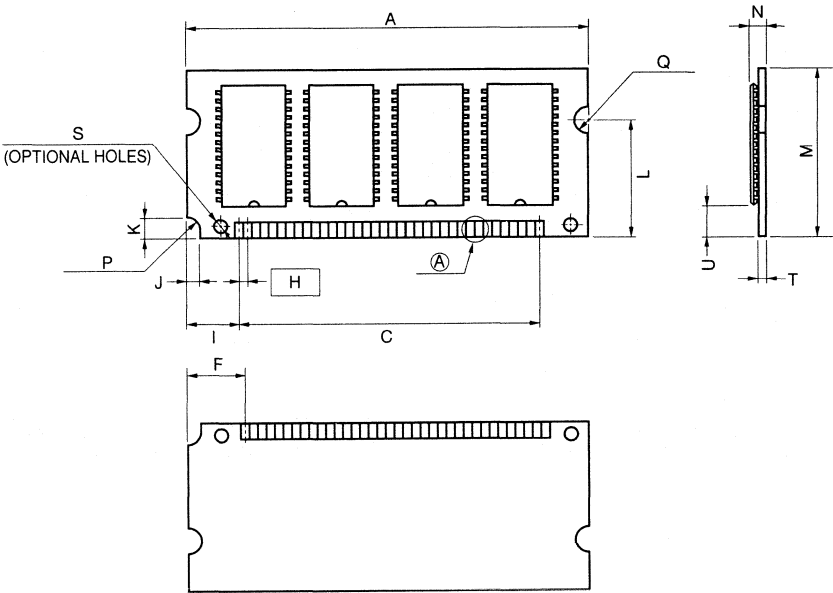
Hidden Refresh Cycle (Write)

★



★ Package Drawing

72PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.03	0.080
K	3.175	0.125
L	17.78	0.700
M	25.4	1.000
N	2.463 MAX.	0.097 MAX.
P	R1.57	R0.062
Q	R2.0	R0.079
S	φ1.8	φ0.071
T	1.016±0.1	0.04±0.004
U	3.175 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72S-50A1-1

MOS INTEGRATED CIRCUIT

MC-42S2000LAD32S SERIES

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S2000LAD32S series is a 2,097,152 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 4 pieces of 16 M DRAM: μ PD42S18160L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S2000LAD32S-A60	60 ns	110 ns	1,083.6 mW	2.16 mW (CMOS level input)
MC-42S2000LAD32S-A70	70 ns	130 ns	1,011.6 mW	
MC-42S2000LAD32S-A80	80 ns	150 ns	939.6 mW	

- 1,024 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V $\pm$ 0.3 V power supply

The information in this document is subject to change without notice.

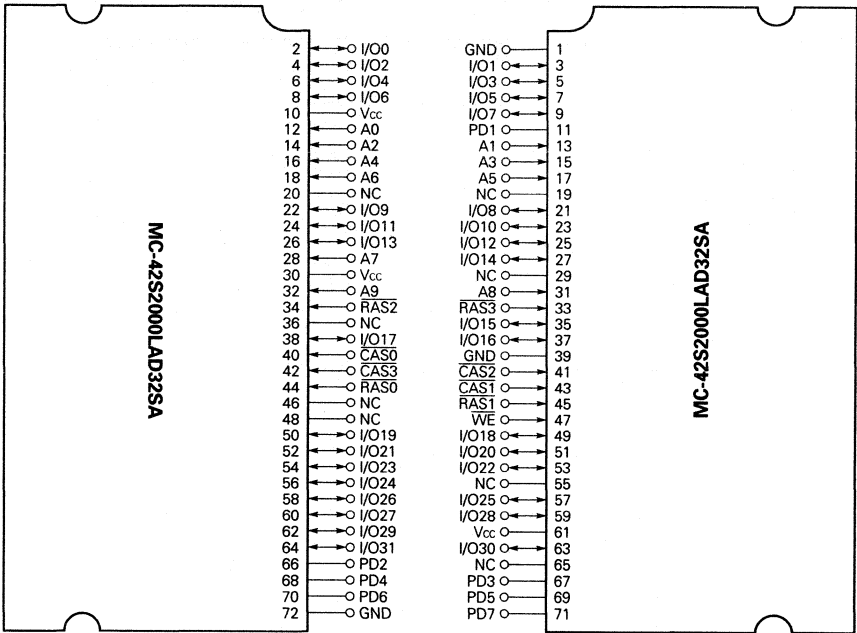
★ Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S2000LAD32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μ PD42S18160LG5 (400 mil TSOP (II)) [Double side]
MC-42S2000LAD32SA-A70	70 ns		
MC-42S2000LAD32SA-A80	80 ns		

Pin Configuration



72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)

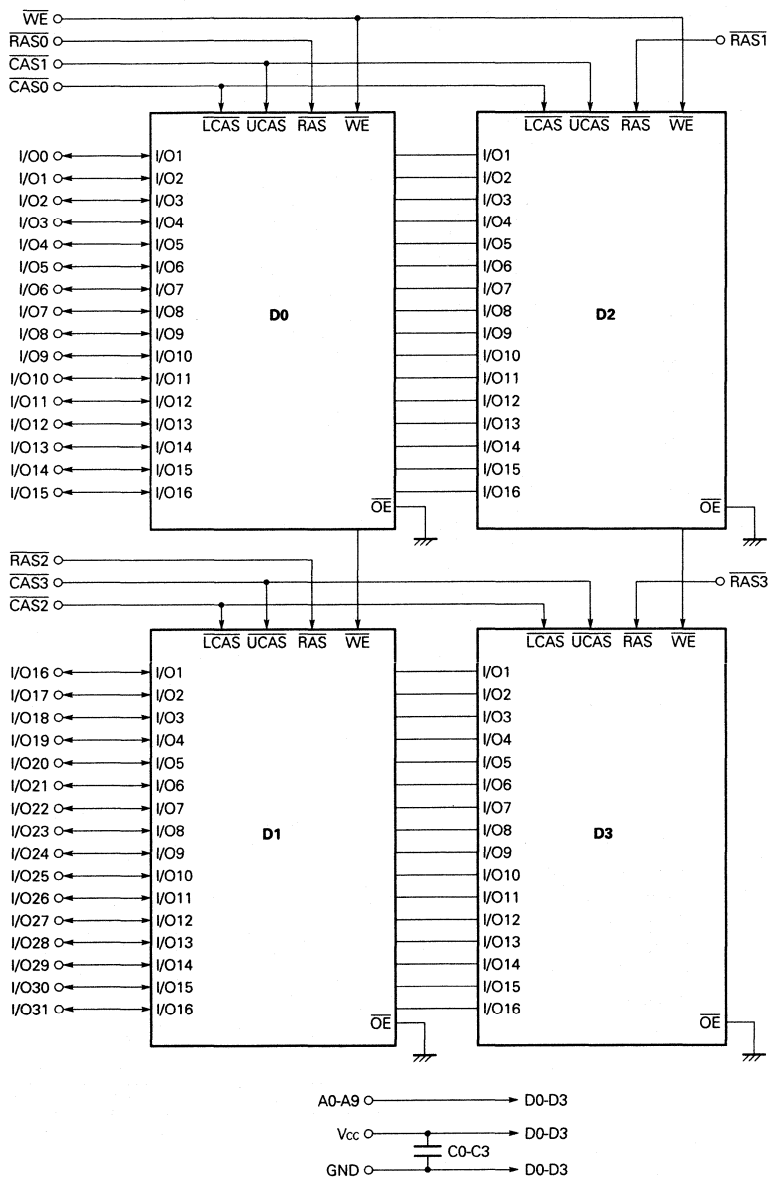


- A0 - A9 : Address Inputs
I/O0 - I/O31 : Data Inputs/Outputs
RAS0 - RAS3 : Row Address Strobe
CAS0 - CAS3 : Column Address Strobe
WE : Write Enable
PD1 - PD7 : Presence Detect Pins
Vcc : Power Supply
GND : Ground
NC : No connection

The internal connection of PD pins (PD1 - PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	NC	NC	NC
PD2	66	GND	GND	GND
PD3	67	GND	GND	GND
PD4	68	GND	GND	GND
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram



Remark D0-D3 : μ PD42S18160LG5 (TSOP (III))

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			35	pF
	C_{I2}	$\overline{WE}$			43	
	C_{I3}	RAS0 - RAS3			23	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			24	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			19	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

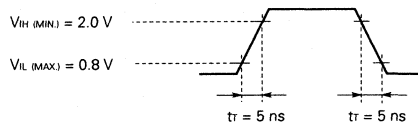
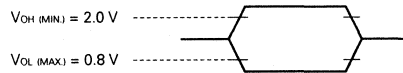
Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		301	mA	3, 4, 7
			$\text{trac} = 70 \text{ ns}$		281		
			$\text{trac} = 80 \text{ ns}$		261		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$	$I_o = 0 \text{ mA}$		2.0	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$	$I_o = 0 \text{ mA}$		0.6		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\text{CAS} \geq V_{IH}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		301	mA	3, 4, 5, 7
			$\text{trac} = 70 \text{ ns}$		281		
			$\text{trac} = 80 \text{ ns}$		261		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{IL}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $\text{tpc} = \text{tpc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		181	mA	3, 4, 6
			$\text{trac} = 70 \text{ ns}$		161		
			$\text{trac} = 80 \text{ ns}$		141		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$ $\text{trac} = 70 \text{ ns}$ $\text{trac} = 80 \text{ ns}$		301 281 261	mA	3, 4
★ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current	I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: $\text{trc} = 125.0 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$: $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH}(\text{MAX.})$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Address : V_{IH} or V_{IL} WE : V_{IH} $I_o = 0 \text{ mA}$	$\text{tras} \leq 1 \mu\text{s}$		720	μA	3, 4
★ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh current	I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}$: $\text{trass} = 5 \text{ ms}$ $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH}(\text{MAX.})$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$			600	μA	4
Input leakage current	I _{I(L)}	$V_i = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V		-5	+5	μA	
Output leakage current	I _{O(L)}	$V_o = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)		-5	+5	μA	
High level output voltage	V _{OH}	$I_o = -2.0 \text{ mA}$		2.4		V	
Low level output voltage	V _{OL}	$I_o = +2.0 \text{ mA}$			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RA}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RAH}	15		18		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CA}	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CAH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RC}	20	45	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{APC}	5		5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RAHCP}	35		40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	5		5		5		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10		10		10		ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	t _{RASS}	100		100		100		μ s	
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	t _{RPS}	110		130		150		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	t _{CHS}	-50		-50		-50		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		128		128		128	ms	

Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. Icc1 , Icc3 , Icc4 , Icc5 and Icc6 depend on cycle rates (trc and tpc).
4. Specified values are obtained with outputs unloaded.
5. Icc3 is measured assuming that all column address inputs are held at either high or low.
6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.).
8. AC measurements assume $t_{\text{T}} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification**(2) Output timing specification**

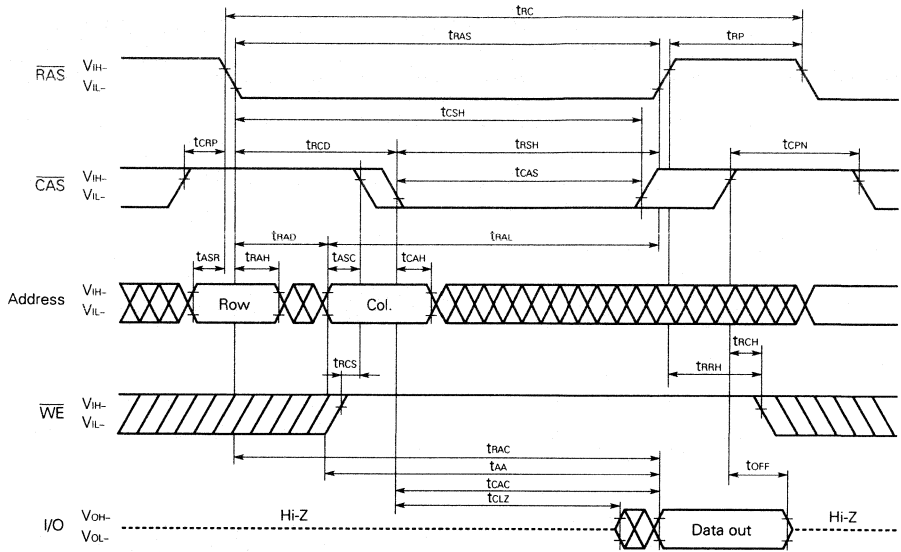
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\text{trAD} > \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$	$\text{trAD} + \text{tAA} (\text{MAX.})$
$\text{trCD} > \text{trCD} (\text{MAX.})$	$\text{tCAC} (\text{MAX.})$	$\text{trCD} + \text{tCAC} (\text{MAX.})$

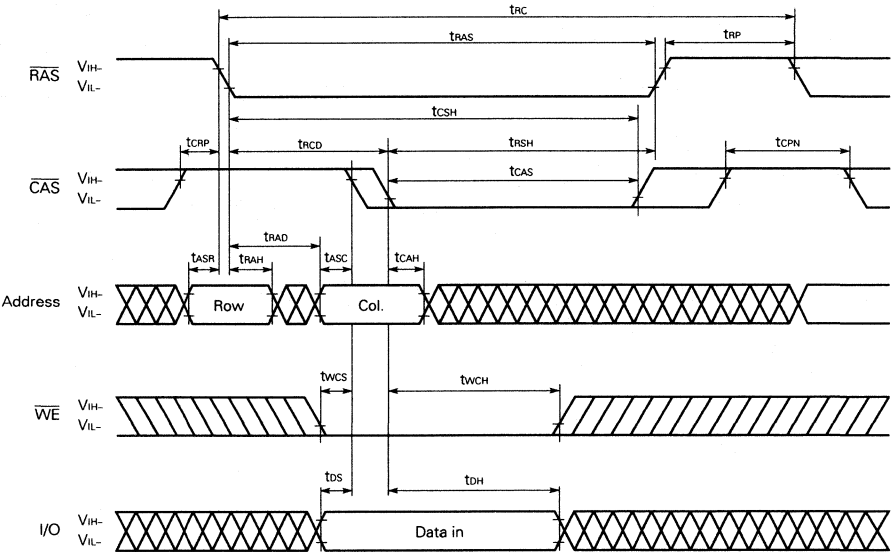
$\text{trAD} (\text{MAX.})$ and $\text{trCD} (\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD} (\text{MAX.})$ and $\text{trCD} \geq \text{trCD} (\text{MAX.})$ will not cause any operation problems.

11. Loading conditions are 1 TTL and 100 pF.
12. $\text{tOFF} (\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $\text{tCRP} (\text{MIN.})$ requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either $\text{trCH} (\text{MIN.})$ or $\text{trRH} (\text{MIN.})$ should be met in read cycles.
15. In early write cycles, $\text{twCH} (\text{MIN.})$ should be met.
16. $\text{tDS} (\text{MIN.})$ and $\text{tDH} (\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $\text{twCS} \geq \text{twCS} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Read Cycle



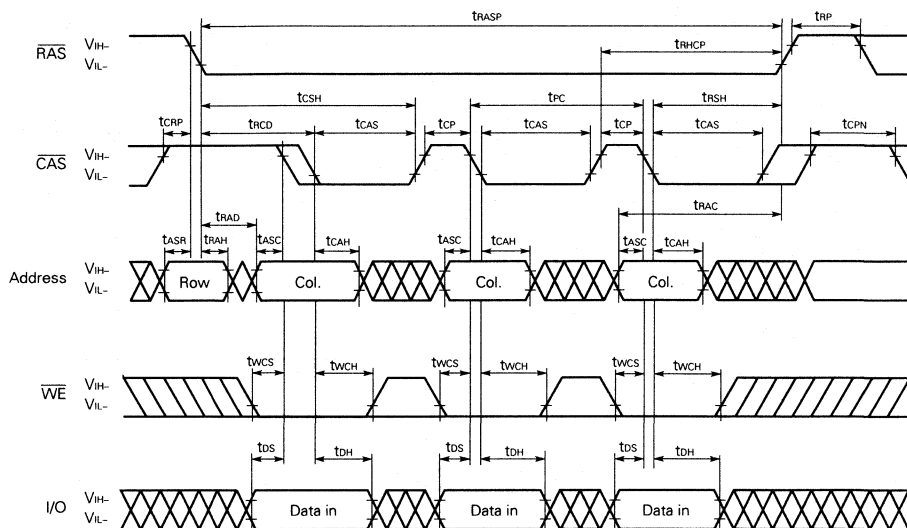
Early Write Cycle



[illegible]

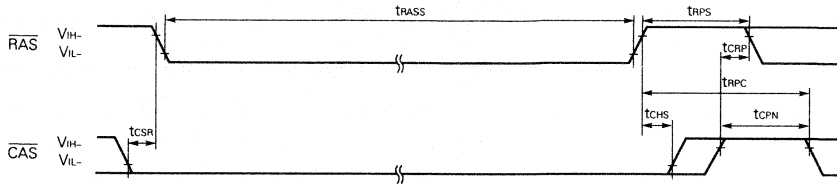
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Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle



Remark Address, $\overline{WE}$: Don't care I/O : Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

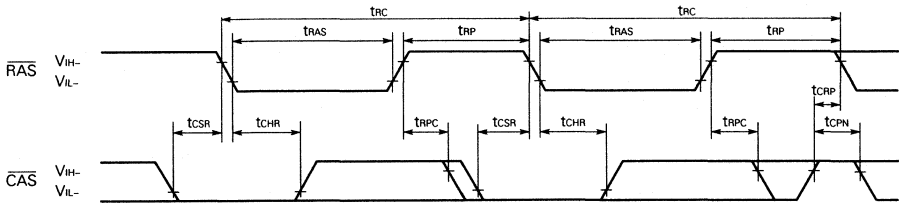
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 1,024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh 1,024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

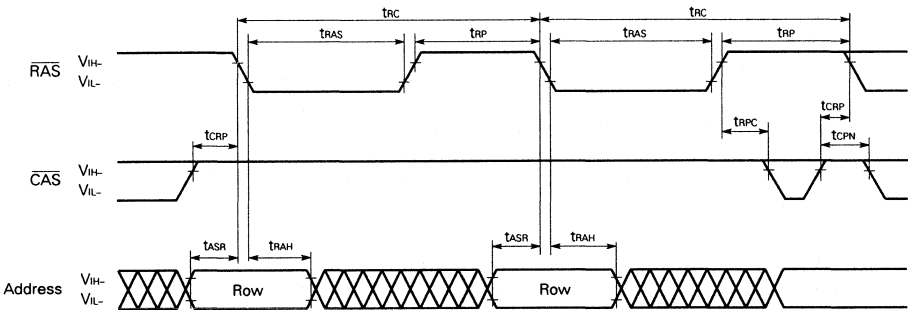
For details, please refer to **How to use DRAM User's Manual**.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



Remark Address, $\overline{\text{WE}}$: Don't care I/O: Hi-Z

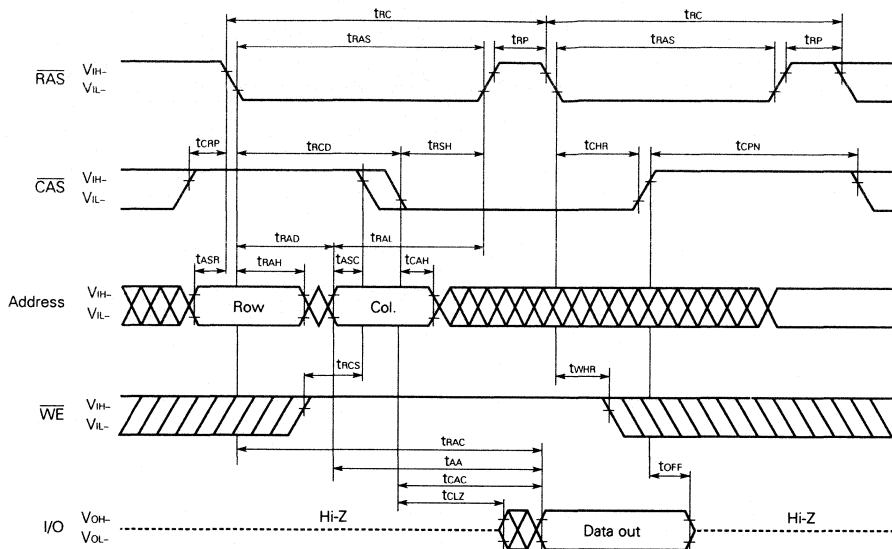
$\overline{\text{RAS}}$ Only Refresh Cycle



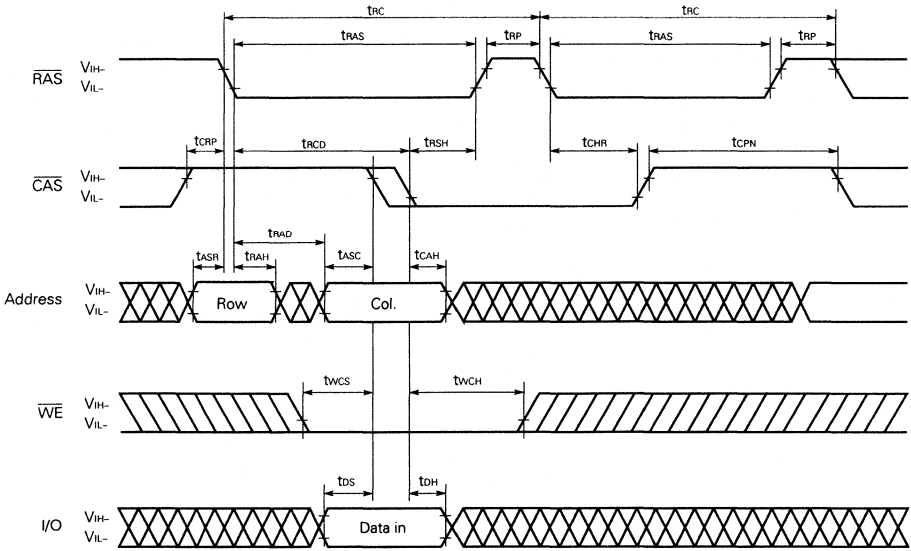
Remark $\overline{\text{WE}}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

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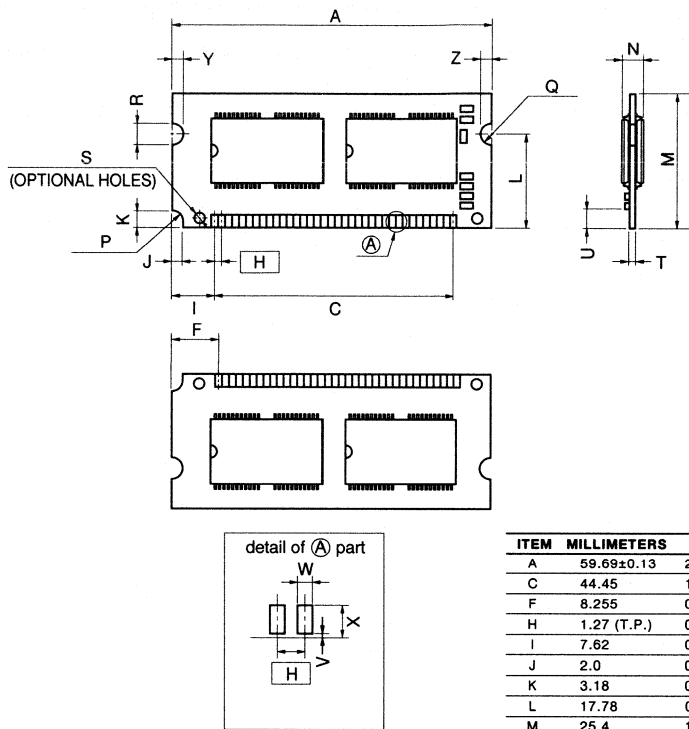


★ Hidden Refresh Cycle (Write)



Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.0	0.079
K	3.18	0.125
L	17.78	0.700
M	25.4	1.000
N	3.8 MAX.	0.150 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ1.8	φ0.071
T	1.0±0.1	0.039 ^{+0.005} _{-0.004}
U	3.18 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039 ^{+0.003} _{-0.002}
X	2.54 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.

M72S-50A3

MOS INTEGRATED CIRCUIT

MC-42S1000LAA32S SERIES

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S1000LAA32S series is a 1,048,576 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 4 M DRAM: μ PD42S4400L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 1,048,576 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S1000LAA32S-A70	70 ns	130 ns	2,016 mW	2.88 mW
MC-42S1000LAA32S-A80	80 ns	150 ns	1,728 mW	(CMOS level input)

- 1,024 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V $\pm$ 0.3 V power supply

Ordering Information

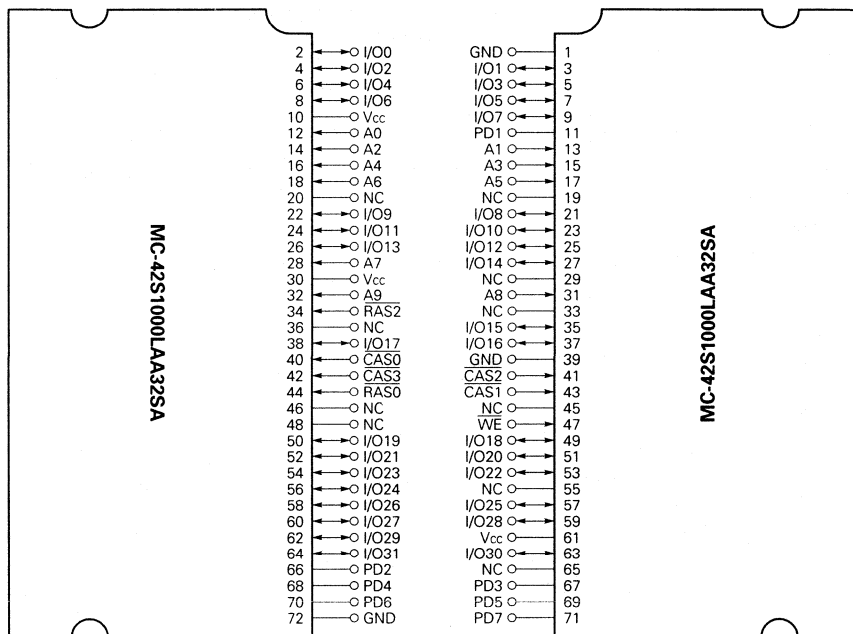
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Part number	Access time (MAX.)	Package	Mounted devices
MC-42S1000LAA32SA-A70	70 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μ PD42S4400LGS (300 mil TSOP (II)) [Double side]
MC-42S1000LAA32SA-A80	80 ns		

The information in this document is subject to change without notice.

Pin Configuration

★ 72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)

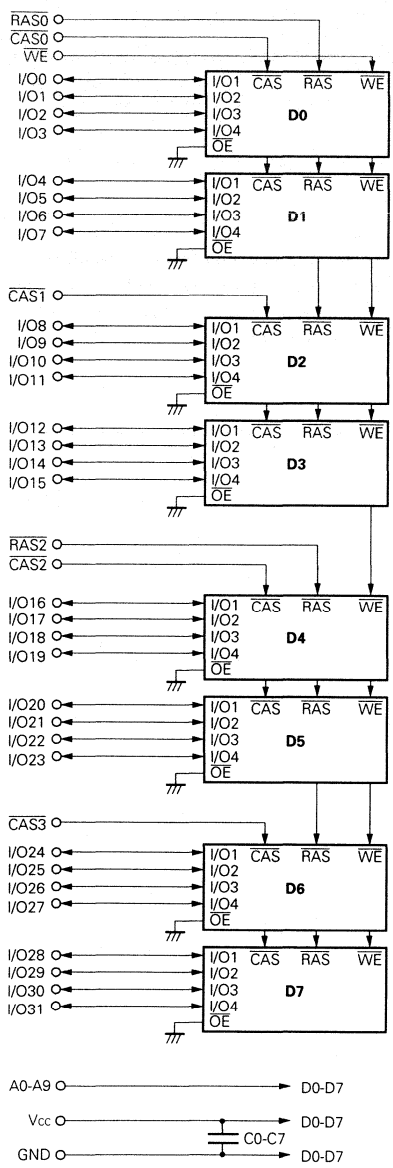


- A0 - A9 : Address Inputs
- I/O0 - I/O31 : Data Inputs/Outputs
- $\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$: Row Address Strobe
- $\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- PD1 - PD7 : Presence Detect Pins
- Vcc : Power Supply
- GND : Ground
- NC : No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time	
		70 ns	80 ns
PD1	11	NC	NC
PD2	66	GND	GND
PD3	67	GND	GND
PD4	68	NC	NC
PD5	69	GND	NC
PD6	70	NC	GND
PD7	71	GND	GND

Block Diagram



Remark D0-D7 : μ PD42S4400LGS (TSOP (III))

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

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Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			55	pF
	C_{I2}	$\overline{WE}$			71	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			36	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			19	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			10	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	560	mA	3, 4, 7
			$t_{\text{RAC}} = 80 \text{ ns}$	480		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $I_o = 0 \text{ mA}$		4.0	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ $I_o = 0 \text{ mA}$		0.8		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} - t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	560	mA	3, 4, 5, 7
			$t_{\text{RAC}} = 80 \text{ ns}$	480		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	480	mA	3, 4, 6
			$t_{\text{RAC}} = 80 \text{ ns}$	400		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	560	mA	3, 4
			$t_{\text{RAC}} = 80 \text{ ns}$	480		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current	I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: $t_{\text{RC}} = 125.0 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}} :$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : V_{H1} or V_{IL} $\overline{\text{WE}} : V_{\text{IH}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAS}} \leq 200 \text{ ns}$	800	μA	3, 4
			$t_{\text{RAS}} \leq 1 \mu\text{s}$	1,200	μA	3, 4
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh current	I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}} :$ $t_{\text{RAS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$		800	μA	4
Input leakage current	I _{I (L)}	$V_i = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V	-5	+5	μA	
Output leakage current	I _{O (L)}	$V_o = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)	-5	+5	μA	
High level output voltage	V _{OH}	$I_o = -2.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +2.0 \text{ mA}$		0.4	V	

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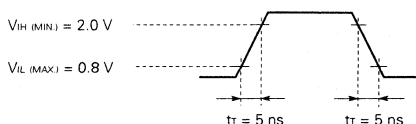
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	45		50		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		20		20	ns	10, 11
Access Time Column Address	t _{AA}		35		40	ns	10, 11
Access Time from CAS Precharge	t _{ACP}		40		45	ns	11
RAS to Column Address Delay Time	t _{RAD}	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	ns	
RAS Precharge Time	t _{RP}	50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	70	125,000	80	125,000	ns	
RAS Hold Time	t _{RSH}	20		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	70		80		ns	
RAS to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	50	25	60	ns	10
CAS to RAS Precharge Time	t _{CRP}	10		10		ns	13
CAS Precharge Time	t _{CPN}	10		10		ns	
CAS Precharge Time (Fast Page Mode)	t _{CP}	10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	40		45		ns	
Row Address Setup Time	t _{ASR}	0		0		ns	
Row Address Hold Time	t _{RAH}	10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	10		10		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		ns	15
Data-in Setup Time	t _{DS}	0		0		ns	16
Data-in Hold Time	t _{DH}	15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		ns	17
$\overline{\text{CAS}}$ Setup Time (CAS before RAS Refresh)	t _{CSR}	10		10		ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	15		15		ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before RAS Self Refresh)	t _{RASS}	100		100		μs	
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before RAS Self Refresh)	t _{RPS}	130		150		ns	
CAS Hold Time (CAS before RAS Self Refresh)	t _{CHS}	-50		-50		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		ns	
Refresh Time	t _{REF}		128		128	ms	

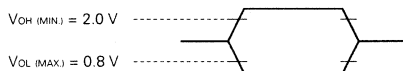
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC5} and I_{CC6} depend on cycle rates (trc and tpc).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq \text{V}_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq \text{V}_{\text{IH}}$ (MIN.).
8. AC measurements assume $\text{tr} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



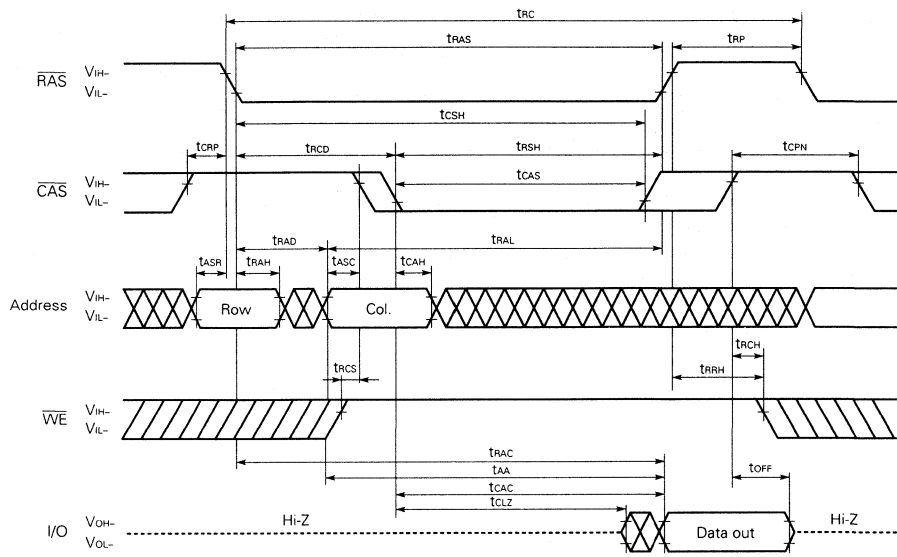
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\text{trAD} > \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$	$\text{trAD} + \text{tAA} (\text{MAX.})$
$\text{trCD} > \text{trCD} (\text{MAX.})$	$\text{tCAC} (\text{MAX.})$	$\text{trCD} + \text{tCAC} (\text{MAX.})$

$\text{trAD} (\text{MAX.})$ and $\text{trCD} (\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD} (\text{MAX.})$ and $\text{trCD} \geq \text{trCD} (\text{MAX.})$ will not cause any operation problems.

11. Loading conditions are 1 TTL and 100 pF.
12. $\text{toFF} (\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $\text{tCRP} (\text{MIN.})$ requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either $\text{trCH} (\text{MIN.})$ or $\text{trRH} (\text{MIN.})$ should be met in read cycles.
15. In early write cycles, $\text{twCH} (\text{MIN.})$ should be met.
16. $\text{tDS} (\text{MIN.})$ and $\text{tDH} (\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $\text{twCS} \geq \text{twCS} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Read Cycle

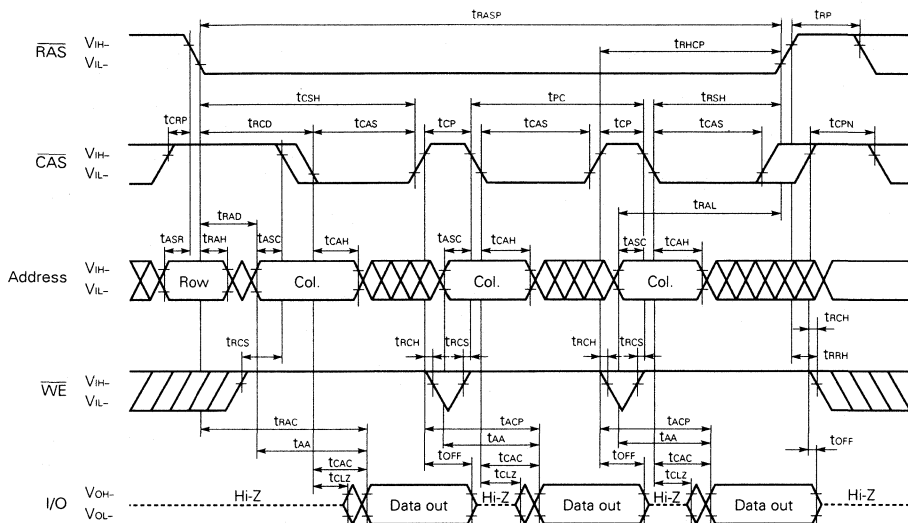


The diagram illustrates the timing relationships for a 256Kbit DRAM. It features five signal traces: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, $\overline{\text{WE}}$, and I/O. The signals are shown with their high (V_{IH}) and low (V_{IL}) levels. Various timing parameters are indicated by horizontal arrows and vertical dashed lines:

- t_{RAS} : RAS access time (from $\overline{\text{RAS}}$ low to high).
- t_{RC} : RAS refresh time (from $\overline{\text{RAS}}$ low to high).
- t_{AP} : RAS to CAS delay (from $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low).
- t_{CRP} : RAS precharge time (from $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low).
- t_{RCD} : RAS to CAS delay (from $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low).
- t_{CSH} : CAS hold time (from $\overline{\text{CAS}}$ low to high).
- t_{RSH} : RAS hold time (from $\overline{\text{RAS}}$ low to high).
- t_{CAS} : CAS access time (from $\overline{\text{CAS}}$ low to high).
- t_{CPN} : CAS precharge time (from $\overline{\text{CAS}}$ high to low).
- t_{ASR} : Address setup time (before Row).
- t_{RAH} : Address hold time (after Row).
- t_{ASC} : Address setup time (before Column).
- t_{CAH} : Address hold time (after Column).
- tw_{CS} : Write cycle time (from $\overline{\text{WE}}$ low to high).
- tw_{CH} : Write cycle time (from $\overline{\text{WE}}$ low to high).
- t_{DS} : Data setup time (before I/O data).
- t_{DH} : Data hold time (after I/O data).

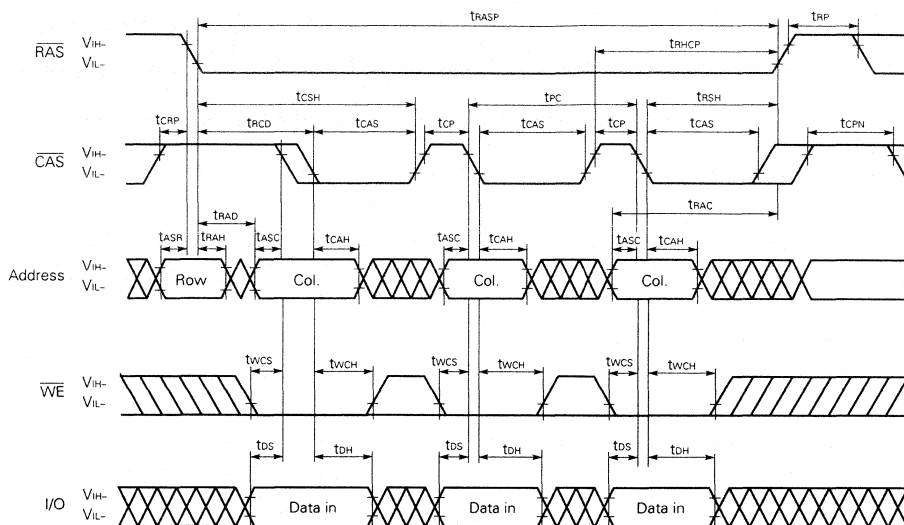
The Address signal shows two access cycles: Row and Column. The $\overline{\text{WE}}$ signal shows two write cycles. The I/O signal shows data being written to the memory during the active periods of the write cycles.

Fast Page Mode Read Cycle



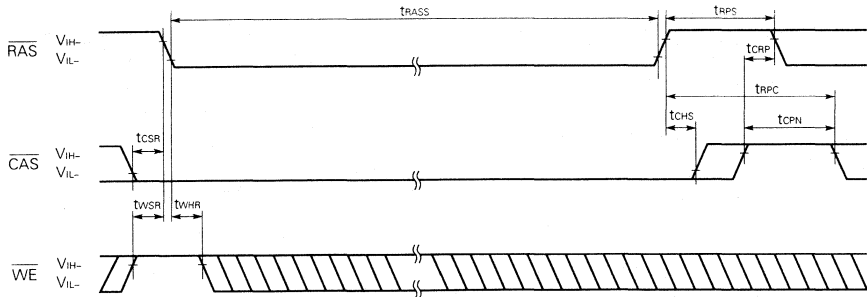
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle



Remark Address : Don't care I/O : Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

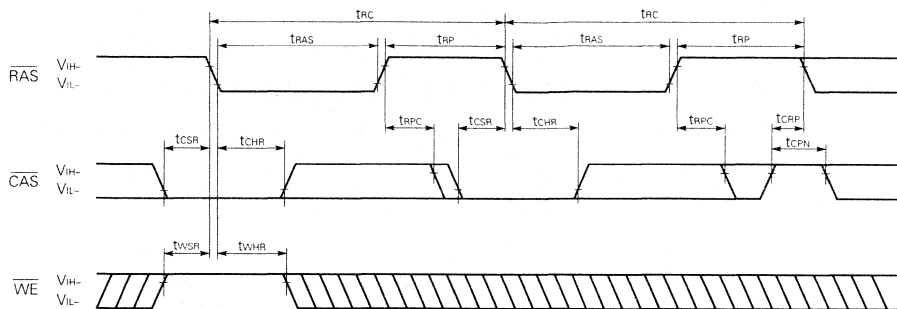
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 1,024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 1,024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

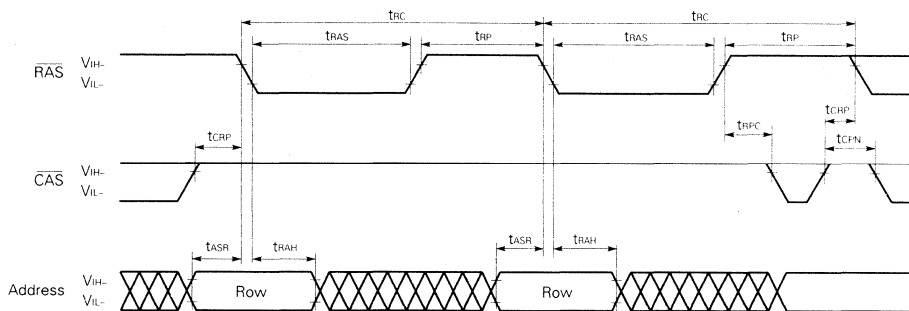
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



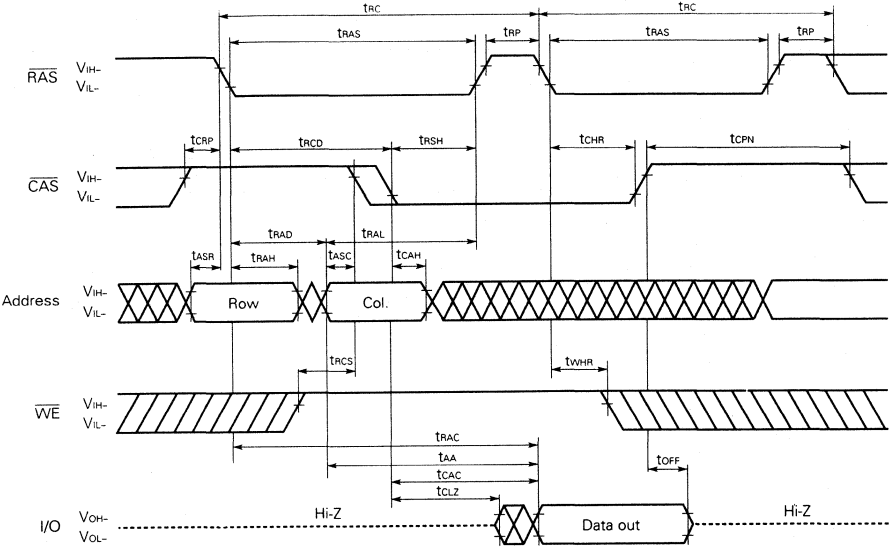
Remark Address : Don't care I/O: Hi-Z

RAS Only Refresh Cycle



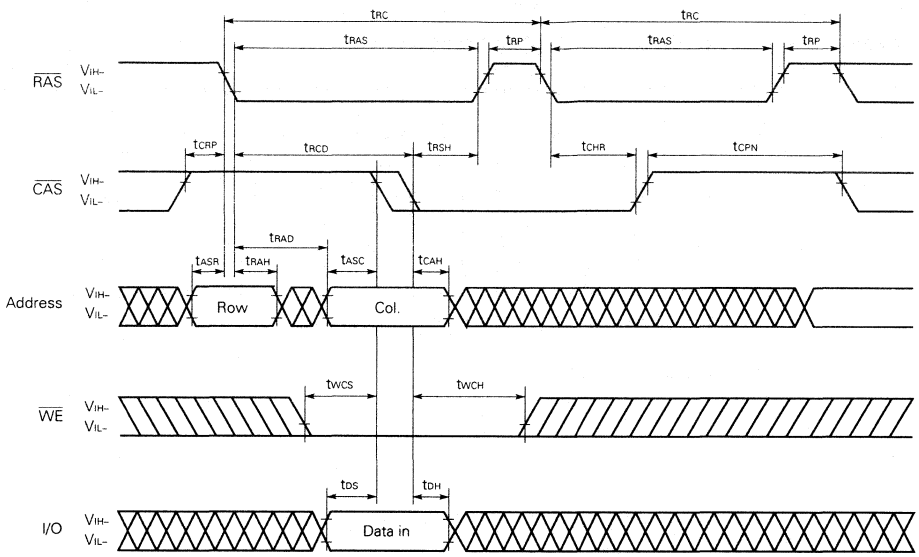
Remark $\overline{\text{WE}}$: Don't care I/O: Hi-Z

★ Hidden Refresh Cycle (Read)



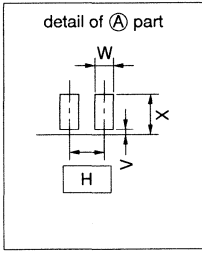
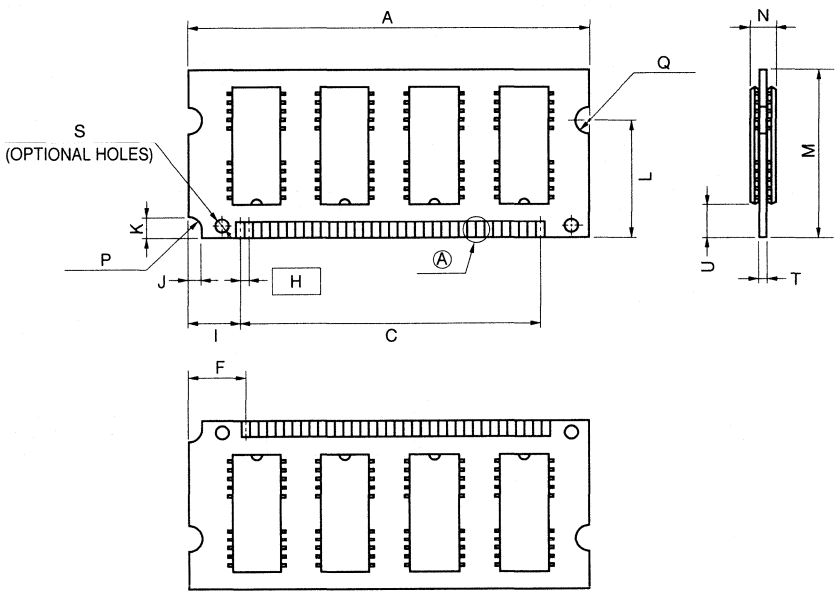
Hidden Refresh Cycle (Write)

★



★ Package Drawing

72PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.03	0.080
K	3.175	0.125
L	17.78	0.700
M	25.4	1.000
N	3.81 MAX.	0.150 MAX.
P	R1.57	R0.062
Q	R2.0	R0.079
S	φ1.8	φ0.071
T	1.016±0.1	0.04±0.004
U	3.175 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72S-50A-1

MOS INTEGRATED CIRCUIT MC-42S1000LAD32S SERIES

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S1000LAD32S series is a 1,048,576 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 2 pieces of 16 M DRAM: μ PD42S18160L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 1,048,576 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S1000LAD32S-A60	60 ns	110 ns	1,080 mW	1.08 mW (CMOS level input)
MC-42S1000LAD32S-A70	70 ns	130 ns	1,008 mW	
MC-42S1000LAD32S-A80	80 ns	150 ns	936 mW	

- 1,024 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V $\pm$ 0.3 V power supply

The information in this document is subject to change without notice.

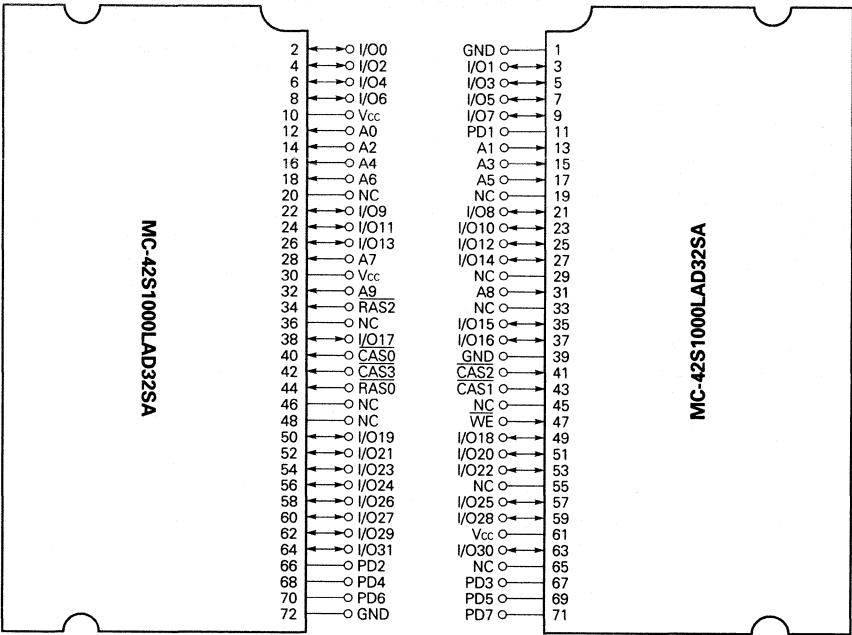
★ Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S1000LAD32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	2 pieces of μ PD42S18160LG5 (400 mil TSOP (II)) [Single side]
MC-42S1000LAD32SA-A70	70 ns		
MC-42S1000LAD32SA-A80	80 ns		

Pin Configuration



72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



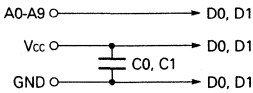
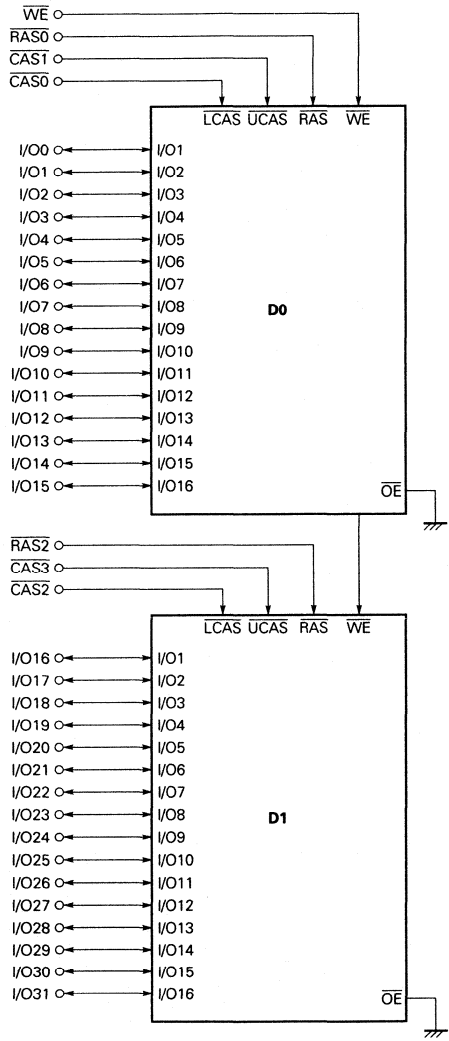
- A0 - A9 : Address Inputs
- I/O0 - I/O31 : Data Inputs/Outputs
- $\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$: Row Address Strobe
- CAS0 - CAS3 : Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- PD1 - PD7 : Presence Detect Pins
- Vcc : Power Supply
- GND : Ground
- NC : No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	NC	NC	NC
PD2	66	GND	GND	GND
PD3	67	GND	GND	GND
PD4	68	NC	NC	NC
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram

Remark D0, D1 : μ PD42S18160L (TSOP (II))



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V _T		−0.5 to +4.6	V
Supply voltage	V _{CC}		−0.5 to +4.6	V
Output current	I _O		20	mA
Power dissipation	P _D		2	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		3.0	3.3	3.6	V
High level input voltage	V _{IH}		2.0		V _{CC} + 0.3	V
Low level input voltage	V _{IL}		−0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 - A9			29	pF
	C _{I2}	$\overline{\text{WE}}$			29	
	C _{I3}	RAS0, RAS2			23	
	C _{I4}	CAS0 - CAS3			17	
Data Input/Output capacitance	C _{IO}	I/O0 - I/O31			12	pF

★

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		300	mA	3, 4, 7
			$t_{\text{RAC}} = 70 \text{ ns}$		280		
			$t_{\text{RAC}} = 80 \text{ ns}$		260		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$I_O = 0 \text{ mA}$		1.0	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$I_O = 0 \text{ mA}$		0.3		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		300	mA	3, 4, 5, 7
			$t_{\text{RAC}} = 70 \text{ ns}$		280		
			$t_{\text{RAC}} = 80 \text{ ns}$		260		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		180	mA	3, 4, 6
			$t_{\text{RAC}} = 70 \text{ ns}$		160		
			$t_{\text{RAC}} = 80 \text{ ns}$		140		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_O = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		300	mA	3, 4
			$t_{\text{RAC}} = 70 \text{ ns}$		280		
			$t_{\text{RAC}} = 80 \text{ ns}$		260		
★ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current	I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: $t_{\text{RC}} = 125.0 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}} :$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : V_{IH} or V_{IL} $\overline{\text{WE}} : V_{\text{IH}}$ $I_O = 0 \text{ mA}$	$t_{\text{RAS}} \leq 1 \mu\text{s}$		360	μA	3, 4
★ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh current	I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}} :$ $t_{\text{RAS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_O = 0 \text{ mA}$			300	μA	4
Input leakage current	I _{I (L)}	$V_I = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V		-5	+5	μA	
Output leakage current	I _{O (L)}	$V_O = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)		-5	+5	μA	
High level output voltage	V _{OH}	$I_O = -2.0 \text{ mA}$		2.4		V	
Low level output voltage	V _{OL}	$I_O = +2.0 \text{ mA}$			0.4	V	

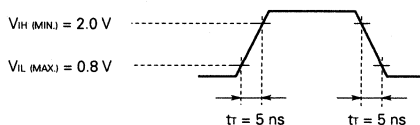
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Access Time from RAS	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t _{AA}		30		35		40	ns	10, 11
Access Time from CAS Precharge	t _{ACP}		35		40		45	ns	11
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	t _{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{RP}	40		50		60		ns	
RAS Pulse Width	t _{RA}	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RA} SP	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	t _{RH}	15		18		20		ns	
CAS Pulse Width	t _{CA}	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	t _{CH}	60		70		80		ns	
RAS to $\overline{\text{CAS}}$ Delay Time	t _{RC} D	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	t _{CRP}	5		5		5		ns	13
CAS Precharge Time	t _{CP}	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
RAS Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RH} CP	35		40		45		ns	
Row Address Setup Time	t _{AS} R	0		0		0		ns	
Row Address Hold Time	t _{RA} H	10		10		12		ns	
Column Address Setup Time	t _{AS} C	0		0		0		ns	
Column Address Hold Time	t _{CA} H	15		15		15		ns	
Column Address Lead Time Referenced to RAS	t _{AL}	30		35		40		ns	
Read Command Setup Time	t _{RC} S	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RR} H	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RC} H	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _W CH	10		10		15		ns	15
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WC} S	0		0		0		ns	17
CAS Setup Time ($\overline{\text{CAS}}$ before RAS Refresh)	t _{CS} R	5		5		5		ns	
CAS Hold Time ($\overline{\text{CAS}}$ before RAS Refresh)	t _{CH} R	10		10		10		ns	
RAS Pulse Width ($\overline{\text{CAS}}$ before RAS Refresh)	t _{RA} SS	100		100		100		μ s	
RAS Precharge Time ($\overline{\text{CAS}}$ before RAS Self Refresh)	t _{RP} S	110		130		150		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before RAS Self Refresh)	t _{CH} S	-50		-50		-50		ns	
$\overline{\text{WE}}$ Hold Time	t _{WH} R	15		15		15		ns	
Refresh Time	t _{REF}		128		128		128	ms	

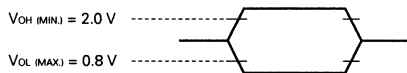
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. Icc1 , Icc3 , Icc4 , Icc5 and Icc6 depend on cycle rates (t_{rc} and t_{pc}).
4. Specified values are obtained with outputs unloaded.
5. Icc3 is measured assuming that all column address inputs are held at either high or low.
6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.).
8. AC measurements assume $t_{\text{T}} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

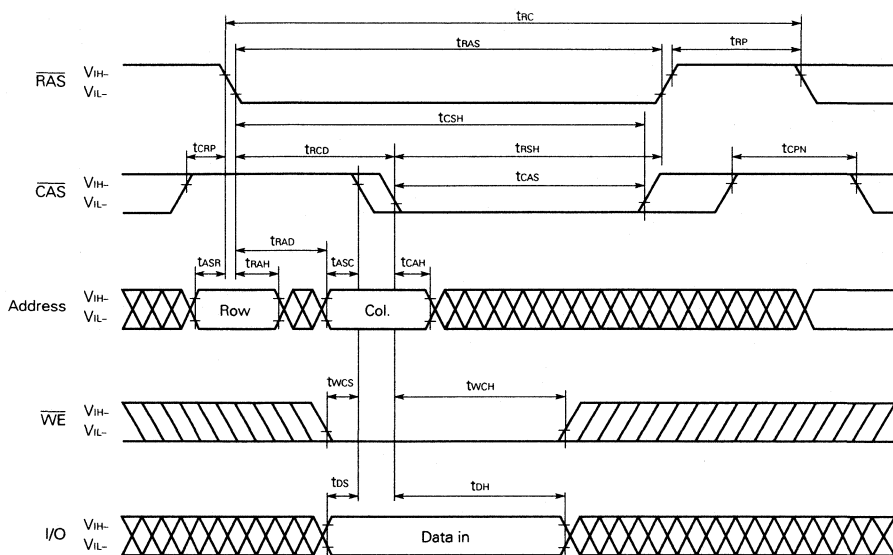
Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX.})$	$t_{\text{RAC}} (\text{MAX.})$	$t_{\text{RAC}} (\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX.})$	$t_{\text{AA}} (\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}} (\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}} (\text{MAX.})$	$t_{\text{CAC}} (\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}} (\text{MAX.})$

$t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} (\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{MAX.})$ will not cause any operation problems.

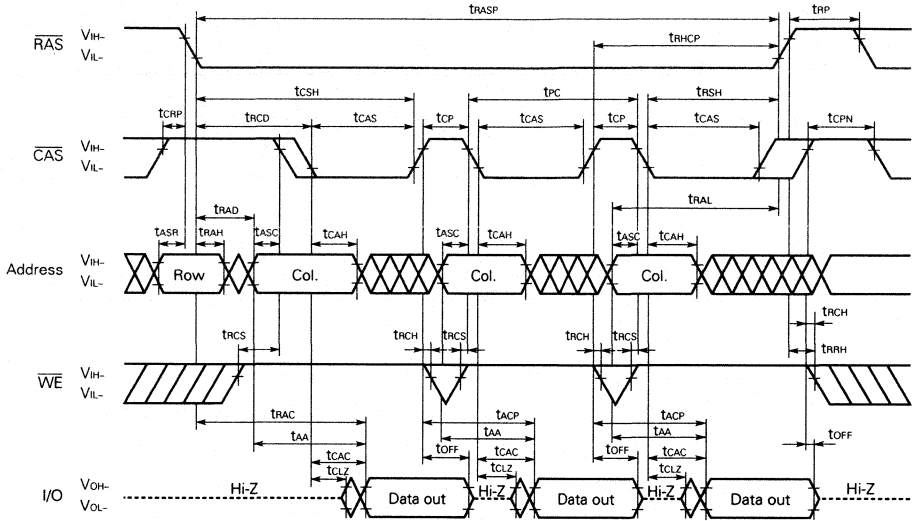
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{\text{OFF}} (\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $t_{\text{CRP}} (\text{MIN.})$ requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either $t_{\text{RCH}} (\text{MIN.})$ or $t_{\text{RRH}} (\text{MIN.})$ should be met in read cycles.
15. In early write cycles, $t_{\text{WCH}} (\text{MIN.})$ should be met.
16. $t_{\text{DS}} (\text{MIN.})$ and $t_{\text{DH}} (\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

[illegible]

Early Write Cycle

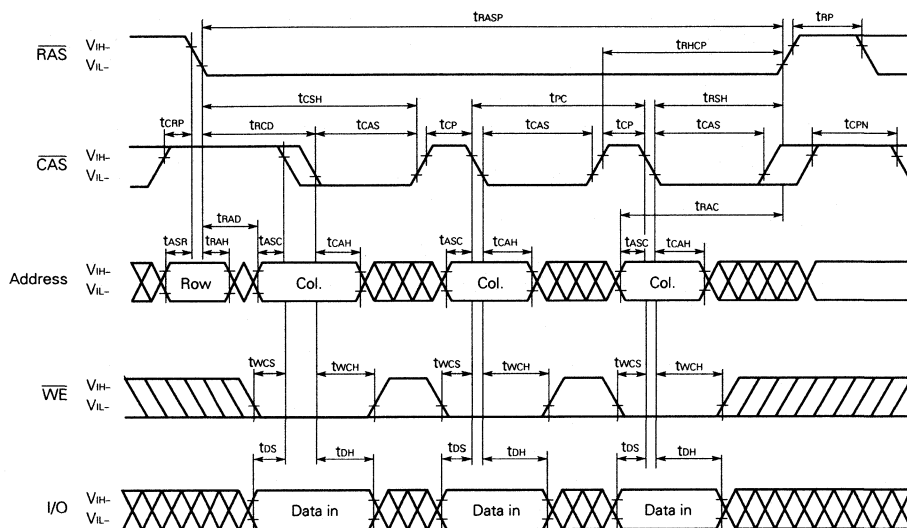


Fast Page Mode Read Cycle



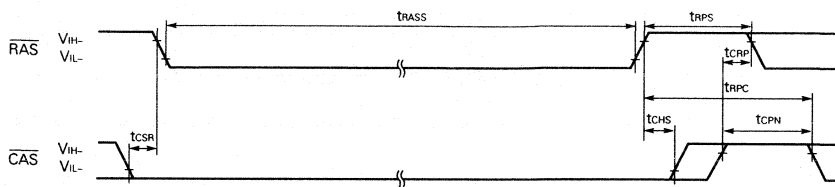
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh Cycle



Remark Address, $\overline{\text{WE}}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh can be used independently when used in combination with distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh; However, when used in combination with burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh or with burst long $\overline{\text{RAS}}$ only refresh, the following cautions must be observed.

(1) Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Burst $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Long Refresh

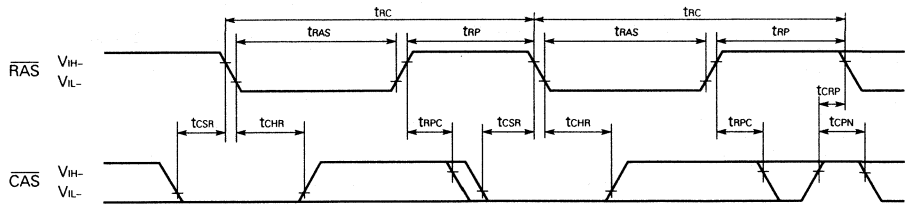
When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh are used in combination, please perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh 1,024 times within a 16 ms interval just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

(2) Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Burst Long $\overline{\text{RAS}}$ Only Refresh

When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{RAS}}$ only refresh are used in combination, please perform $\overline{\text{RAS}}$ only refresh 1,024 times within a 16 ms interval just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

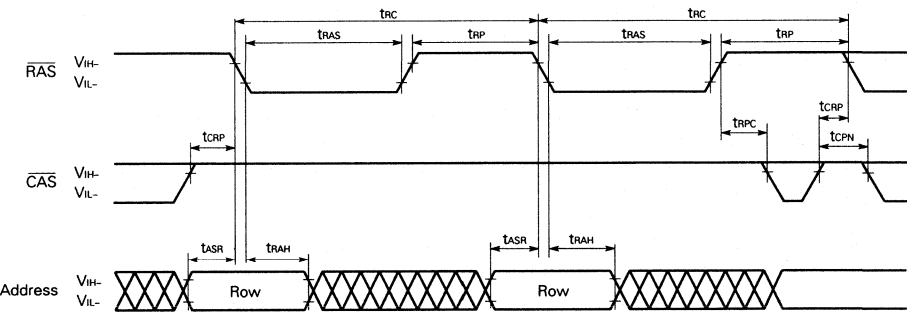
For details, please refer to **How to use DRAM** User's Manual.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



Remark Address, $\overline{\text{WE}}$: Don't care I/O: Hi-Z

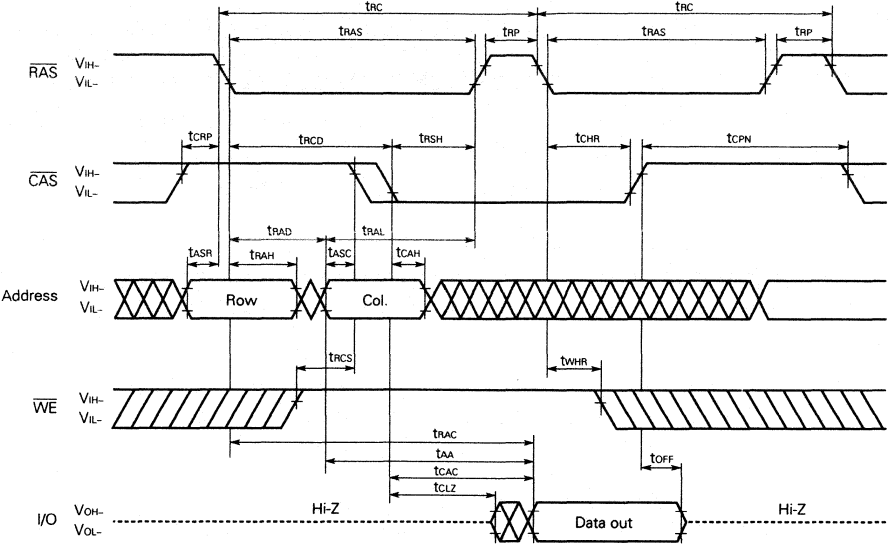
$\overline{\text{RAS}}$ Only Refresh Cycle



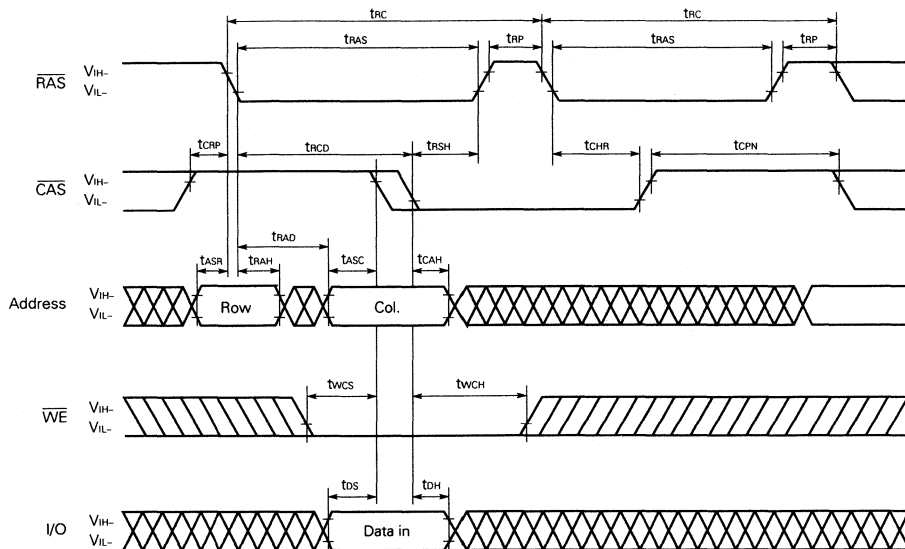
Remark $\overline{\text{WE}}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

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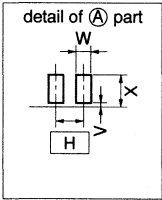
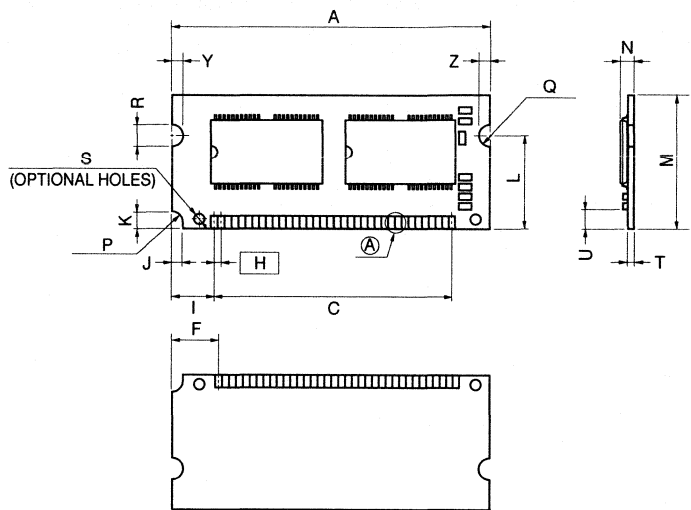


★ Hidden Refresh Cycle (Write)



Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.0	0.079
K	3.18	0.125
L	17.78	0.700
M	25.4	1.000
N	2.45 MAX.	0.097 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ1.8	φ0.071
T	1.0±0.1	0.039 ^{+0.005} _{-0.004}
U	3.18 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039 ^{+0.003} _{-0.002}
X	2.54 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.

M72S-50A4

MOS INTEGRATED CIRCUIT

MC-424000AB72F

4 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-424000AB72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μ PD4217400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000AB72-60	60 ns	110 ns	10.73 W	430 mW (CMOS level input)
MC-424000AB72-70	70 ns	130 ns	9.79 W	
MC-424000AB72-80	80 ns	150 ns	8.84 W	

- 2,048 refresh cycles/32 ms
- CAS before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ± 0.25 V power supply

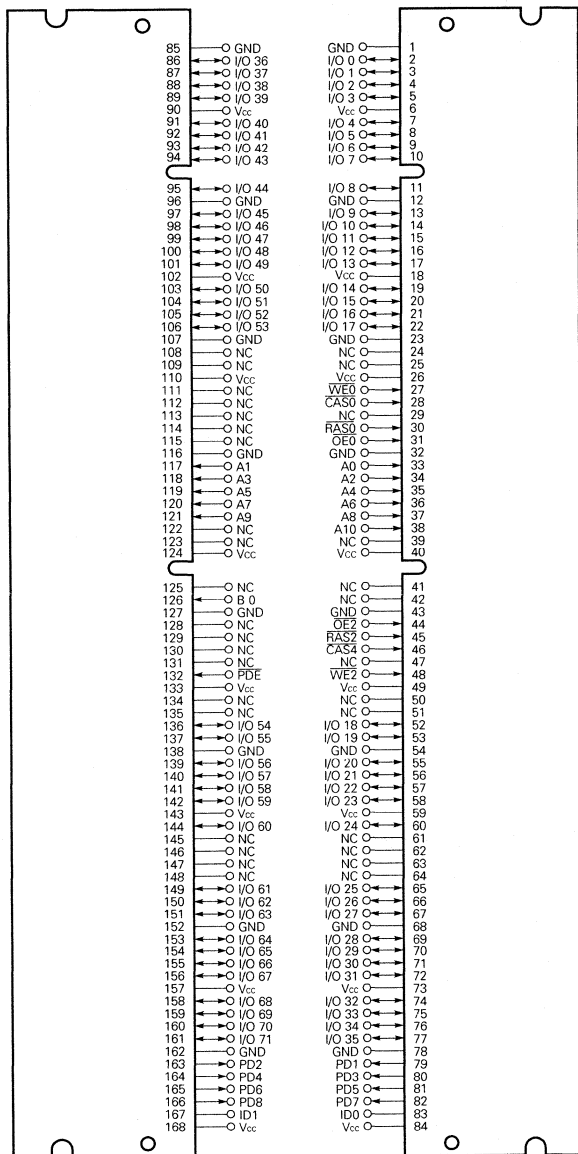
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000AB72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of μ PD4217400G3 (300 mil TSOP(III)) [Double side]
MC-424000AB72F-70	70 ns		
MC-424000AB72F-80	80 ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



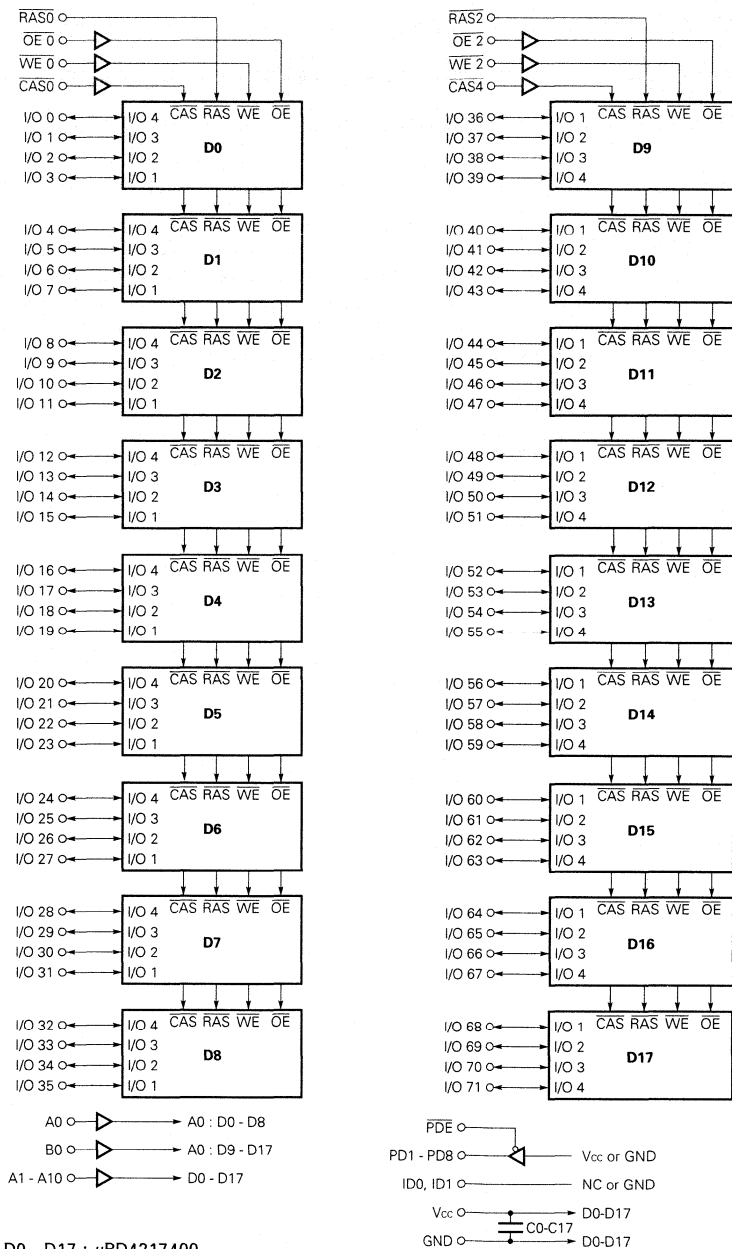
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	H	H	H
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	H	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

- A0 - A10, B0 : Address Inputs
- I/O 0 - I/O 71 : Data Inputs/Outputs
- RAS0, RAS2 : Row Address Strobe
- CAS0, CAS4 : Column Address Strobe
- WE0, WE2 : Write Enable
- OE0, OE2 : Output Enable
- PDE : Presence Detect Enable
- PD1 - PD8 : Presence Detect Pins
- ID0, ID1 : Identity Pins
- Vcc : Power Supply
- GND : Ground
- NC : No connection

Block Diagram



Remark D0 - D17 : μ PD4217400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		20	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}} (\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		2,044	mA	3, 4, 7
			$t_{\text{RAC}} = 70 \text{ ns}$		1,864		
			$t_{\text{RAC}} = 80 \text{ ns}$		1,684		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.})$ $I_o = 0 \text{ mA}$			100	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ $I_o = 0 \text{ mA}$			82		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}} (\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		2,044	mA	3, 4, 5, 7
			$t_{\text{RAC}} = 70 \text{ ns}$		1,864		
			$t_{\text{RAC}} = 80 \text{ ns}$		1,684		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}} (\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}} (\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		1,324	mA	3, 4, 6
			$t_{\text{RAC}} = 70 \text{ ns}$		1,144		
			$t_{\text{RAC}} = 80 \text{ ns}$		964		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}} (\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		2,044	mA	3, 4
			$t_{\text{RAC}} = 70 \text{ ns}$		1,864		
			$t_{\text{RAC}} = 80 \text{ ns}$		1,684		
Input leakage current	I _{I (L)}	$V_I = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	$\overline{\text{RAS}}$	-10	+10	μA	
			Others	-5	+1		
Output leakage current	I _{O (L)}	$V_O = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)		-10	+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$		2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

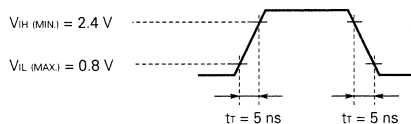
Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t _{RWC}	175		195		220		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	85		90		105		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t _{AA}		35		40		45	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		40		45		50	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEa}		15		18		20	ns	11
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	t _{CLZ}	0		0		0		ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OEZ}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0		0		0		ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		60		ns	
RAS Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	t _{RSH}	15		18		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		ns	
RAS to CAS Delay Time	t _{RCD}	20	40	20	50	25	60	ns	10
CAS to RAS Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
RAS Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40		45		50		ns	
Row Address Setup Time	t _{ASR}	5		5		5		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{AL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
WE Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
WE Pulse Width	t _{WP}	10		10		15		ns	15

Parameter	Symbol	trac = 60 ns		trac = 70 ns		trac = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tOH	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS to WE Delay Time	tcWD	40		43		50		ns	17
RAS to WE Delay Time	trWD	95		105		120		ns	17
CAS Precharge to WE Delay Time	tcpWD	58		65		70		ns	17
Column Address to WE Delay Time	tawD	60		65		75		ns	17
WE Lead Time Referenced to RAS	trWL	25		25		25		ns	
WE Lead Time Referenced to CAS	tcWL	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	tCSR	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tCHR	10		10		10		ns	
WE Setup Time	tWSR	10		10		10		ns	
WE Hold Time	tWHR	15		15		15		ns	
Refresh Time	tREF		32		32		32	ms	

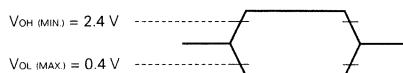
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. t_{CC1} , t_{CC3} , t_{CC4} and t_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. t_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. t_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. t_{CC1} and t_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{IL}$ (MAX.) and $\overline{\text{CAS}} \geq V_{IH}$ (MIN.).
8. AC measurements assume $t_r = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



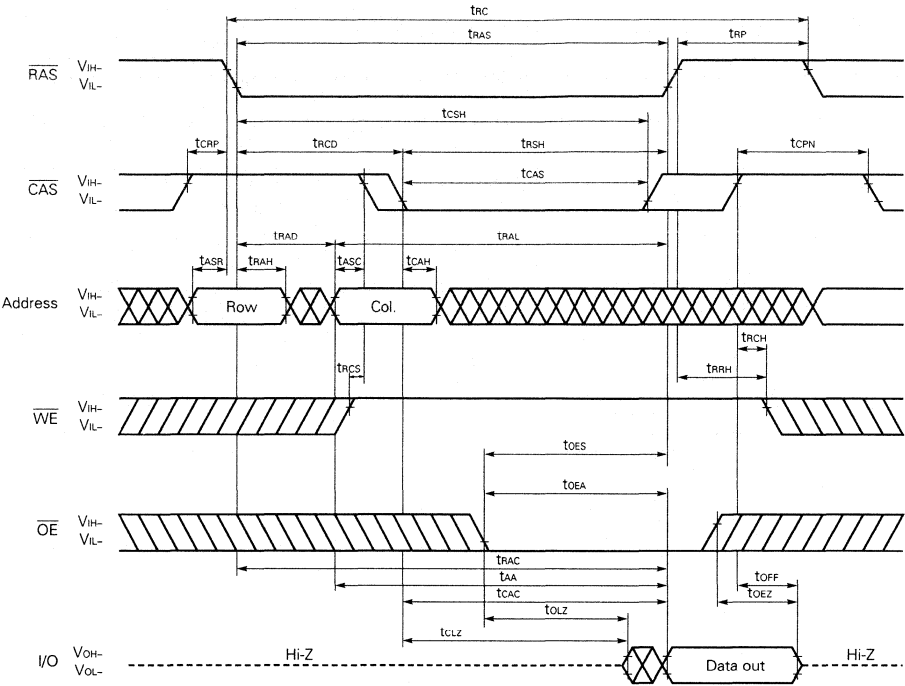
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

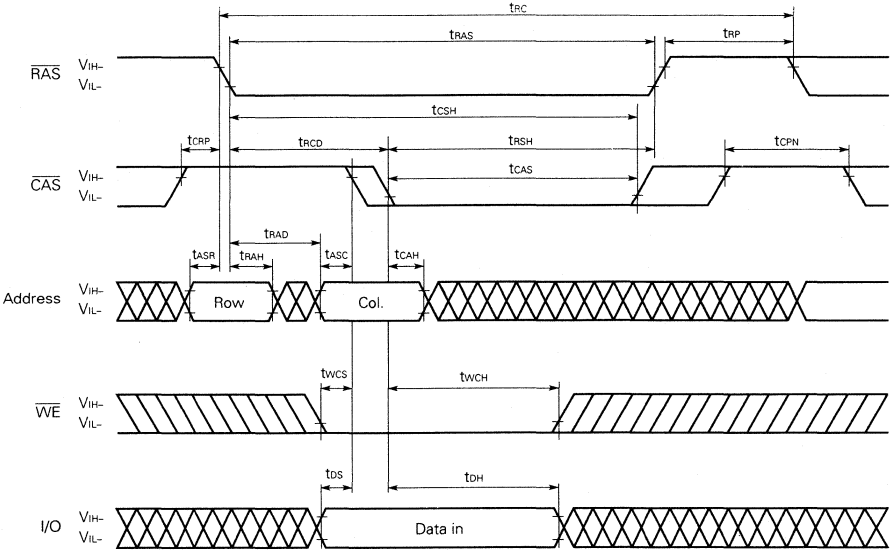
trAD (MAX.) and trCD (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. tOFF (MAX.) and tOEZ (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. tCRP (MIN.) requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either trCH (MIN.) or trRH (MIN.) should be met in read cycles.
15. tWP (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, tWCH (MIN.) should be met.
16. tDS (MIN.) and tDH (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
17. If $\text{twCS} \geq \text{twCS (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{trWD} \geq \text{trWD (MIN.)}$, $\text{tcWD} \geq \text{tcWD (MIN.)}$, $\text{tAWD} \geq \text{tAWD (MIN.)}$ and $\text{tcpWD} \geq \text{tcpWD (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Read Cycle

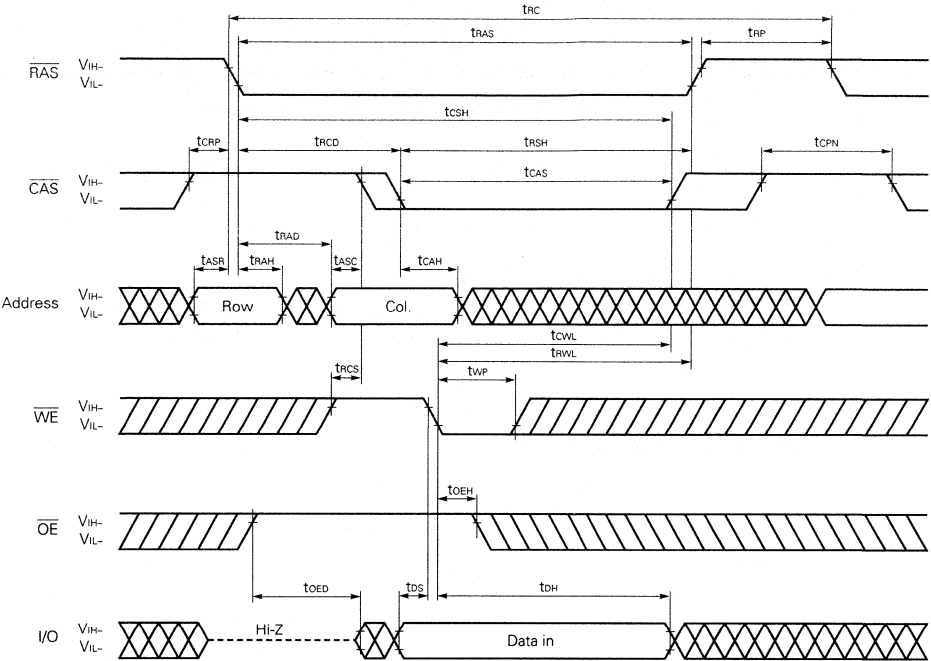


Early Write Cycle

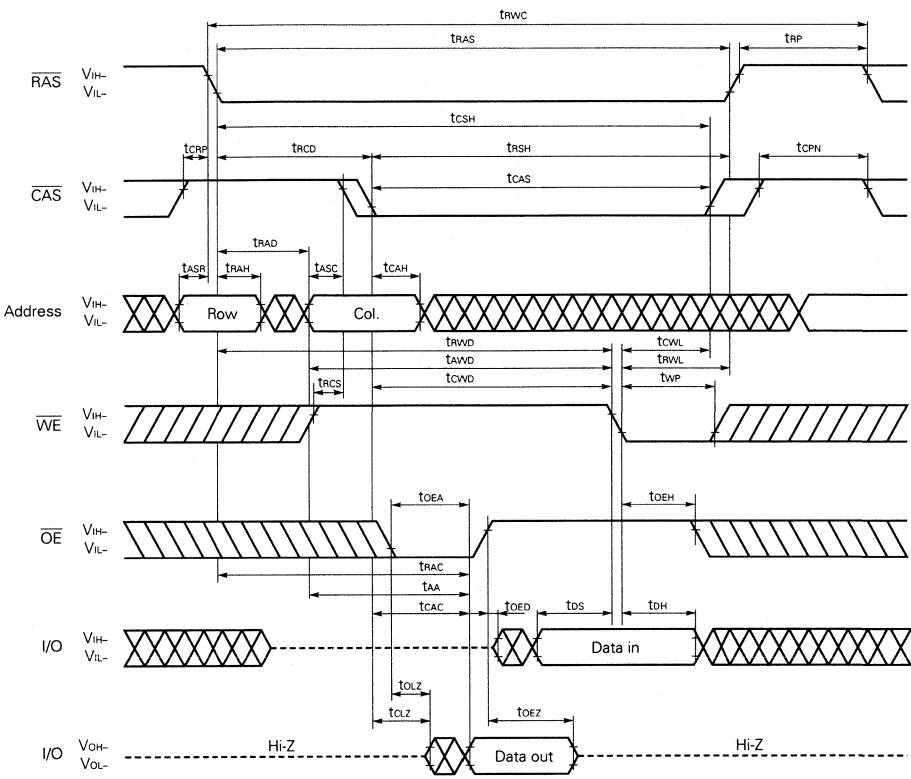


Remark $\overline{\text{OE}}$: Don't care

Late Write Cycle



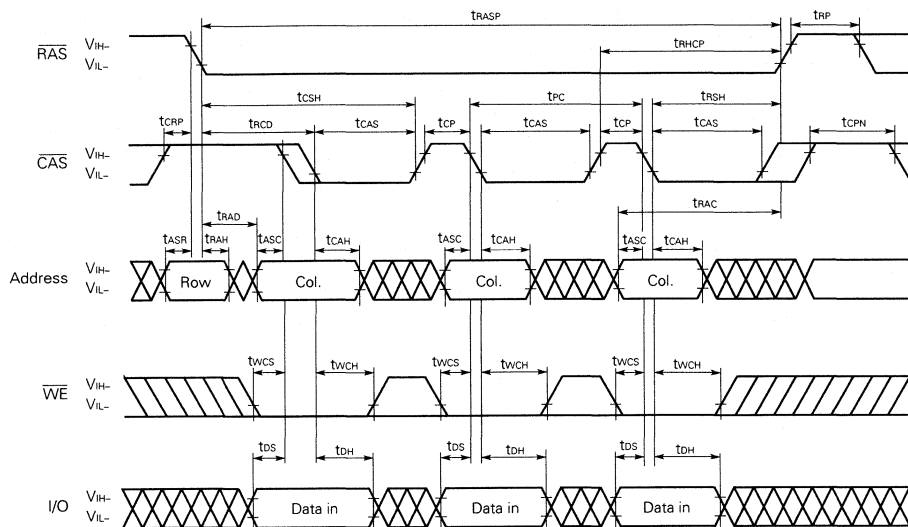
Read Modify Write Cycle



[illegible]

1289

Fast Page Mode Early Write Cycle



Remarks 1. $\overline{\text{OE}}$: Don't care

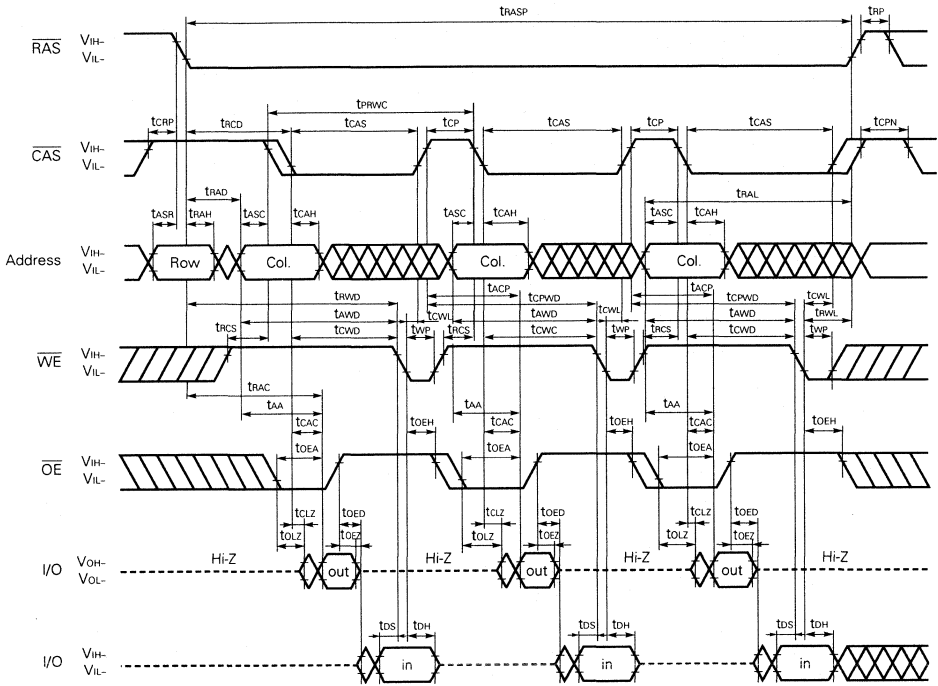
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

The diagram illustrates the timing relationships for a 256Kbit DRAM. It shows the signals RAS, CAS, Address, WE, OE, and I/O. The timing parameters are defined as follows:

- t_{RASP} : RAS pulse width
- t_{RHP} : RAS hold time
- t_{AP} : RAS to CAS delay
- t_{CSH} : CAS hold time
- t_{CP} : CAS pulse width
- t_{CAS} : CAS access time
- t_{CPN} : CAS to next pulse delay
- t_{ASR} : Address setup time
- t_{RAH} : Address row hold time
- t_{ASC} : Address to CAS delay
- t_{CAH} : Address column hold time
- t_{OEW} : Output enable width
- t_{WP} : Write pulse width
- t_{OEH} : Output enable hold time
- t_{DS} : Data setup time
- t_{DH} : Data hold time
- t_{OED} : Output enable delay

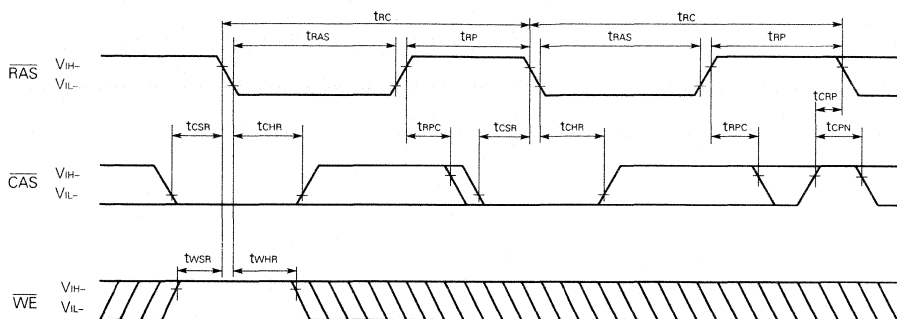
1291

Fast Page Mode Read Modify Write Cycle



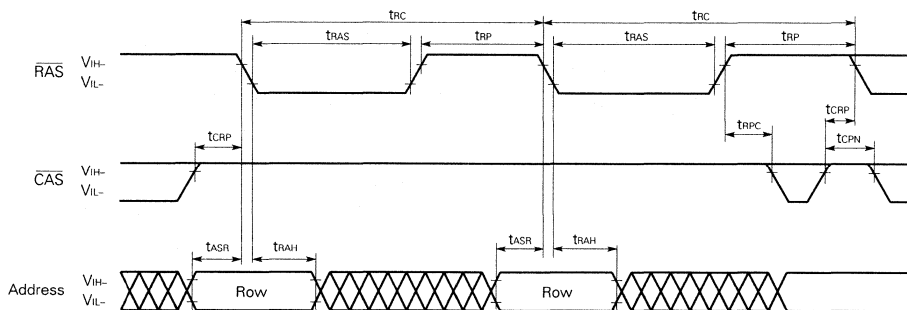
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

CAS Before RAS Refresh Cycle



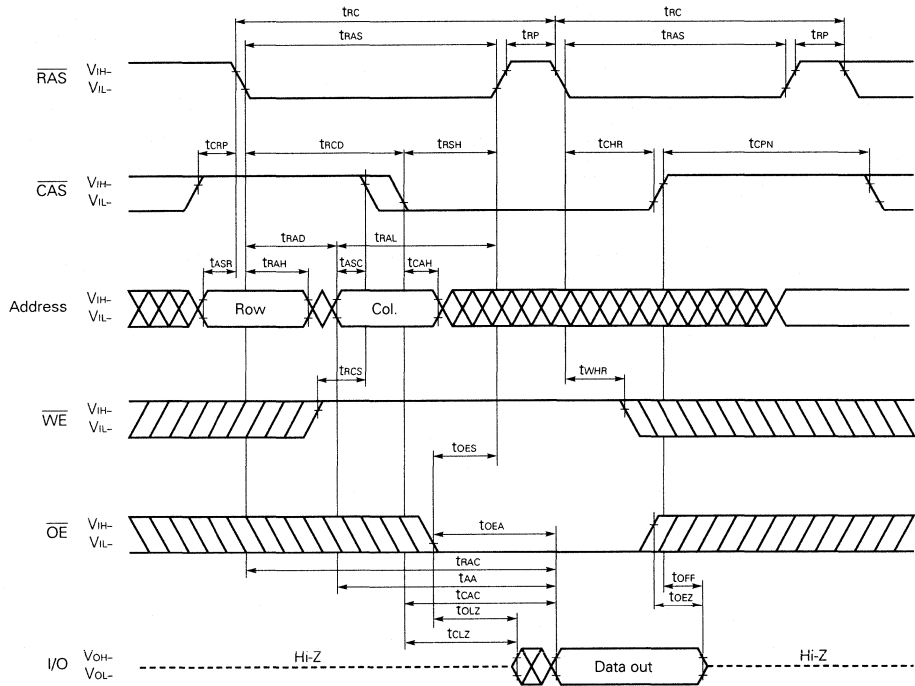
Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

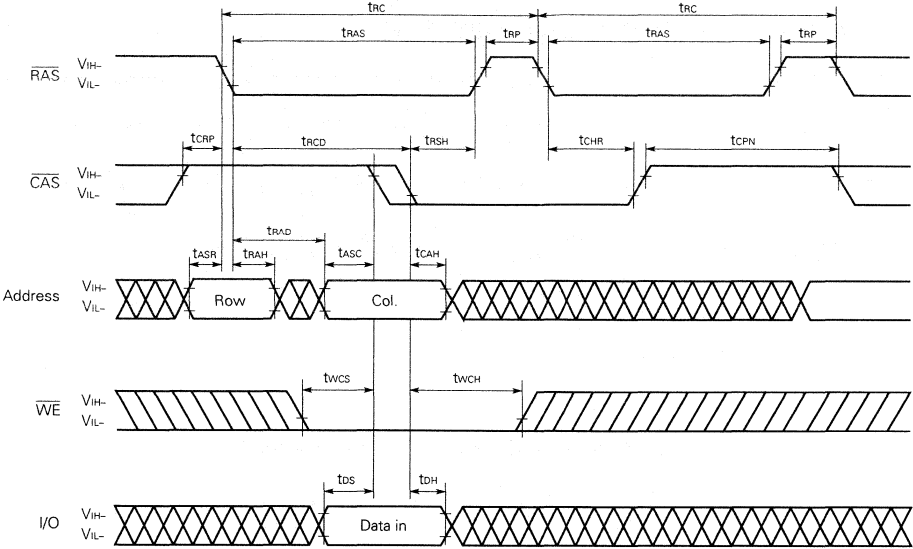


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



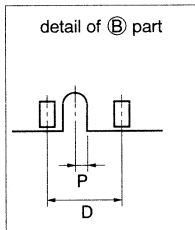
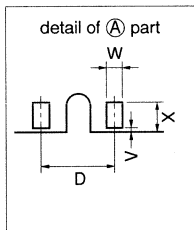
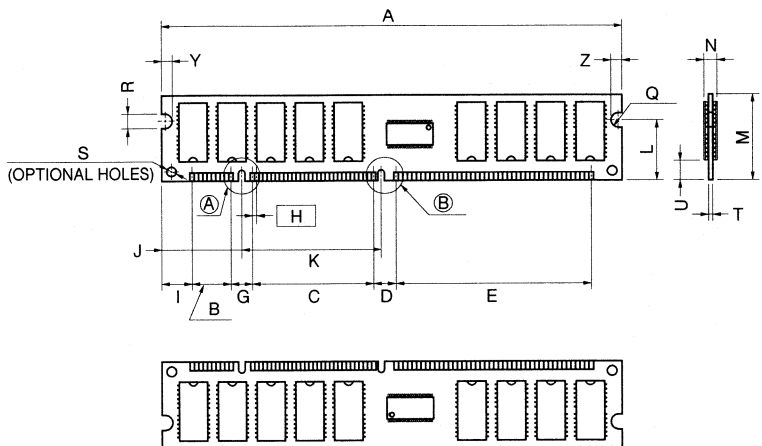
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A2

MOS INTEGRATED CIRCUIT
MC-424000AC72F4 M-WORD BY 72-BIT DYNAMIC RAM MODULE
FAST PAGE MODE (ECC)

Description

The MC-424000AC72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μ PD4216400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- Fast access and cycle time

★

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000AC72-60	60 ns	110 ns	8.84 W	430 mW (CMOS level input)
MC-424000AC72-70	70 ns	130 ns	7.90 W	
MC-424000AC72-80	80 ns	150 ns	6.95 W	

- 4,096 refresh cycles/64 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ± 0.25 V power supply

Ordering Information

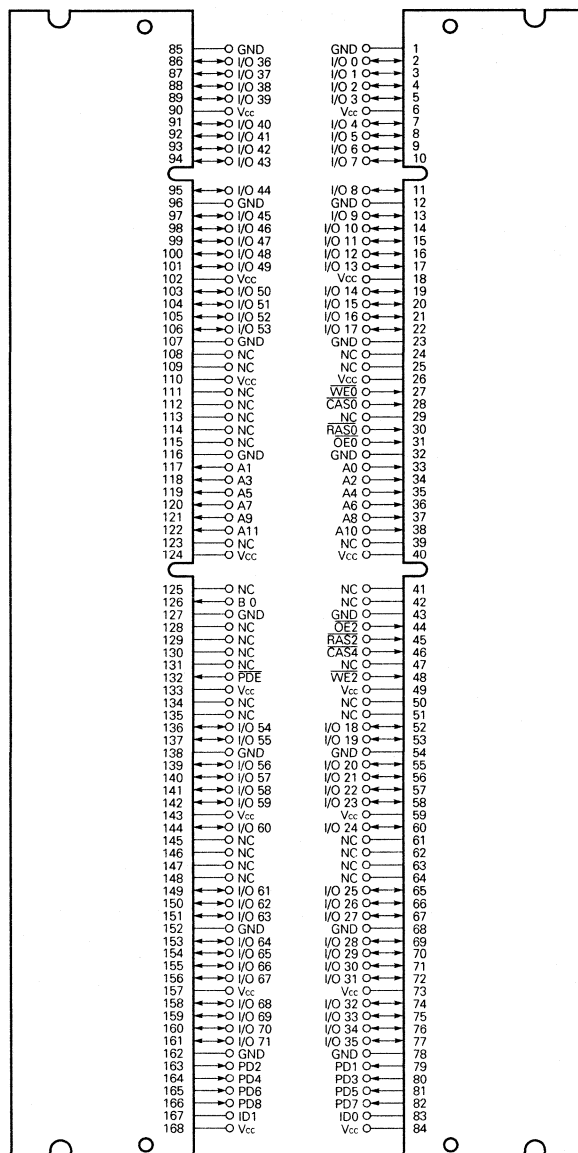
Part number	Access time (MAX.)	Package	Mounted devices
MC-424000AC72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of μ PD4216400G3 (300 mil TSOP(III)) [Double side]
MC-424000AC72F-70	70 ns		
MC-424000AC72F-80	80 ns		

The information in this document is subject to change without notice.

The mark ★ shows revised point.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



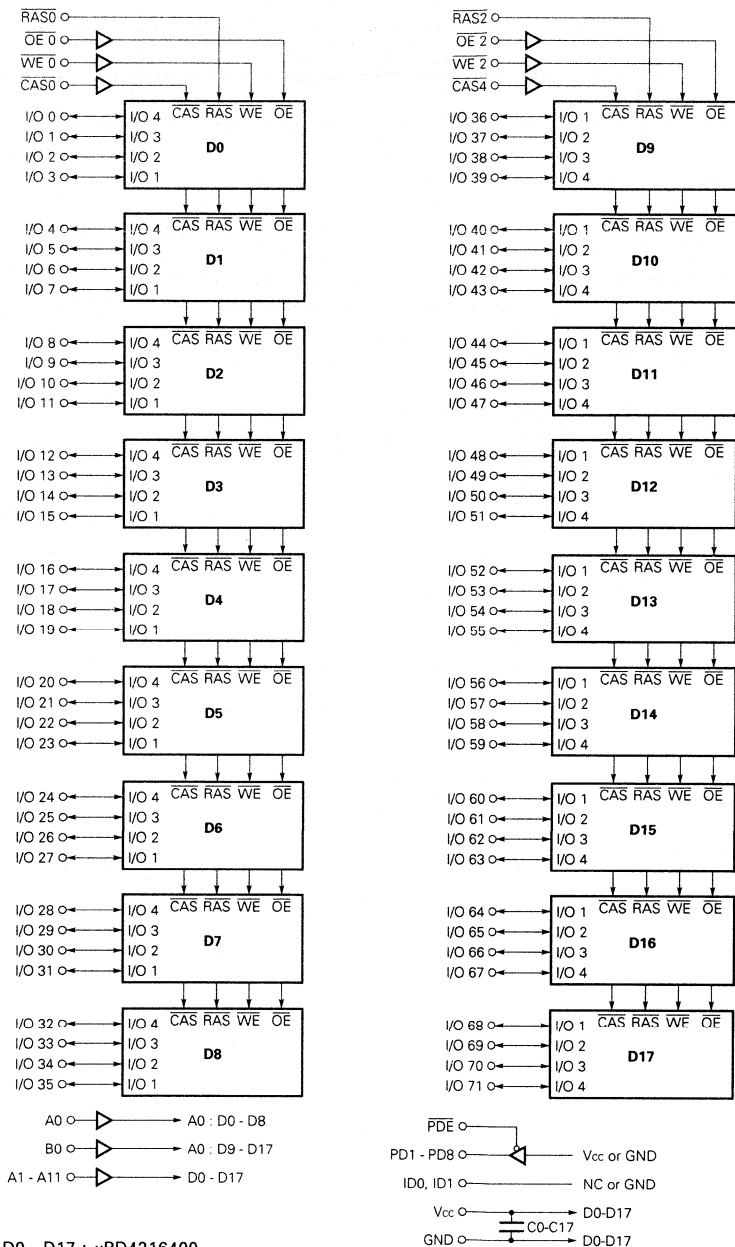
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	H	H	H
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	H	H
PD7	82	H	L	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

- A0 - A11, B0 : Address Inputs
 I/O 0 - I/O 71 : Data Inputs/Outputs
 RAS0, RAS2 : Row Address Strobe
 CAS0, CAS4 : Column Address Strobe
 WE0, WE2 : Write Enable
 OE0, OE2 : Output Enable
 PDE : Presence Detect Enable
 PD1 - PD8 : Presence Detect Pins
 ID0, ID1 : Identity Pins
 Vcc : Power Supply
 GND : Ground
 NC : No connection

Block Diagram



Remark D0 - D17 : μ PD4216400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		20	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

★

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}} (\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1,684	mA	3, 4, 7
			$t_{\text{RAC}} = 70 \text{ ns}$	1,504		
			$t_{\text{RAC}} = 80 \text{ ns}$	1,324		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.})$ $I_o = 0 \text{ mA}$		100	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ $I_o = 0 \text{ mA}$		82		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}} (\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1,684	mA	3, 4, 5, 7
			$t_{\text{RAC}} = 70 \text{ ns}$	1,504		
			$t_{\text{RAC}} = 80 \text{ ns}$	1,324		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}} (\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}} (\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1,324	mA	3, 4, 6
			$t_{\text{RAC}} = 70 \text{ ns}$	1,144		
			$t_{\text{RAC}} = 80 \text{ ns}$	964		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}} (\text{MIN.})$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1,684	mA	3, 4
			$t_{\text{RAC}} = 70 \text{ ns}$	1,504		
			$t_{\text{RAC}} = 80 \text{ ns}$	1,324		
Input leakage current	I _{I (L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	$\overline{\text{RAS}}$	-10	+10	μA
			Others	-5	+1	
Output leakage current	I _{O (L)}	$V_o = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)		-10	+10	μA
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

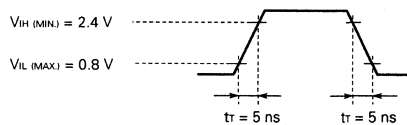
Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t _{RMWC}	175		195		220		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	85		90		105		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t _{AA}		35		40		45	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		40		45		50	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEA}		15		18		20	ns	11
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	t _{CLZ}	0		0		0		ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OEZ}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0		0		0		ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{RP}	40		50		60		ns	
RAS Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RS}	15		18		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CS}	60		70		80		ns	
RAS to CAS Delay Time	t _{RCD}	20	40	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40		45		50		ns	
Row Address Setup Time	t _{ASR}	5		5		5		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to RAS	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
$\overline{\text{WE}}$ Pulse Width	t _{WP}	10		10		15		ns	15

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	40		43		50		ns	17
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	95		105		120		ns	17
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	58		65		70		ns	17
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	60		65		75		ns	17
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	25		25		25		ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15		15		15		ns	
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	5		5		5		ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10		10		10		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		64		64		64	ms	

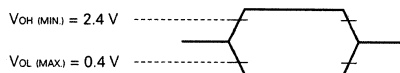
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{ac} and t_{pc}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}$ (MAX.) and $\overline{\text{CAS}} \geq V_{\text{IH}}$ (MIN.).
8. AC measurements assume t_r = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



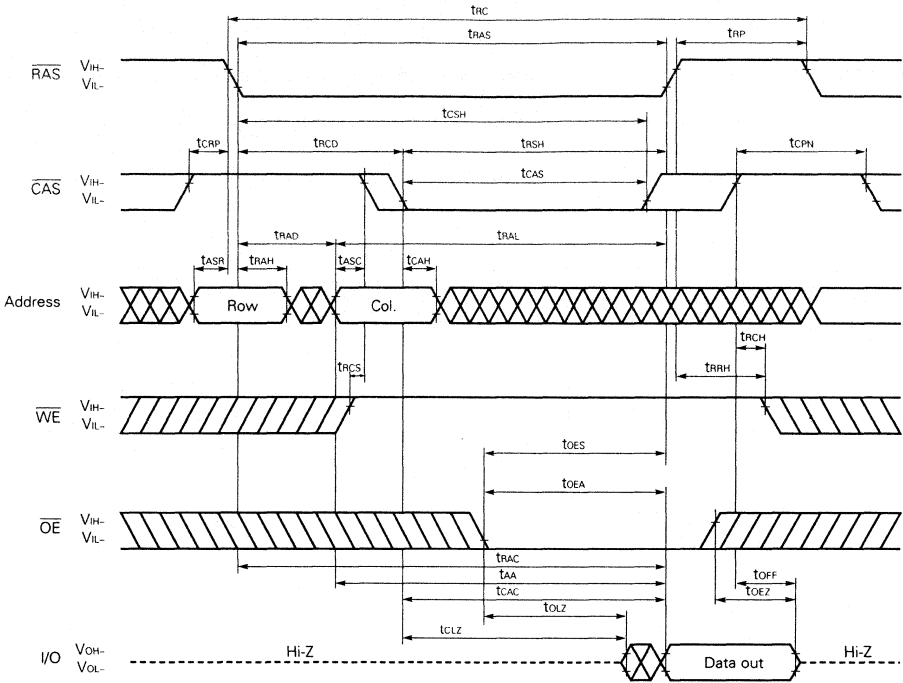
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{t}_{\text{RAD}} \leq \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \leq \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{RAC}}(\text{MAX.})$	$\text{t}_{\text{RAC}}(\text{MAX.})$
$\text{t}_{\text{RAD}} > \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \leq \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{AA}}(\text{MAX.})$	$\text{t}_{\text{RAD}} + \text{t}_{\text{AA}}(\text{MAX.})$
$\text{t}_{\text{RCD}} > \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{CAC}}(\text{MAX.})$	$\text{t}_{\text{RCD}} + \text{t}_{\text{CAC}}(\text{MAX.})$

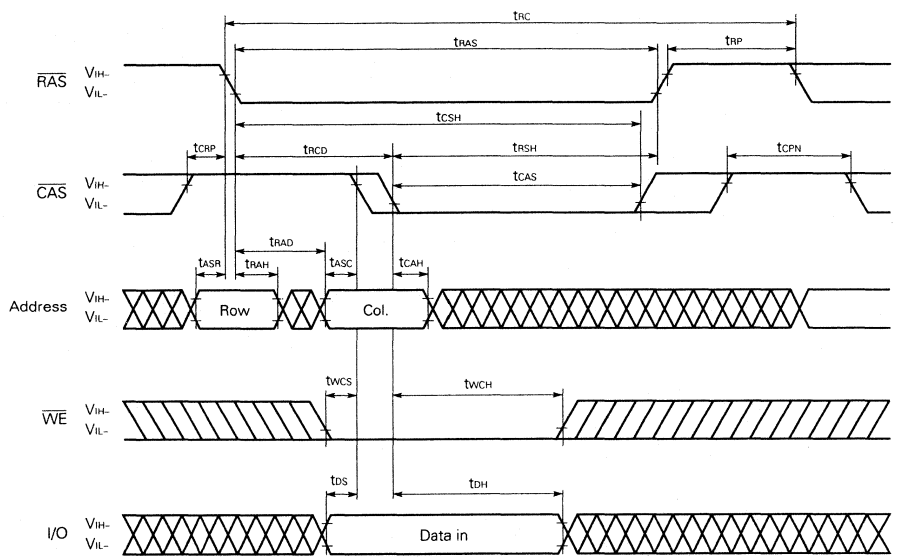
$\text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{t}_{\text{RAD}} \geq \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \geq \text{t}_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. $\text{t}_{\text{OFF}}(\text{MAX.})$ and $\text{t}_{\text{OEZ}}(\text{MAX.})$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $\text{t}_{\text{CRP}}(\text{MIN.})$ requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either $\text{t}_{\text{RCH}}(\text{MIN.})$ or $\text{t}_{\text{RRH}}(\text{MIN.})$ should be met in read cycles.
15. $\text{t}_{\text{WP}}(\text{MIN.})$ is applied to late write cycles or read modify write cycles. In early write cycles, $\text{t}_{\text{WCH}}(\text{MIN.})$ should be met.
16. $\text{t}_{\text{DS}}(\text{MIN.})$ and $\text{t}_{\text{DH}}(\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
17. If $\text{t}_{\text{WCS}} \geq \text{t}_{\text{WCS}}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{t}_{\text{RWD}} \geq \text{t}_{\text{RWD}}(\text{MIN.})$, $\text{t}_{\text{CWD}} \geq \text{t}_{\text{CWD}}(\text{MIN.})$, $\text{t}_{\text{AWD}} \geq \text{t}_{\text{AWD}}(\text{MIN.})$ and $\text{t}_{\text{CPWD}} \geq \text{t}_{\text{CPWD}}(\text{MIN.})$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Read Cycle



Early Write Cycle

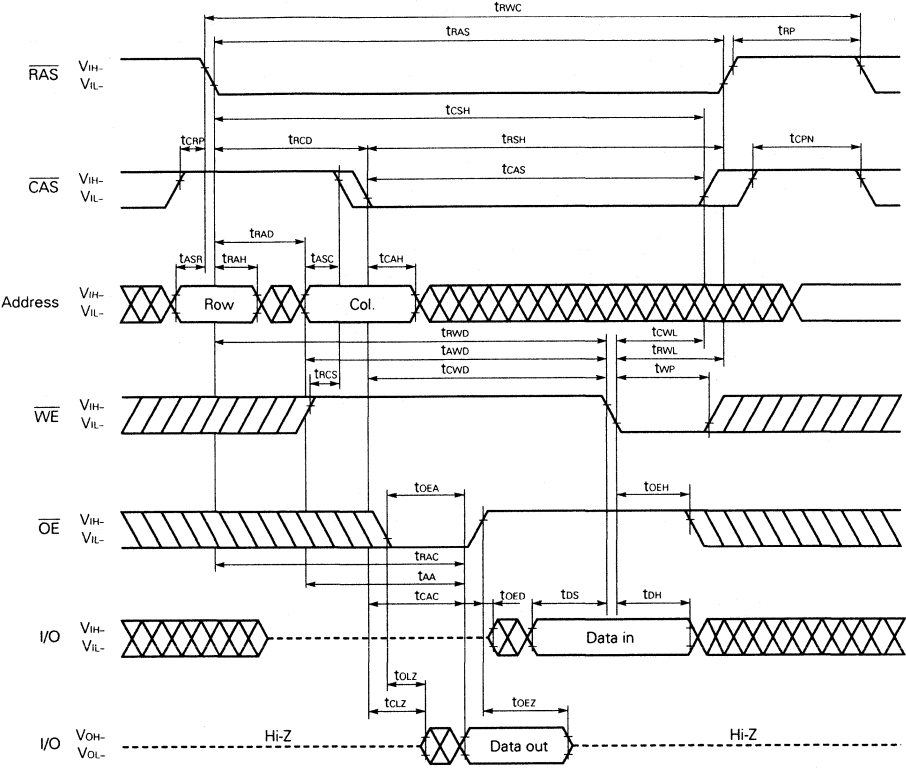


Remark $\overline{OE}$: Don't care

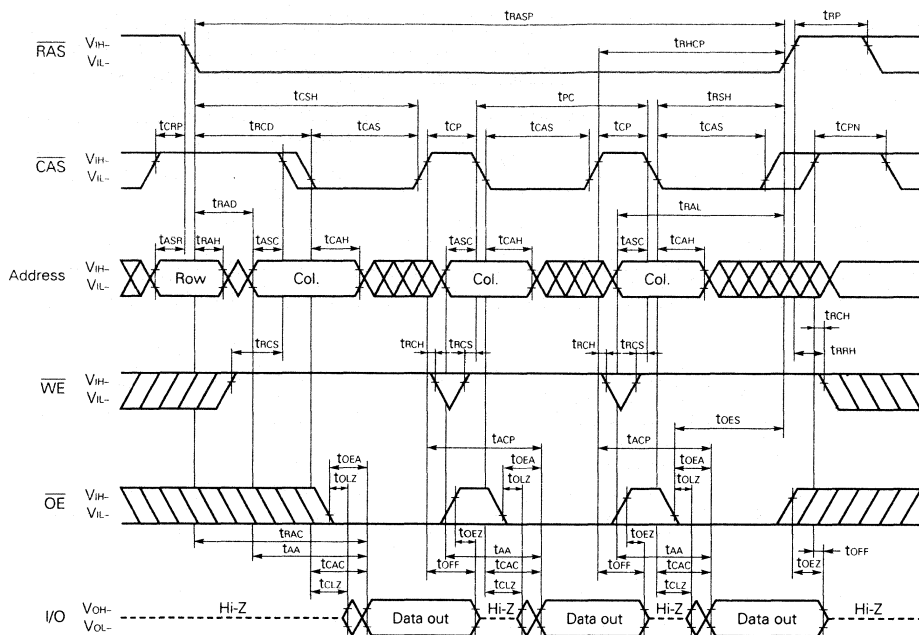
The diagram illustrates the timing relationships for a 256K16 DRAM. The signals shown are $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, and I/O. The I/O signal is shown in two states: Hi-Z (high-impedance) and Data in. The timing parameters are defined as follows:

- t_{RAS} : RAS access time (from $\overline{\text{RAS}}$ falling edge to Data in setup).
- t_{RCP} : RAS to CAS precharge time (from $\overline{\text{RAS}}$ rising edge to $\overline{\text{CAS}}$ falling edge).
- t_{CAS} : CAS access time (from $\overline{\text{CAS}}$ falling edge to Data in setup).
- t_{RAD} : Row address to Data access time (from Address Row falling edge to Data in setup).
- t_{RAH} : Row address hold time (from Address Row rising edge to Data in setup).
- t_{ASC} : Address to CAS time (from Address Col. falling edge to $\overline{\text{CAS}}$ falling edge).
- t_{CAH} : Column address hold time (from Address Col. rising edge to Data in setup).
- t_{RCD} : RAS to Data delay (from $\overline{\text{RAS}}$ falling edge to Data in setup).
- t_{RSH} : RAS to Data hold time (from $\overline{\text{RAS}}$ rising edge to Data in setup).
- t_{CAS} : CAS to Data delay (from $\overline{\text{CAS}}$ falling edge to Data in setup).
- t_{CAH} : Column address hold time (from Address Col. rising edge to Data in setup).
- t_{WE} : Write enable time (from $\overline{\text{WE}}$ falling edge to Data in setup).
- t_{OE} : Output enable time (from $\overline{\text{OE}}$ falling edge to Data in setup).
- t_{DS} : Data setup time (from Data in setup to $\overline{\text{OE}}$ falling edge).
- t_{DH} : Data hold time (from Data in setup to $\overline{\text{OE}}$ rising edge).
- t_{CPH} : CAS precharge hold time (from $\overline{\text{CAS}}$ rising edge to Data in setup).
- t_{CWL} : Column write latency (from $\overline{\text{WE}}$ falling edge to Data in setup).
- t_{RWL} : Row write latency (from $\overline{\text{WE}}$ falling edge to Data in setup).
- t_{TP} : Turnaround time (from $\overline{\text{RAS}}$ rising edge to $\overline{\text{CAS}}$ falling edge).

Read Modify Write Cycle

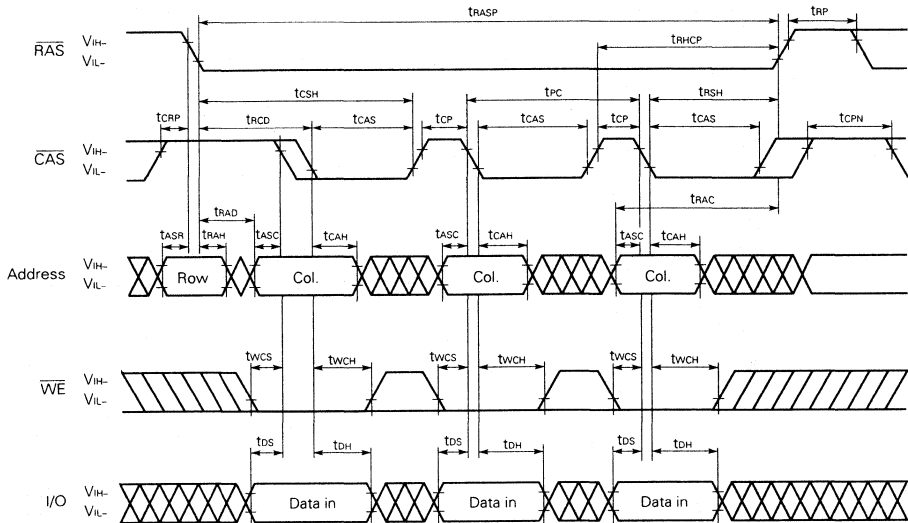


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

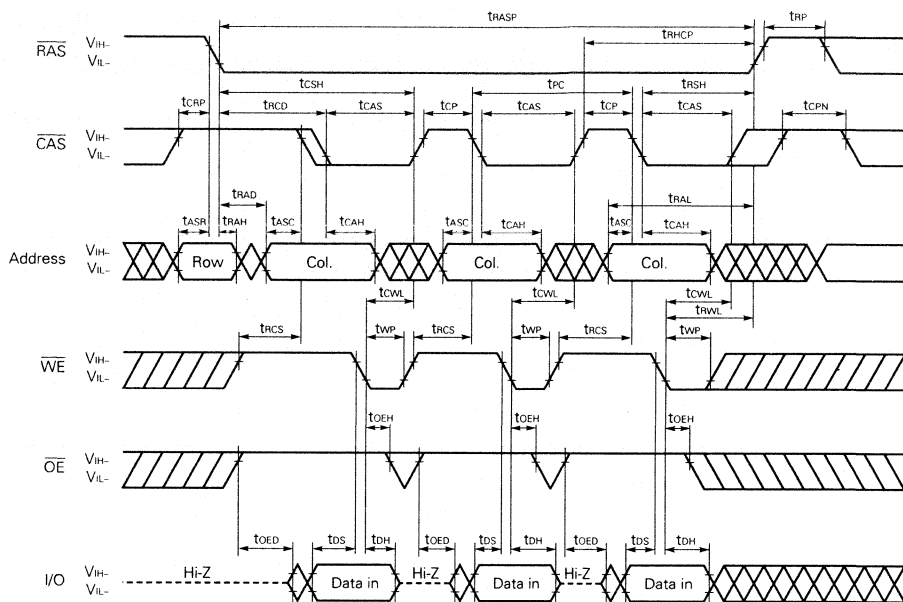
Fast Page Mode Early Write Cycle



Remark $\overline{\text{OE}}$: Don't care

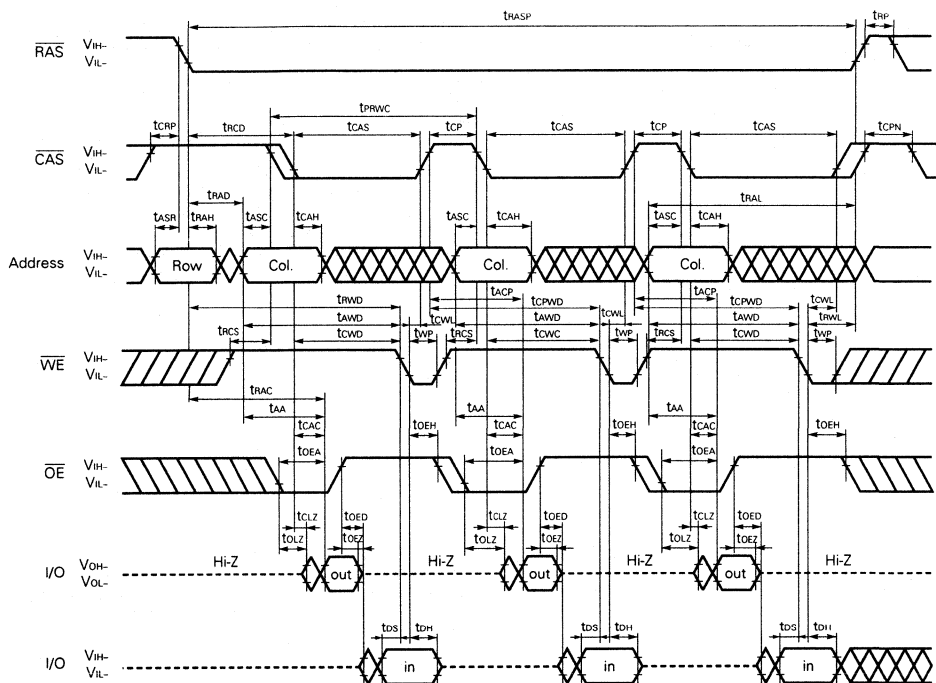
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Late Write Cycle



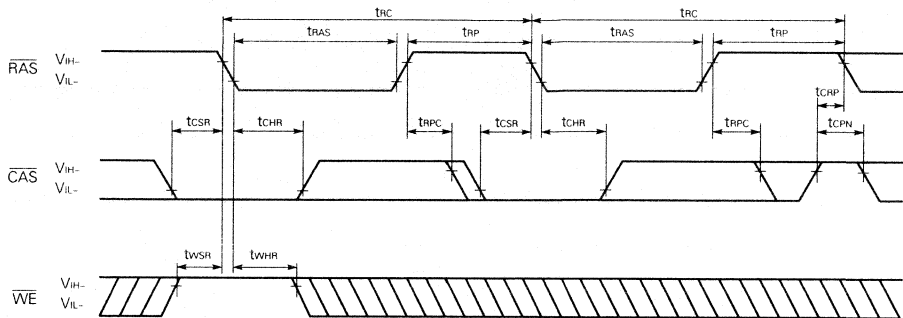
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Read Modify Write Cycle



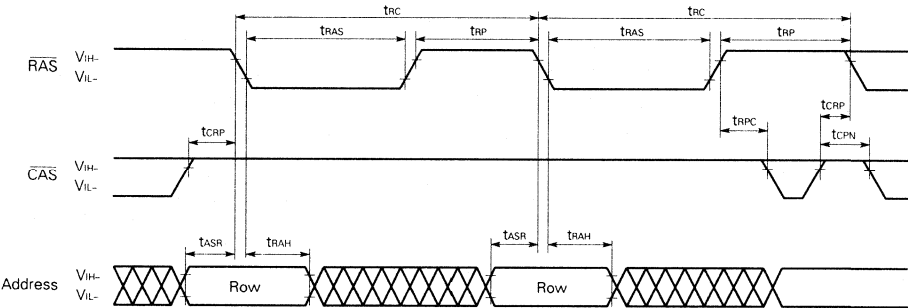
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



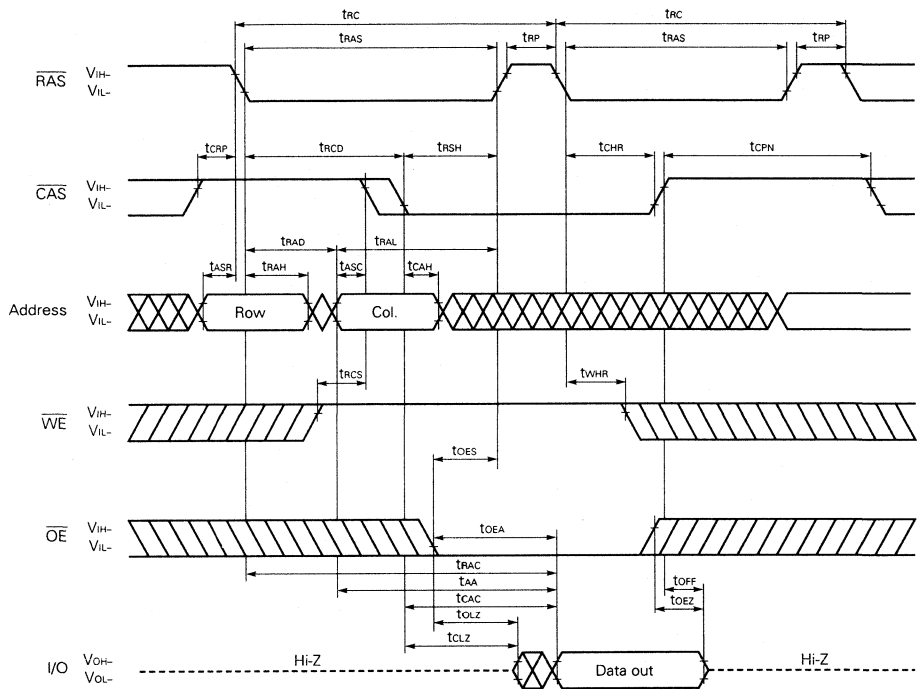
Remark Address, OE : Don't care I/O: Hi-Z

RAS Only Refresh Cycle

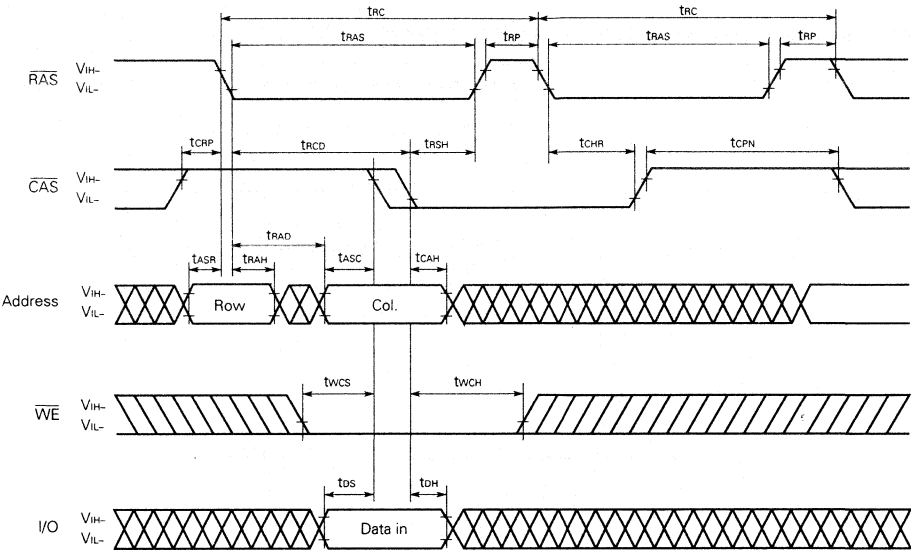


Remark WE, OE : Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



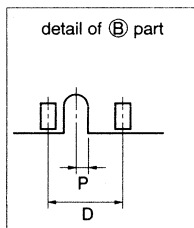
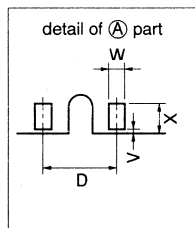
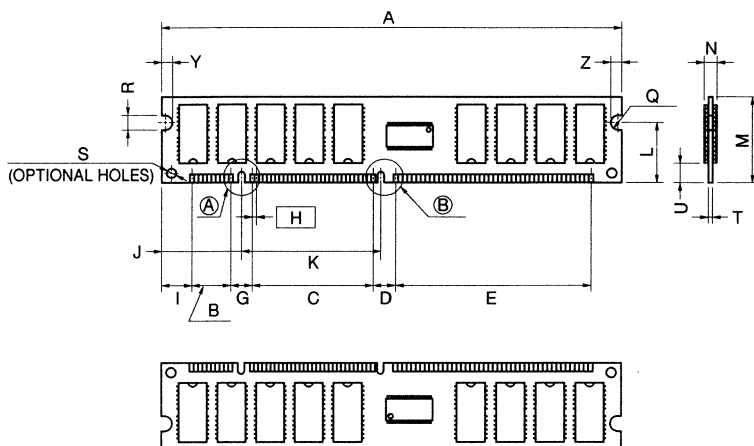
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

★ Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A2

MOS INTEGRATED CIRCUIT

MC-422000AB72F

2 M-WORD BY 72-BIT DYNAMIC RAM MODULE

FAST PAGE MODE (ECC)

Description

The MC-422000AB72F is a 2,097,152 words by 72 bits dynamic RAM module on which 9 pieces of 16 M DRAM: μ PD4217800 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 72 bits organization
- Fast access and cycle time

★

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000AB72-60	60 ns	110 ns	5.53 W	383 mW (CMOS level input)
MC-422000AB72-70	70 ns	130 ns	5.06 W	
MC-422000AB72-80	80 ns	150 ns	4.59 W	

- 2,048 refresh cycles/32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ± 0.25 V power supply

Ordering Information

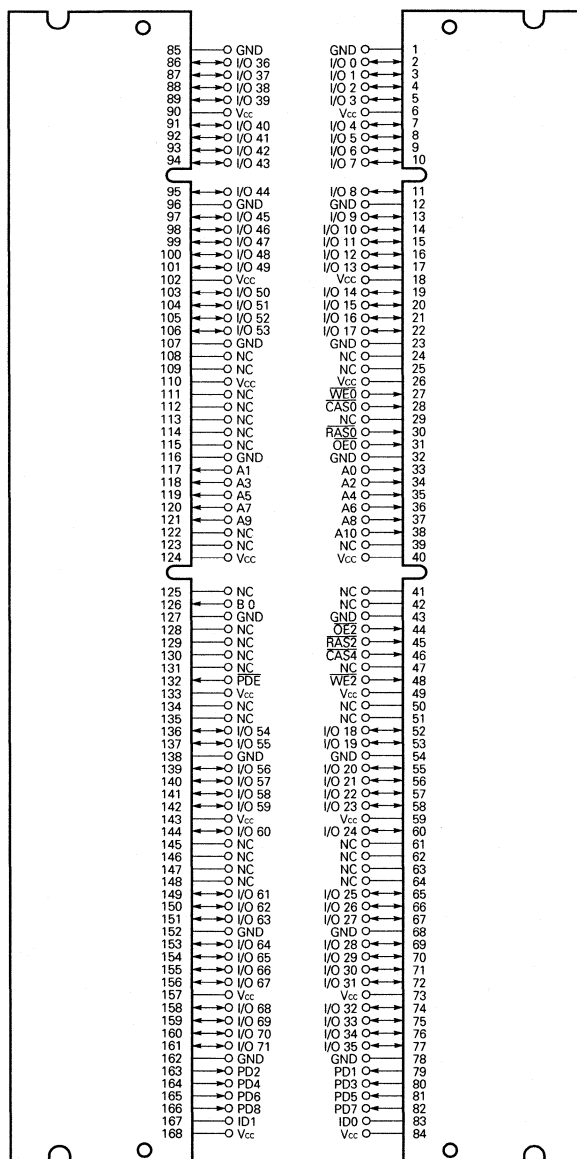
Part number	Access time (MAX.)	Package	Mounted devices
MC-422000AB72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of μ PD4217800G5 (400 mil TSOP(II)) [Double side]
MC-422000AB72F-70	70 ns		
MC-422000AB72F-80	80 ns		

The information in this document is subject to change without notice.

The mark ★ shows revised point.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



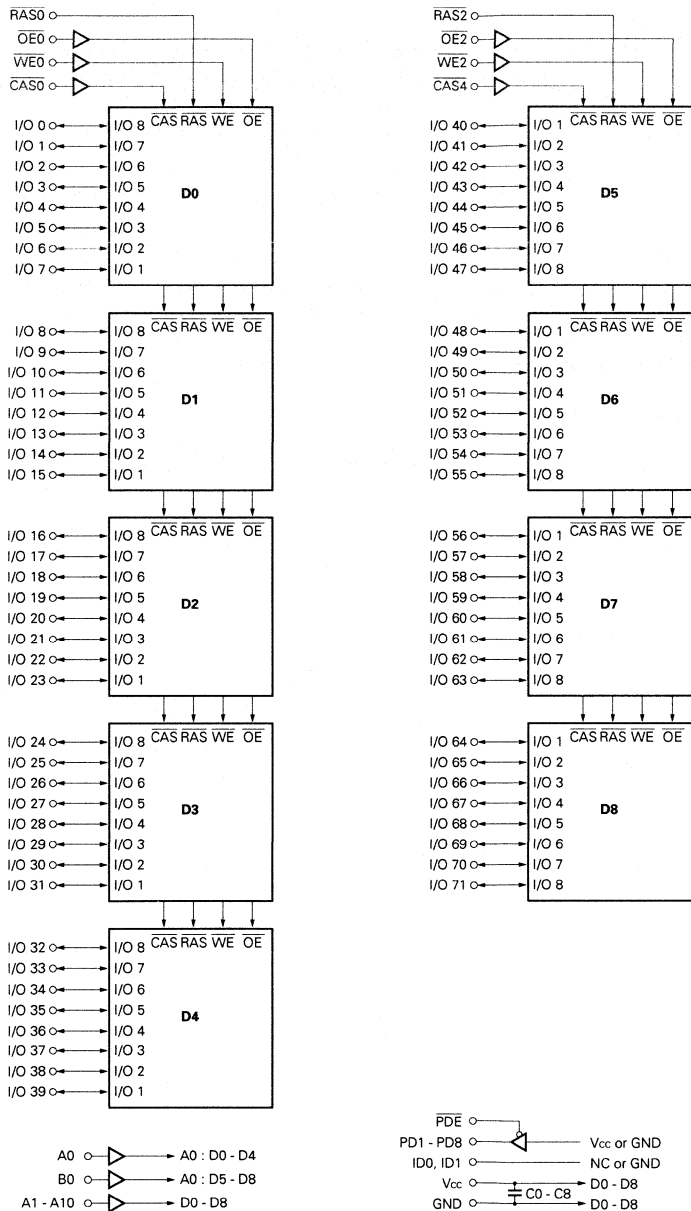
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	L	L	L
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
 I/O 0 - I/O 71 : Data Inputs/Outputs
 RAS0, RAS2 : Row Address Strobe
 CAS0, CAS4 : Column Address Strobe
 WE0, WE2 : Write Enable
 OE0, OE2 : Output Enable
 PDE : Presence Detect Enable
 PD1 - PD8 : Presence Detect Pins
 ID0, ID1 : Identity Pins
 Vcc : Power Supply
 GND : Ground
 NC : No connection

Block Diagram



Remark D0 - D8 : μ PD4217800

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		11	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			50	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

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DC Characteristics (Recommended Operating Conditions unless otherwise noted)

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Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \text{CAS Cycling}$ $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		1,054	mA	3, 4, 7
			$\text{trac} = 70 \text{ ns}$		964		
			$\text{trac} = 80 \text{ ns}$		874		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$\text{I}_\text{O} = 0 \text{ mA}$		82	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$\text{I}_\text{O} = 0 \text{ mA}$		73		
RAS only refresh current	I _{CC3}	$\overline{\text{RAS}} \text{ Cycling}$ $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		1,054	mA	3, 4, 5, 7
			$\text{trac} = 70 \text{ ns}$		964		
			$\text{trac} = 80 \text{ ns}$		874		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}} \text{ Cycling}$ $\text{tpc} = \text{tpc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		694	mA	3, 4, 6
			$\text{trac} = 70 \text{ ns}$		604		
			$\text{trac} = 80 \text{ ns}$		514		
CAS before RAS refresh current	I _{CC5}	$\overline{\text{RAS}} \text{ Cycling}$ $\text{trc} = \text{trc}(\text{MIN.})$ $\text{I}_\text{O} = 0 \text{ mA}$	$\text{trac} = 60 \text{ ns}$		1,054	mA	3, 4
			$\text{trac} = 70 \text{ ns}$		964		
			$\text{trac} = 80 \text{ ns}$		874		
Input leakage current	I _{I (IL)}	$V_{\text{I}} = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	RAS	-10	+10	μA	
			Others	-5	+1		
Output leakage current	I _{O (IL)}	$V_{\text{O}} = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)		-10	+10	μA	
High level output voltage	V _{OH}	$\text{I}_\text{O} = -5.0 \text{ mA}$		2.4		V	
Low level output voltage	V _{OL}	$\text{I}_\text{O} = +4.2 \text{ mA}$			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

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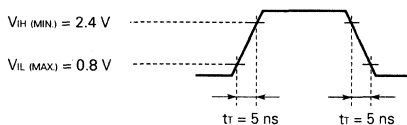
Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t _{RWC}	173		195		215		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	85		90		100		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t _{AA}		35		40		45	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		40		45		50	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEA}		15		18		20	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	13	0	15	0	15	ns	12
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	13		15		15		ns	
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OEZ}	0	13	0	15	0	15	ns	12
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0		0		0		ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15		18		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCd}	20	45	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40		45		50		ns	
Row Address Setup Time	t _{ASR}	5		5		5		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10		10		15		ns	15
$\overline{\text{WE}}$ Pulse Width	t _{WP}	10		10		15		ns	15

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	10		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
CAS to WE Delay Time	t _{CWD}	38		43		45		ns	17
RAS to WE Delay Time	t _{RWD}	93		105		115		ns	17
CAS Precharge to WE Delay Time	t _{CPWD}	58		65		70		ns	17
Column Address to WE Delay Time	t _{AWD}	58		65		70		ns	17
WE Lead Time Referenced to RAS	t _{RWL}	25		25		25		ns	
WE Lead Time Referenced to CAS	t _{CWL}	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	t _{CSR}	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10		10		10		ns	
WE Setup Time	t _{WSR}	10		10		10		ns	
WE Hold Time	t _{WHR}	15		15		15		ns	
Refresh Time	t _{REF}		32		32		32	ms	

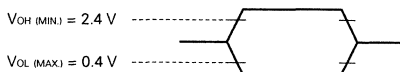
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{IL}$ (MAX.) and $\overline{\text{CAS}} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_r = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



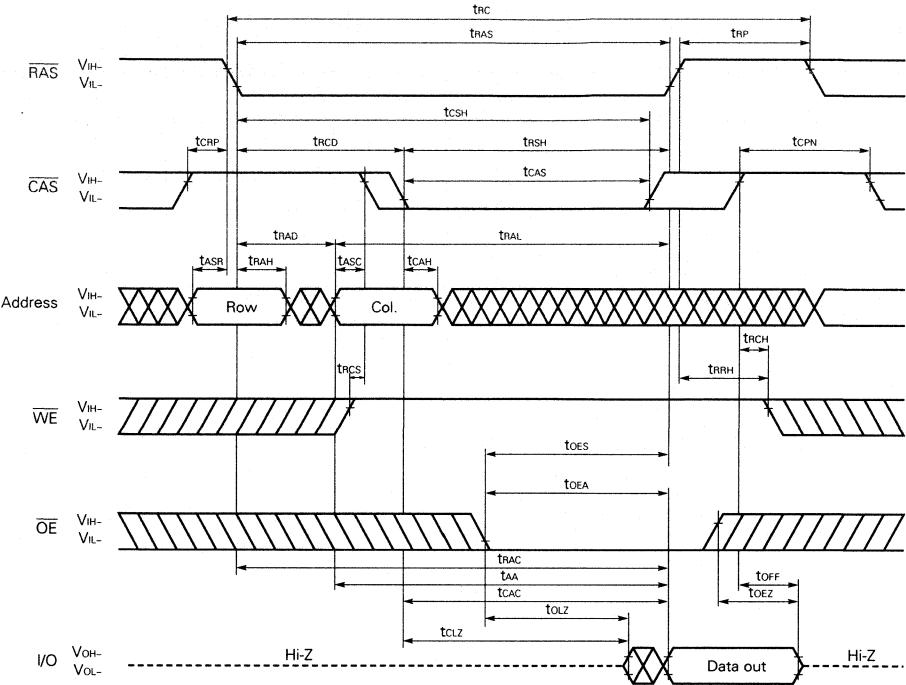
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)	$\text{trAD} + \text{tAA (MAX.)}$
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)	$\text{trCD} + \text{tCAC (MAX.)}$

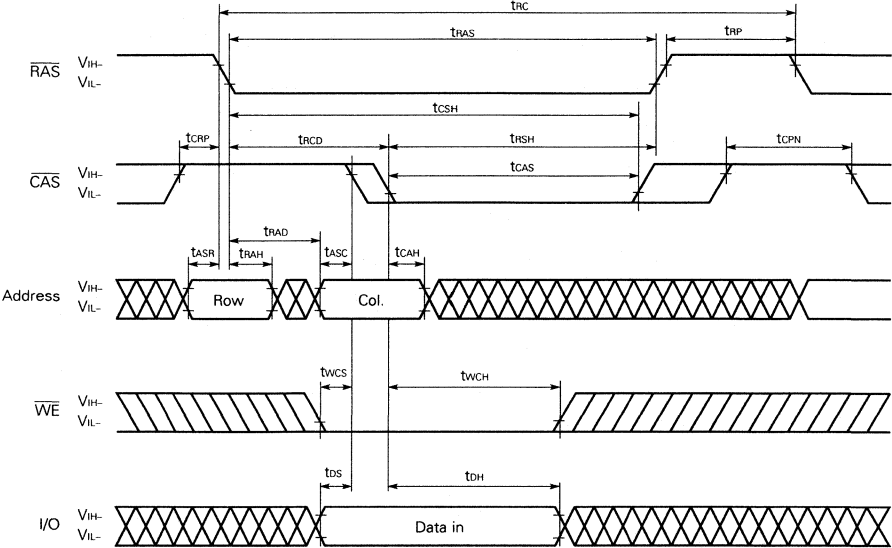
trAD (MAX.) and trCD (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD (MAX.)}$ and $\text{trCD} \geq \text{trCD (MAX.)}$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. tOFF (MAX.) and tOEZ (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to VoH or VoL .
13. tCRP (MIN.) requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either trCH (MIN.) or trRH (MIN.) should be met in read cycles.
15. tWP (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twCH (MIN.) should be met.
16. tDS (MIN.) and tDH (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
17. If $\text{twCS} \geq \text{twCS (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{trWD} \geq \text{trWD (MIN.)}$, $\text{tcWD} \geq \text{tcWD (MIN.)}$, $\text{tAWD} \geq \text{tAWD (MIN.)}$ and $\text{tcpWD} \geq \text{tcpWD (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Read Cycle

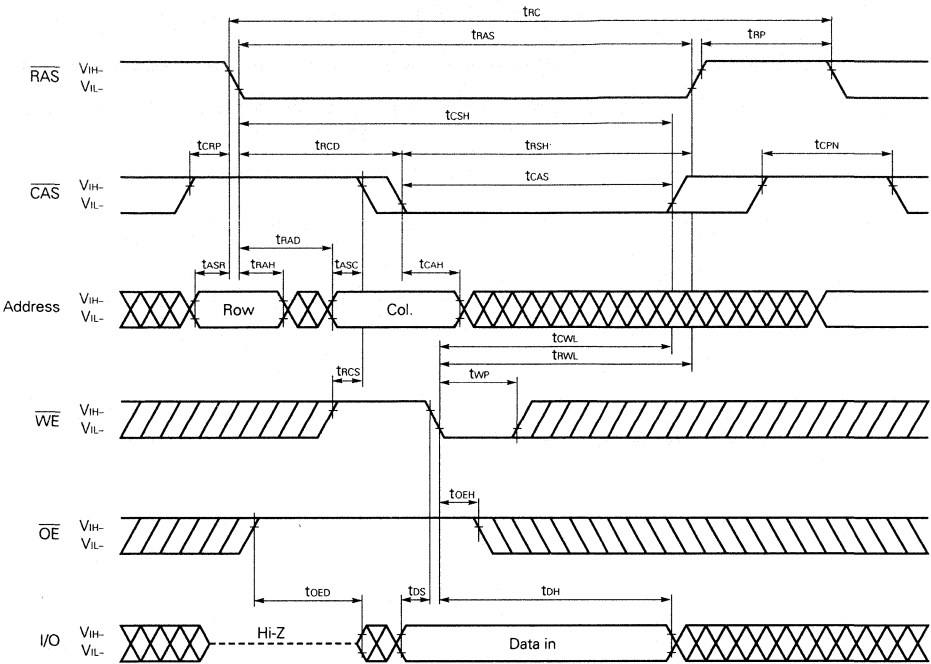


Early Write Cycle

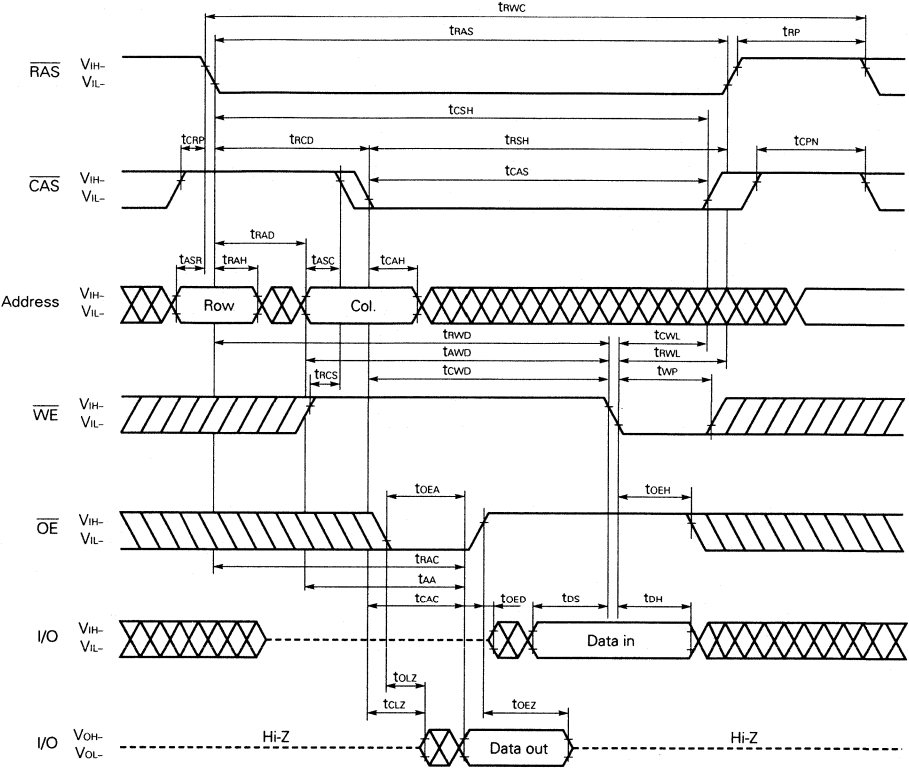


Remark $\overline{OE}$: Don't care

Late Write Cycle



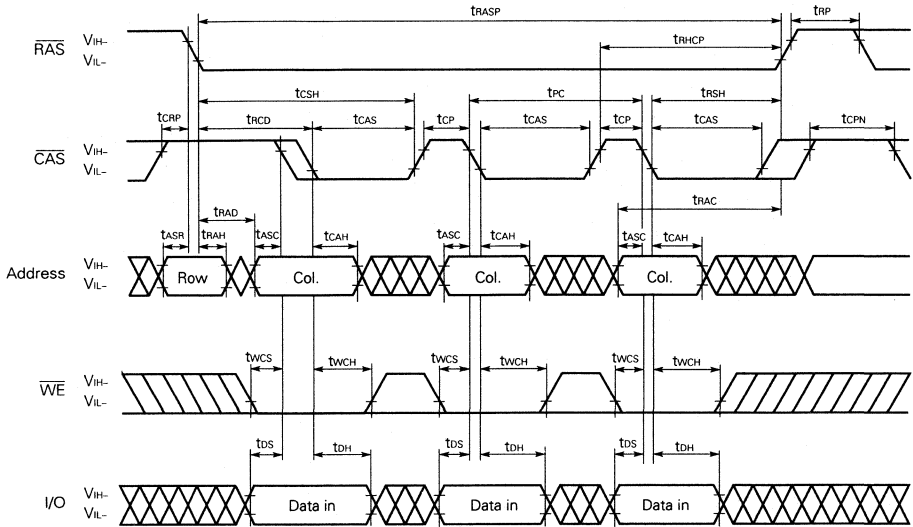
Read Modify Write Cycle



[illegible]

1329

Fast Page Mode Early Write Cycle



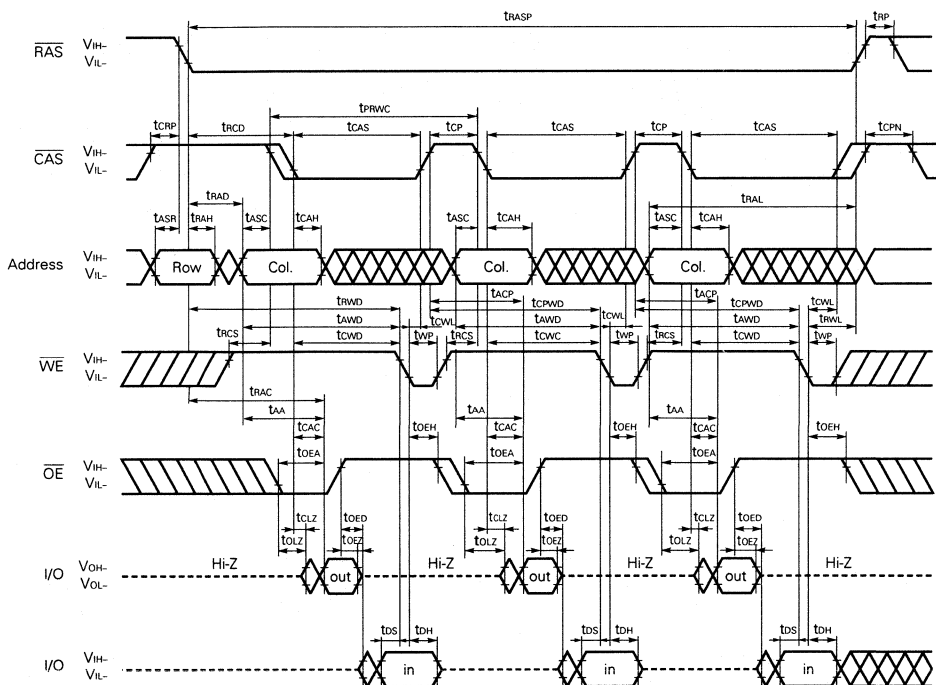
Remarks 1. $\overline{\text{OE}}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

[illegible]

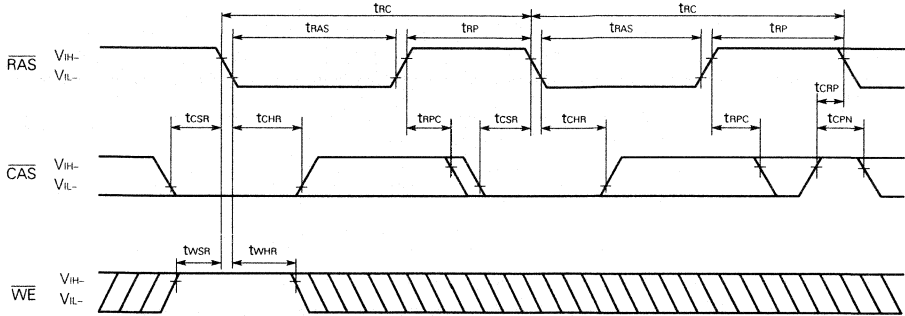
1331

Fast Page Mode Read Modify Write Cycle



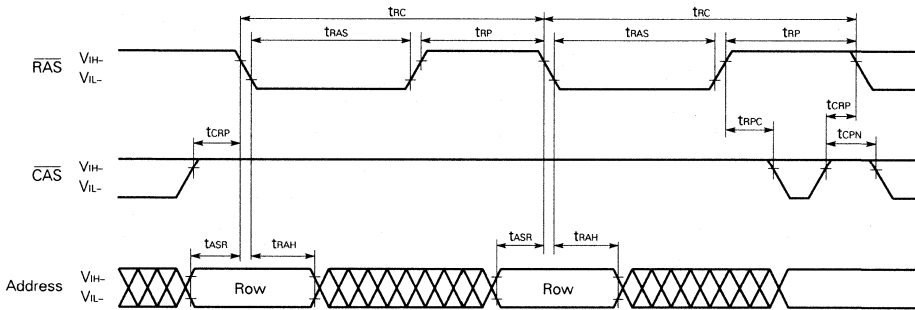
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



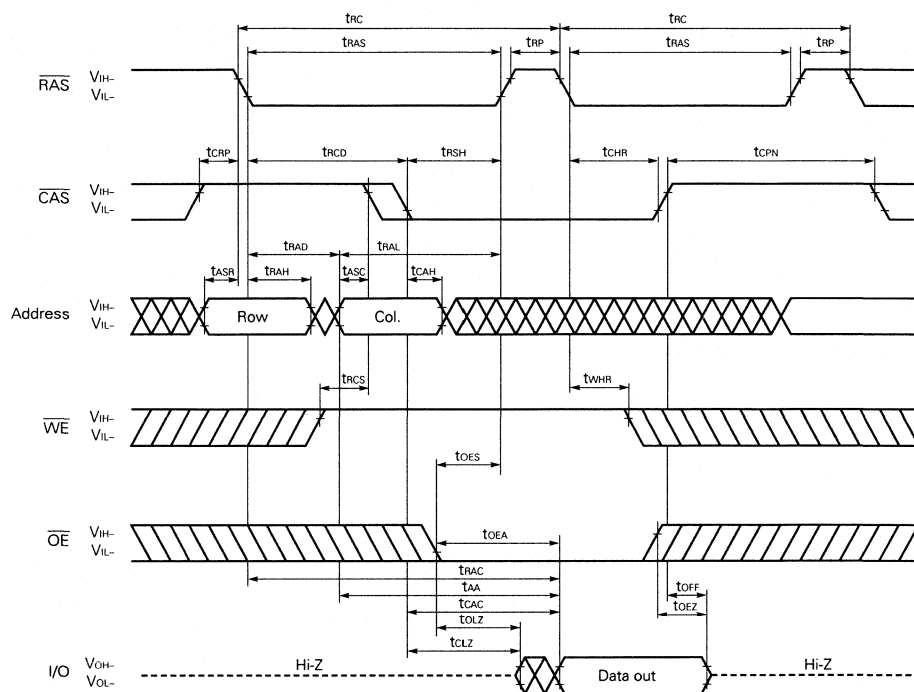
Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

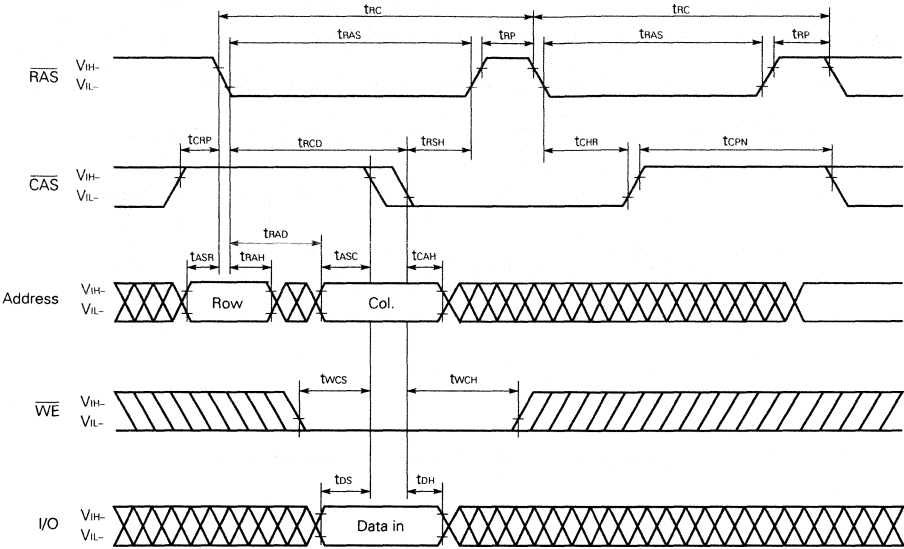


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



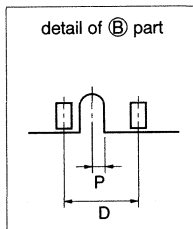
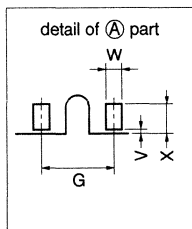
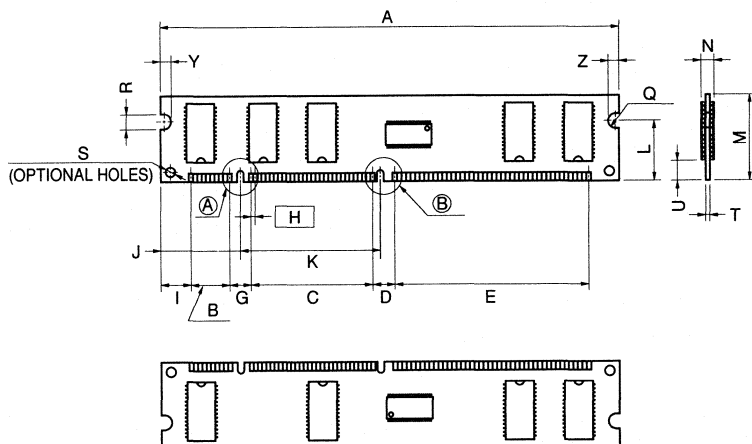
Hidden Refresh Cycle (Write)



Remark $\overline{\text{OE}}$: Don't care

★ Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039 ^{+0.003} _{-0.002}
X	2.54	0.100
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A6

1M -WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-421000AD72F is a 1 048 576 words by 72 bits dynamic RAM module on which 4 pieces of 16M DRAM (μ PD 4218160) and 2 pieces of 4M DRAM (μ PD424400) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1 048 576 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC- 421000AD72-60	60ns	110ns	4.96 w	339 mw (CMOS level)
MC- 421000AD72-70	70ns	130ns	4.54 w	
MC- 421000AD72-80	80ns	150ns	4.22 w	

- 1 024 refresh cycles/16 ms
- CAS before RAS refresh , RAS only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +5.0V $\pm$ 0.25V power supply

The information in this document is subject to change without notice.

Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 421000AD72F-60	60ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of uPD4218160G5 (400mil TSOP)
MC- 421000AD72F-70	70ns		and 2 pieces of uPD424400G3 (300mil TSOP)
MC- 421000AD72F-80	80ns		[Double side]

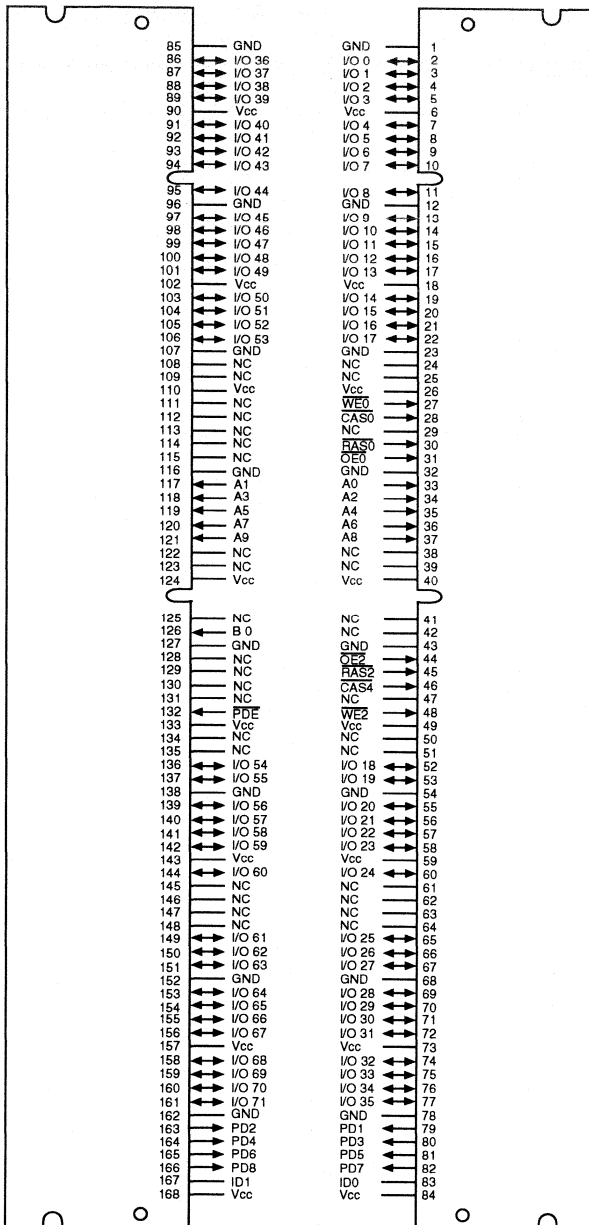
Quality grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



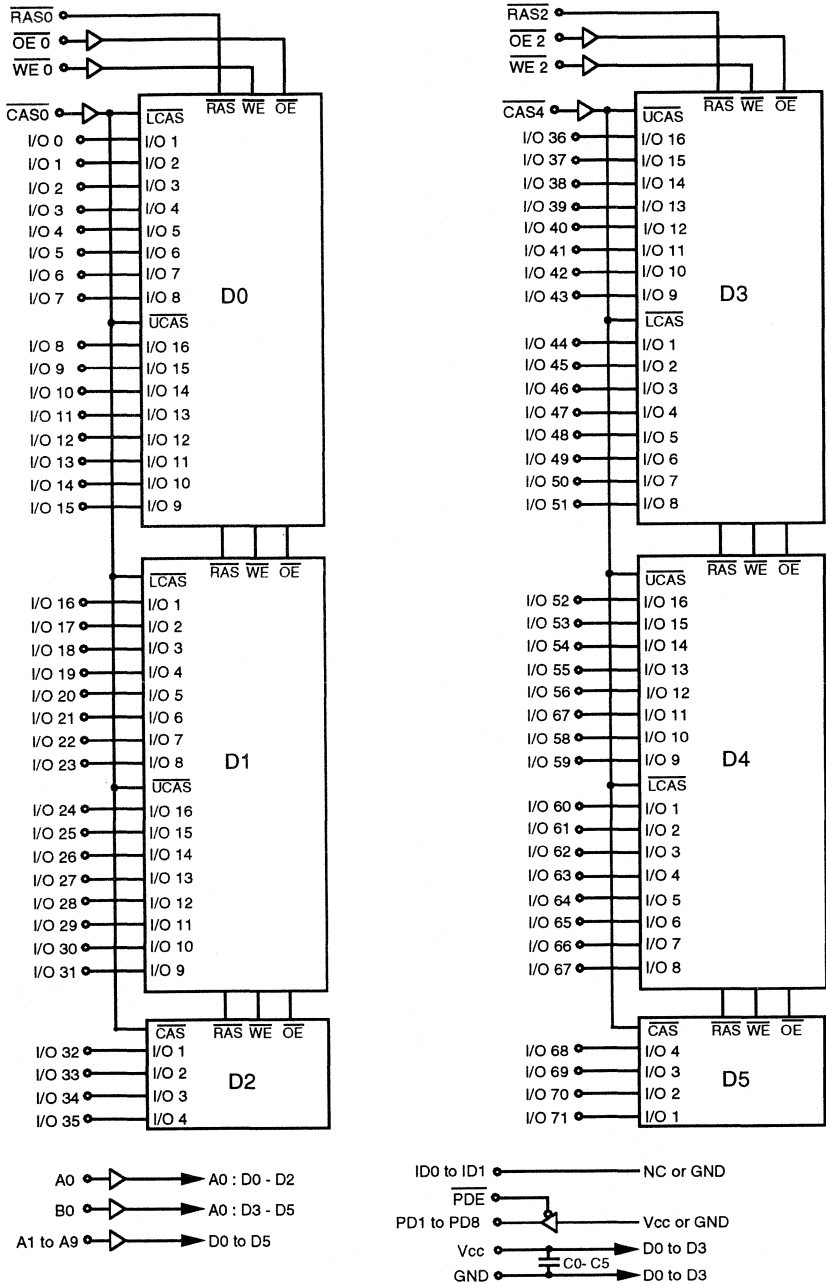
PD and ID Table

Pin Name	Pin No.	Access Time		
		60ns	70ns	80ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Note) H : VOH, L : VOL

A0 - A9, B0 : Address Inputs
 I/O 0-I/O 71 : Data Inputs / Outputs
 RAS0, RAS2 : Row Address Strobe
 CAS0, CAS4 : Column Address Strobe
 WE0, WE2 : Write Enable
 OE0, OE2 : Output Enable
 PDE : Presence Detect Enable
 PD1- PD8 : Presence Detect Pins
 ID0, ID1 : Identity pins
 Vcc : Power Supply
 GND : Ground
 NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0 to +7.0	V
Supply voltage	VCC		-1.0 to +7.0	V
Output current	IO		50	mA
Power dissipation	PD		8	W
Operating temperature	T _{opt}		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES : 1, 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		4.75	5.0	5.25	V
High level input voltage	VIH		2.4		V _{CC} + 1.0	V
Low level input voltage	VIL		-1.0		+0.8	V
Ambient temperature	T _a		0		70	°C

CAPACITANCE (T_a=25°C , f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C I 1	A0 - A10, B0			20	pF
	C I 2	$\overline{\text{WE}} 0, \overline{\text{WE}} 2$			20	pF
	C I 3	$\overline{\text{RAS}} 0, \overline{\text{RAS}} 2$			36	pF
	C I 4	$\overline{\text{CAS}} 0, \overline{\text{CAS}} 4$			20	pF
	C I 5	$\overline{\text{OE}} 0, \overline{\text{OE}} 2$			20	pF
Data Input/ Output capacitance	C I/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	I _{cc1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}}=t_{\text{RC}}(\text{MIN.}), \text{IO}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		944	mA	3,4,7
			$t_{\text{RAC}}=70\text{ns}$		864		
			$t_{\text{RAC}}=80\text{ns}$		804		
Standby Current	I _{cc2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$			76	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}}-0.2\text{V}$			70		
$\overline{\text{RAS}}$ only refresh current	I _{cc3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}$ $t_{\text{RC}}=t_{\text{RC}}(\text{MIN.}), \text{IO}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		944	mA	3,4,5,7
			$t_{\text{RAC}}=70\text{ns}$		864		
			$t_{\text{RAC}}=80\text{ns}$		804		
Operating Current (Fast Page Mode)	I _{cc4}	$\overline{\text{RAS}} \leq V_{\text{IL}}, \overline{\text{CAS}}$ Cycling $t_{\text{PC}}=t_{\text{PC}}(\text{MIN.}), \text{IO}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		604	mA	3,4,6
			$t_{\text{RAC}}=70\text{ns}$		544		
			$t_{\text{RAC}}=80\text{ns}$		484		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{cc5}	$t_{\text{RC}}=t_{\text{RC}}(\text{MIN.})$ $\text{IO}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		944	mA	3,4
			$t_{\text{RAC}}=70\text{ns}$		864		
			$t_{\text{RAC}}=80\text{ns}$		804		
Input Leakage Current	I _{I(L)}	V _I =0 to 5.5V all other pins not under test = 0V	$\overline{\text{RAS}}$	-10	+10	μA	
			others	-5	+1		
Output Leakage Current	I _{O(L)}	Outputs are disabled (Hi - Z) V _O =0 to 5.5V		-10	+10	μA	
High level output voltage	V _{OH}	I _O =-5mA		2.4		V	
Low level output voltage	V _{OL}	I _O =+4.2mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

PARAMETER	SYMBOL	t _{RAC} = 60ns		t _{RAC} = 70ns		t _{RAC} = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	110	-	130	-	160	-	ns	
Read Modify Write Cycle Time	t _{RWC}	173	-	195	-	225	-	ns	
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40	-	45	-	50	-	ns	
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	85	-	90	-	105	-	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	-	60	-	70	-	80	ns	10,11
Access Time from $\overline{\text{CAS}}$	t _{CAC}	-	20	-	25	-	25	ns	10,11
Access Time from Column Address	t _{AA}	-	35	-	40	-	45	ns	10,11
Access Time from CAS Precharge	t _{ACP}	-	40	-	45	-	50	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEa}	-	15	-	20	-	20	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0	-	0	-	0	-	ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0	-	0	-	0	-	ns	11
Output Buffer Turn-off Delay Time($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	15	-	15	-	20	-	ns	
Output Buffer Turn-off Delay Time($\overline{\text{OE}}$)	t _{OEZ}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ Command Hold Time	t _{OEh}	0	-	0	-	0	-	ns	
$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ inactive Setup Time	t _{OES}	0	-	0	-	0	-	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	-	50	-	70	-	ns	
$\overline{\text{RAS}}$ Pulse Width(Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	-	20	-	20	-	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10 000	20	10 000	20	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60	-	70	-	80	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	45	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10	-	10	-	10	-	ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10	-	10	-	10	-	ns	
$\overline{\text{CAS}}$ Precharge Time(Fast Page Mode)	t _{CP}	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40	-	45	-	50	-	ns	
Row Address Set Up Time	t _{ASR}	5	-	5	-	5	-	ns	
Row Address Hold Time	t _{RAH}	10	-	10	-	12	-	ns	
Column Address Set Up Time	t _{ASC}	0	-	0	-	0	-	ns	
Column Address Hold Time	t _{CAH}	15	-	15	-	15	-	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30	-	35	-	40	-	ns	
Lead Command Setup Time	t _{RCS}	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0	-	0	-	10	-	ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0	-	0	-	0	-	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15	-	15	-	15	-	ns	15

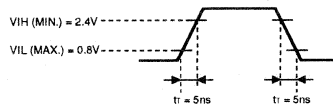
(2/2)

PARAMETER	SYMBOL	trAC = 60ns		trAC = 70ns		trAC = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Comand Set-Up Time	tWP	10	-	10	-	15	-	ms	15
Data-in Seup Time	tDS	0	-	0	-	0	-	ns	16
Data-in Hold Time	tDH	10	-	15	-	15	-	ns	16
Write Comand Setup Time	tWCS	0	-	0	-	0	-	ns	17
CAS to WE Delay Time	tCWD	38	-	40	-	45	-	ns	17
RAS to WE Delay Time	tRWD	93	-	105	-	115	-	ns	17
CAS Precharge Delay Time Referenced to WE (Fast Page Mode)	tCPWD	60	-	65	-	70	-	ns	17
Column Address Delay Time Referenced to WE	tAWD	58	-	65	-	70	-	ns	17
Write Command Lead Time Referenced to RAS	tRWL	25	-	25	-	25	-	ns	
Write Command Lead Time Referenced to CAS	tCWL	15	-	15	-	15	-	ns	
CAS Setup Time for CAS before RAS Refresh	tCSR	10	-	10	-	10	-	ns	
CAS Hold Time for CAS before RAS Refresh	tCHR	10	-	10	-	10	-	ns	
WE Setup Time	tWSR	10	-	10	-	10	-	ns	
WE Hold Time	tWHR	15	-	15	-	15	-	ns	
Refresh Time	tREF	-	16	-	16	-	16	ms	

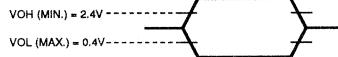
Notes:

1. All voltages are referenced to GND .
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. t_{CC1} , t_{CC3} , t_{CC4} and t_{CC5} depend on cycle rates (t_{RC} and t_{PC}) .
4. Specified values are obtained with outputs unloaded.
5. t_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. t_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. t_{CC1} and t_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{IL(\text{MAX})}$ and $\overline{\text{CAS}} \geq V_{IH(\text{MIN})}$.
8. AC measurements assume $t_r = 5\text{ns}$.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



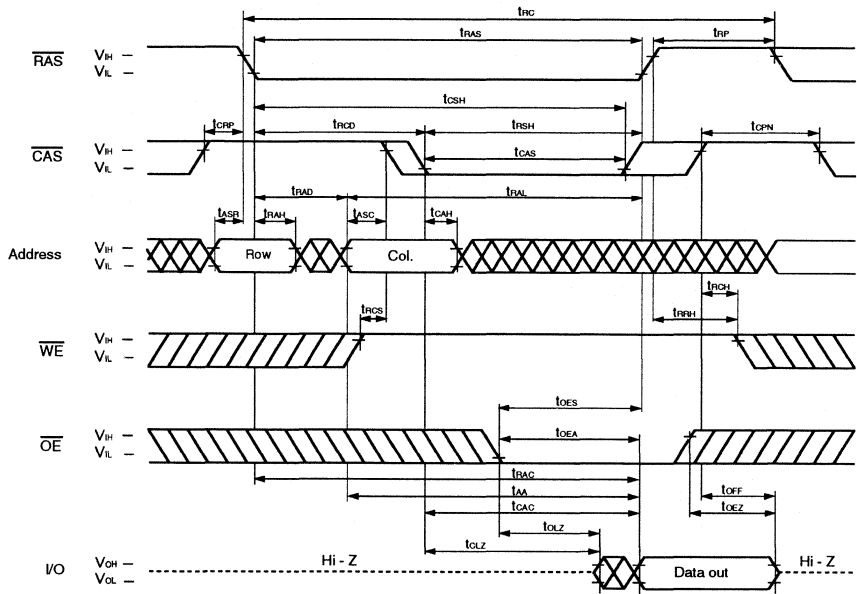
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \leq t_{\text{RCD}(\text{MAX})}$	$t_{\text{RAC}(\text{MAX})}$	$t_{\text{RAC}(\text{MAX})}$
$t_{\text{RAD}} > t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \leq t_{\text{RCD}(\text{MAX})}$	$t_{\text{AA}(\text{MAX})}$	$t_{\text{RAD}} + t_{\text{AA}(\text{MAX})}$
$t_{\text{RCD}} > t_{\text{RCD}(\text{MAX})}$	$t_{\text{CAC}(\text{MAX})}$	$t_{\text{RCD}} + t_{\text{CAC}(\text{MAX})}$

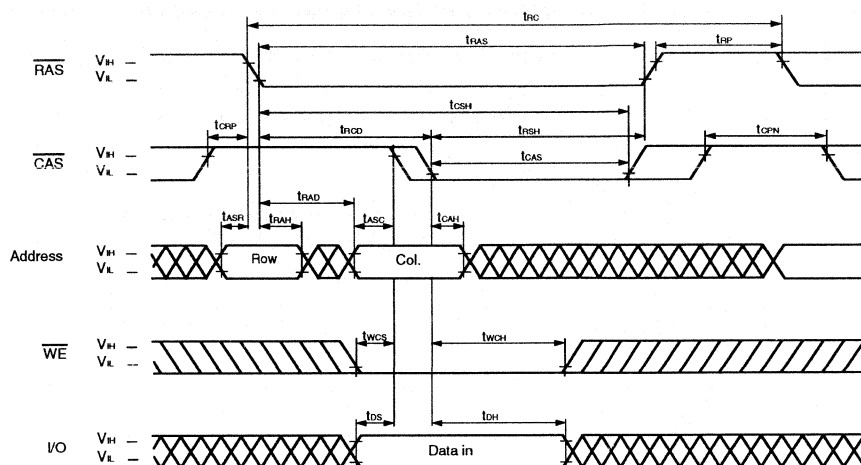
$t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}(\text{MAX})}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \geq t_{\text{RCD}(\text{MAX})}$ will not cause any operation problems.

11. Loading conditions are 1 TTLs and 100 pF.
12. $t_{\text{OFF}(\text{MAX})}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $t_{\text{CRP}(\text{MIN})}$ requirement should be applied to $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycles.
14. Either $t_{\text{ROH}(\text{MIN})}$ or $t_{\text{RRH}(\text{MIN})}$ should be met in read cycles.
15. $t_{\text{WP}(\text{MIN})}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{\text{WCH}(\text{MIN})}$ should be met.
16. $t_{\text{DS}(\text{MIN})}$ and $t_{\text{DH}(\text{MIN})}$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
17. If $t_{\text{WCS}} \geq t_{\text{WCS}(\text{MIN})}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle . If $t_{\text{RWD}} \geq t_{\text{RWD}(\text{MIN})}$, $t_{\text{CWD}} \geq t_{\text{CWD}(\text{MIN})}$, $t_{\text{AWD}} \geq t_{\text{AWD}(\text{MIN})}$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}(\text{MIN})}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Read Cycle

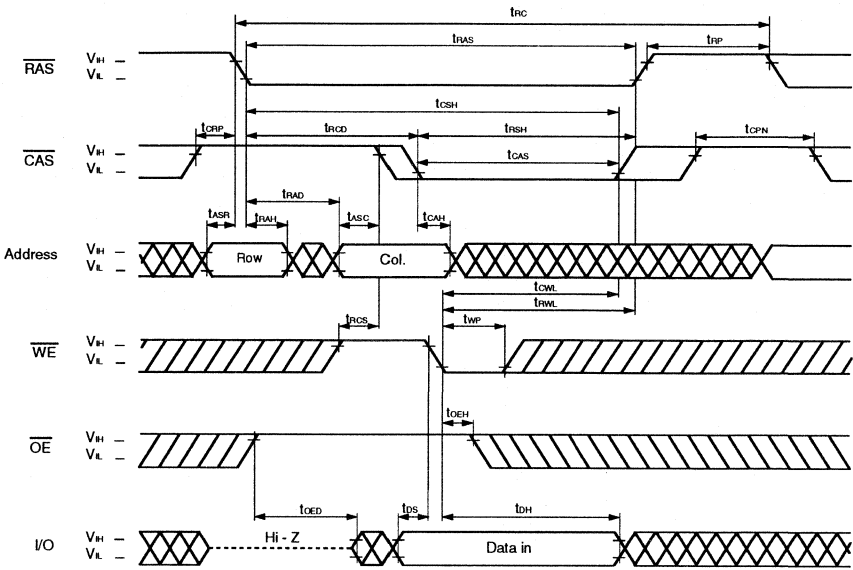


Early Write Cycle

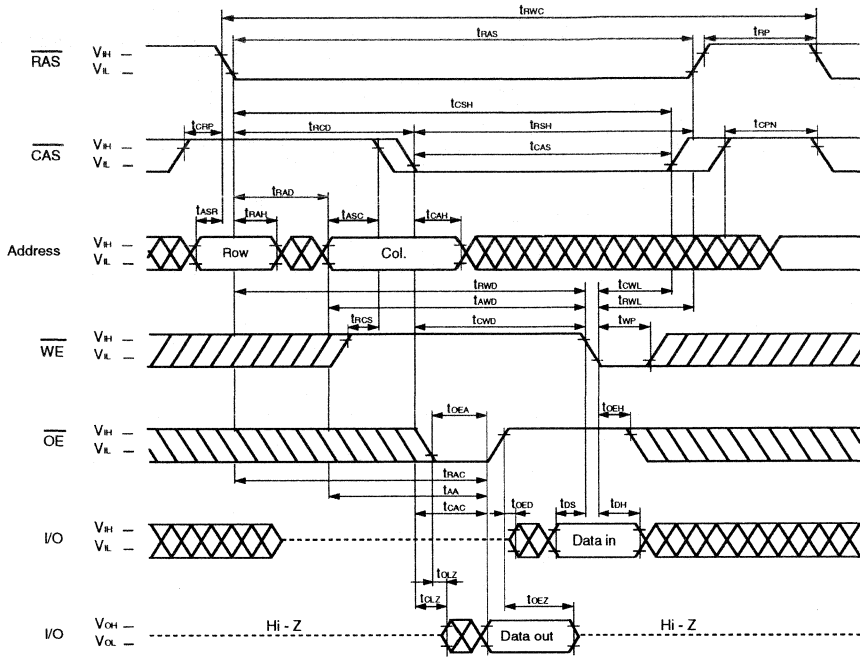


Remark $\overline{OE}$: Don't care

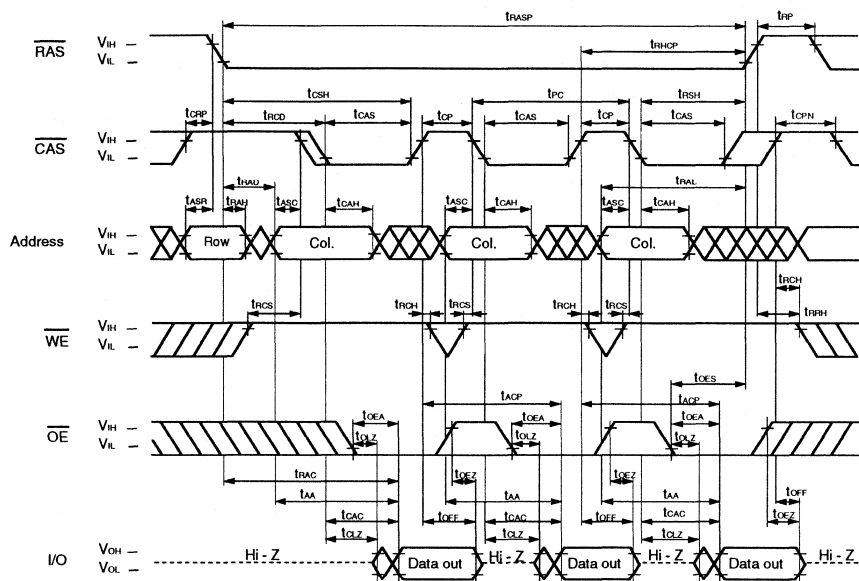
Late Write Cycle



Read Modify Write Cycle

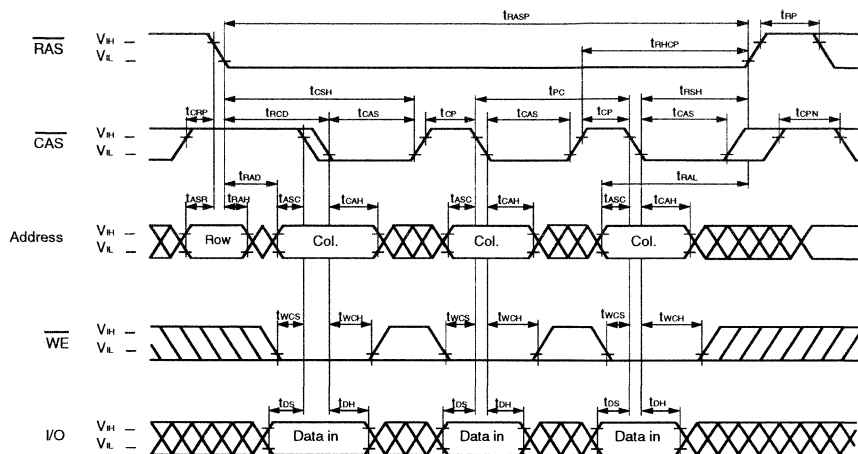


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

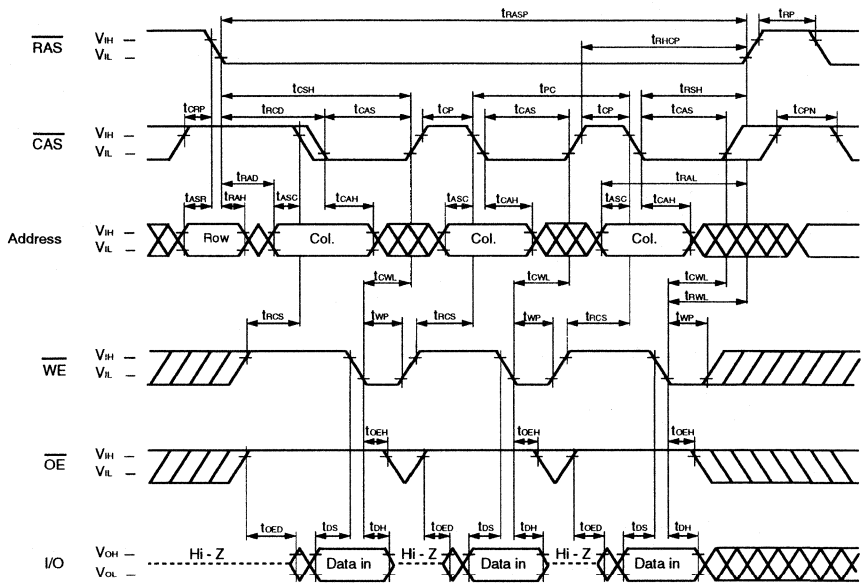
Fast Page Mode Early Write Cycle



Remark $\overline{OE}$: Don't care

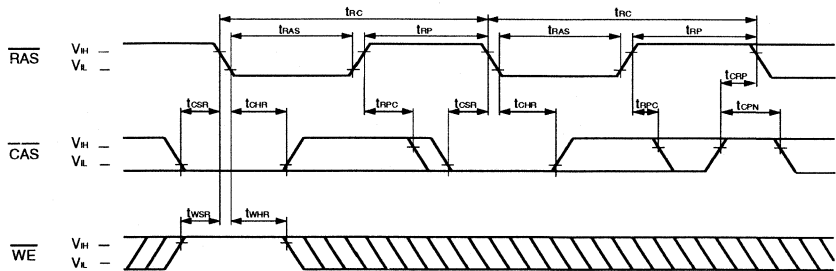
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Late Write Cycle



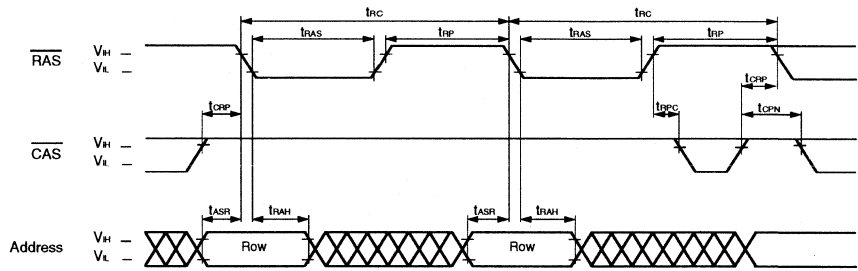
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

CAS Before RAS Refresh Cycle



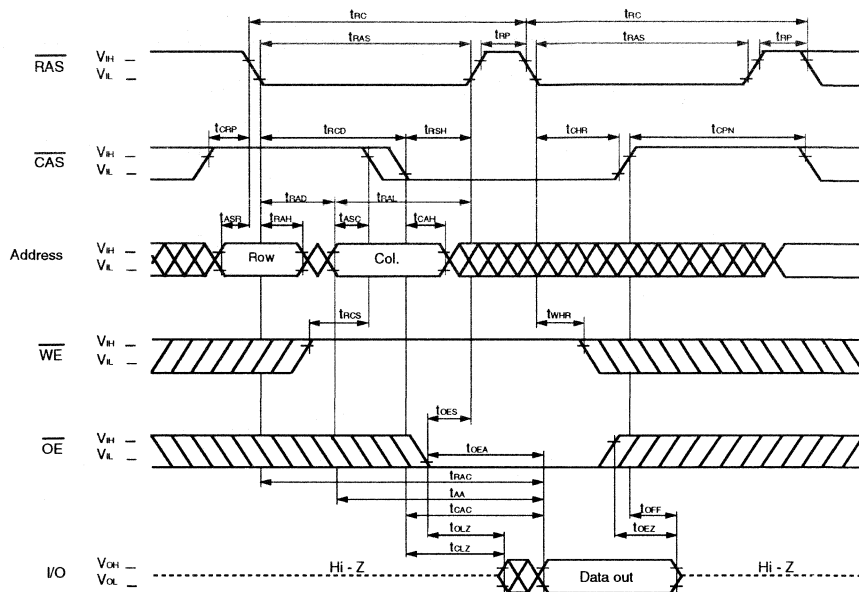
Remark Address, $\overline{OE}$: Don't care I/O : Hi - Z

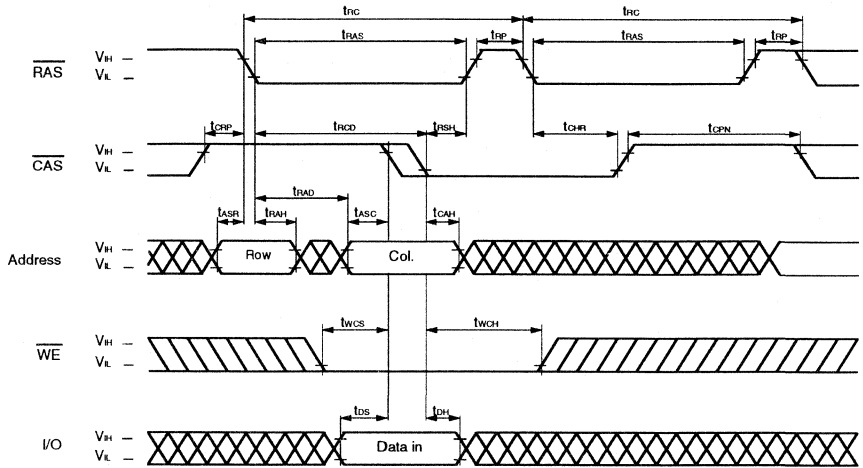
RAS Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi - Z

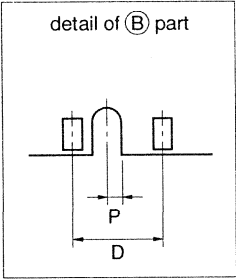
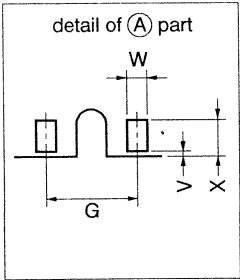
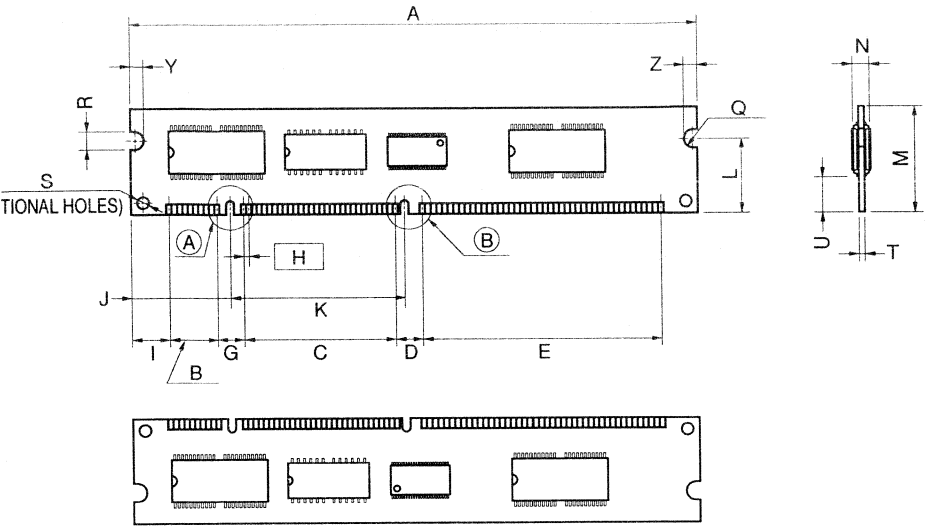
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

Remark OE : Don't care

Package Drawing



ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R 2.0	R 0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54	0.100
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A4

MOS INTEGRATED CIRCUIT

MC-421000AA64FA

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000AA64FA is a 1,048,576 words by 64 bits dynamic RAM module on which 16 pieces of 4 M DRAM: μ PD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 64 bits organization
- Fast access and cycle time

★

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000AA64-60	60 ns	110 ns	10.42 W	420 mW (CMOS level input)
MC-421000AA64-70	70 ns	130 ns	8.74 W	
MC-421000AA64-80	80 ns	150 ns	7.90 W	

- 1,024 refresh cycles/16 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ± 0.25 V power supply

The information in this document is subject to change without notice.

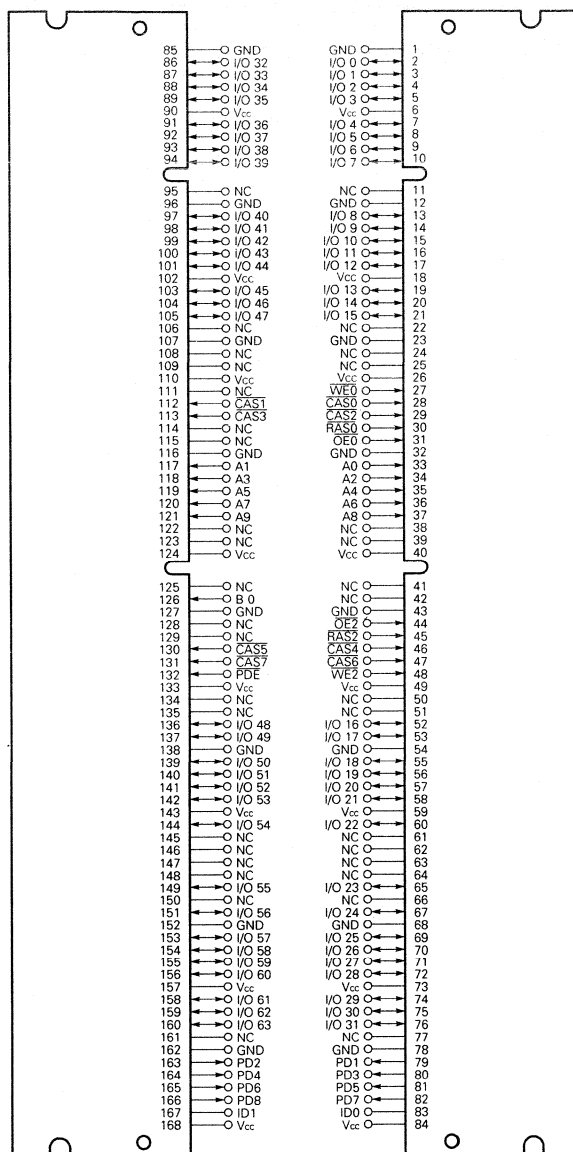
The mark ★ shows revised points.

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000AA64FA-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	16 pieces of μ PD424400LA (300 mil SOJ) [Double side]
MC-421000AA64FA-70	70 ns		
MC-421000AA64FA-80	80 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



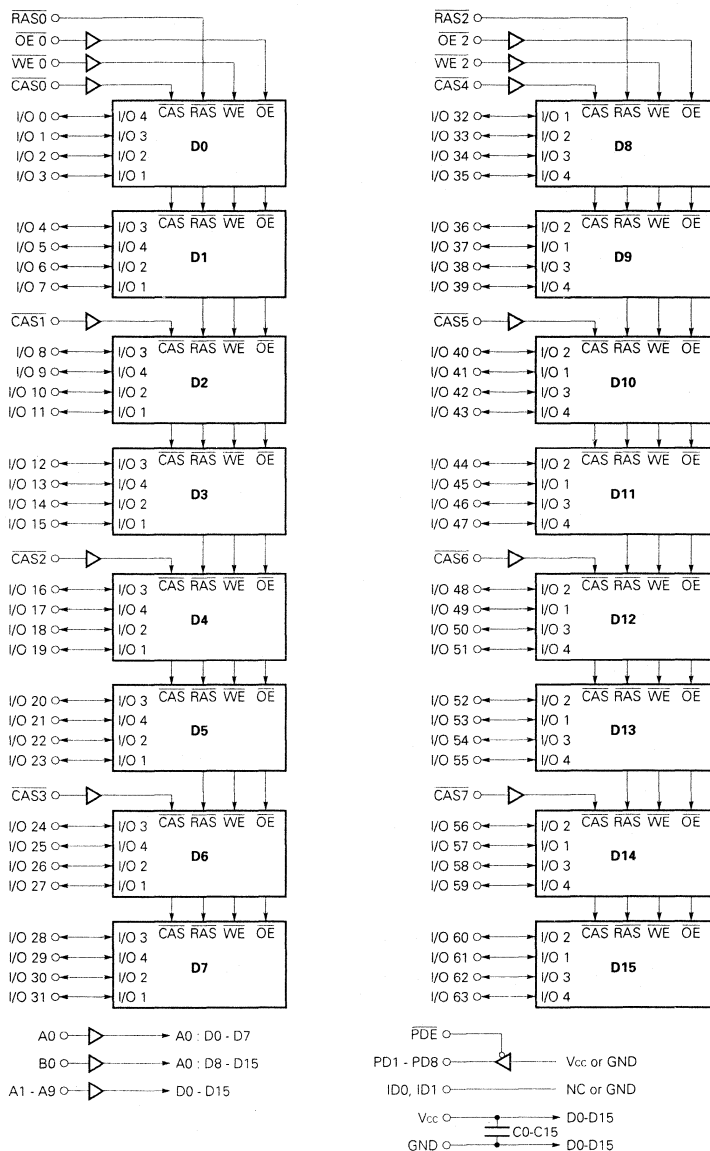
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	H	H	H
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

- A0 - A9, B0 : Address Inputs
- I/O 0 - I/O 63 : Data Inputs/Outputs
- RAS0, RAS2 : Row Address Strobe
- CAS0 - CAS7 : Column Address Strobe
- WE0, WE2 : Write Enable
- OE0, OE2 : Output Enable
- PDE : Presence Detect Enable
- PD1 - PD8 : Presence Detect Pins
- ID0, ID1 : Identity Pins
- V_{cc} : Power Supply
- GND : Ground
- NC : No connection

Block Diagram



Remark D0 - D15 : μ PD424400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		18	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

★

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE}0$, $\overline{WE}2$			20	
	C_{I3}	RAS0, RAS2			78	
	C_{I4}	CAS0 - CAS7			20	
	C_{I5}	$\overline{OE}0$, $\overline{OE}2$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O63			20	pF

★ DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		1,984	mA	3, 4, 7
			$t_{\text{RAC}} = 70 \text{ ns}$		1,664		
			$t_{\text{RAC}} = 80 \text{ ns}$		1,504		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$	$I_{\text{O}} = 0 \text{ mA}$		96	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$I_{\text{O}} = 0 \text{ mA}$		80		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\text{CAS} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		1,984	mA	3, 4, 5, 7
			$t_{\text{RAC}} = 70 \text{ ns}$		1,664		
			$t_{\text{RAC}} = 80 \text{ ns}$		1,504		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		1,504	mA	3, 4, 6
			$t_{\text{RAC}} = 70 \text{ ns}$		1,344		
			$t_{\text{RAC}} = 80 \text{ ns}$		1,184		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$		1,984	mA	3, 4
			$t_{\text{RAC}} = 70 \text{ ns}$		1,664		
			$t_{\text{RAC}} = 80 \text{ ns}$		1,504		
Input leakage current	I _{I(IL)}	$V_{\text{I}} = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	$\overline{\text{RAS}}$	-10	+10	μA	
			Others	-5	+1		
Output leakage current	I _{O(IL)}	$V_{\text{O}} = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)		-10	+10	μA	
High level output voltage	V _{OH}	$I_{\text{O}} = -5.0 \text{ mA}$		2.4		V	
Low level output voltage	V _{OL}	$I_{\text{O}} = +4.2 \text{ mA}$			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

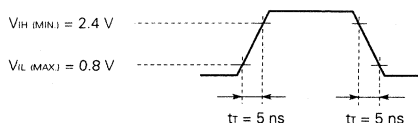
Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	110		130		160		ns	
Read Modify Write Cycle Time	t _{RWC}	165		190		225		ns	
Fast Page Mode Cycle Time	t _{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	80		90		100		ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	t _{CAC}		20		25		25	ns	10, 11
Access Time Column Address	t _{AA}		35		40		45	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		40		45		50	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEA}		15		20		20	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{OFF}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OEZ}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ Hold Time	t _{OEH}	0		0		0		ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40		50		70		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15		20		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		10		ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		10		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40		45		50		ns	
Row Address Setup Time	t _{ASR}	5		5		5		ns	
Row Address Hold Time	t _{RAH}	10		10		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		10		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	14
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		15		ns	15
$\overline{\text{WE}}$ Pulse Width	t _{WP}	10		10		15		ns	15

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t _{DS}	0		0		0		ns	16
Data-in Hold Time	t _{DH}	15		15		15		ns	16
Write Command Setup Time	t _{WCS}	0		0		0		ns	17
CAS to WE Delay Time	t _{CWD}	35		40		45		ns	17
RAS to WE Delay Time	t _{RWD}	90		100		115		ns	17
CAS Precharge to WE Delay Time	t _{CPWD}	55		60		70		ns	17
Column Address to WE Delay Time	t _{AWD}	55		60		70		ns	17
WE Lead Time Referenced to RAS	t _{RWL}	20		25		25		ns	
WE Lead Time Referenced to CAS	t _{CWL}	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	t _{CSR}	10		10		10		ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10		10		15		ns	
WE Setup Time	t _{WSR}	0		0		10		ns	
WE Hold Time	t _{WHR}	10		10		15		ns	
Refresh Time	t _{REF}		16		16		16	ms	

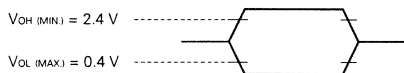
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on cycle rates (trc and trc).
4. Specified values are obtained with outputs unloaded.
5. Icc3 is measured assuming that all column address inputs are held at either high or low.
6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}} (\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}} (\text{MIN.})$.
8. AC measurements assume $\text{tr} = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

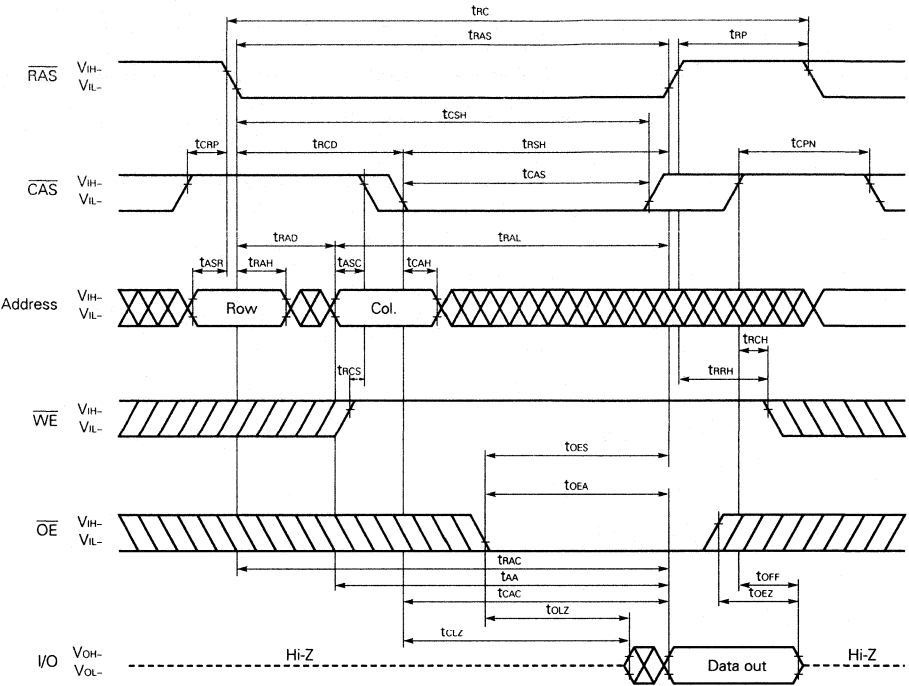
Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{trAD} \leq \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$	$\text{trAC} (\text{MAX.})$
$\text{trAD} > \text{trAD} (\text{MAX.})$ and $\text{trCD} \leq \text{trCD} (\text{MAX.})$	$\text{tAA} (\text{MAX.})$	$\text{trAD} + \text{tAA} (\text{MAX.})$
$\text{trCD} > \text{trCD} (\text{MAX.})$	$\text{tCAC} (\text{MAX.})$	$\text{trCD} + \text{tCAC} (\text{MAX.})$

$\text{trAD} (\text{MAX.})$ and $\text{trCD} (\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trAC , tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{trAD} \geq \text{trAD} (\text{MAX.})$ and $\text{trCD} \geq \text{trCD} (\text{MAX.})$ will not cause any operation problems.

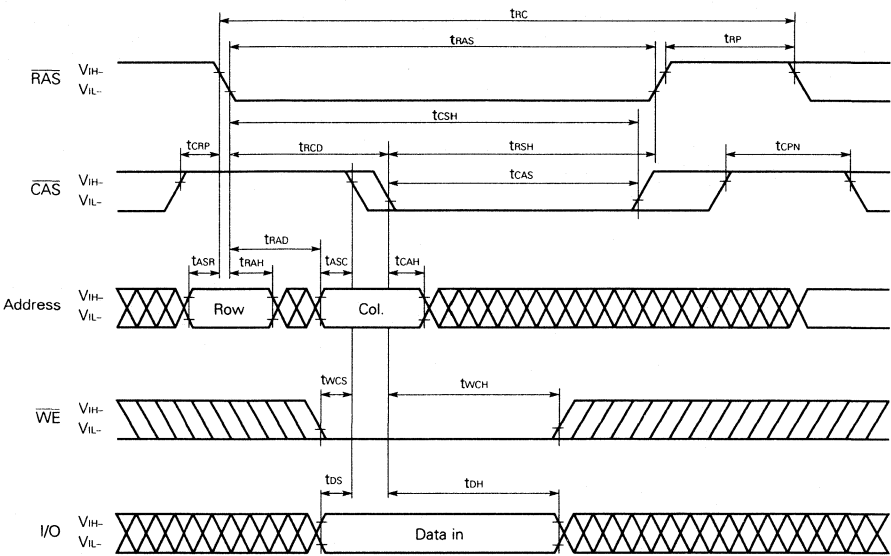
11. Loading conditions are 2 TTLs and 100 pF.
12. $\text{toFF} (\text{MAX.})$ and $\text{toEZ} (\text{MAX.})$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $\text{tCRP} (\text{MIN.})$ requirements should be applied to $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
14. Either $\text{trCH} (\text{MIN.})$ or $\text{trRH} (\text{MIN.})$ should be met in read cycles.
15. $\text{tWP} (\text{MIN.})$ is applied to late write cycles or read modify write cycles. In early write cycles, $\text{twCH} (\text{MIN.})$ should be met.

16. $t_{DS}(\text{MIN.})$ and $t_{DH}(\text{MIN.})$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $twcs \geq twcs(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $trwd \geq trwd(\text{MIN.})$, $tcwd \geq tcwd(\text{MIN.})$, $tawd \geq tawd(\text{MIN.})$ and $tcpwd \geq tcpwd(\text{MIN.})$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Read Cycle

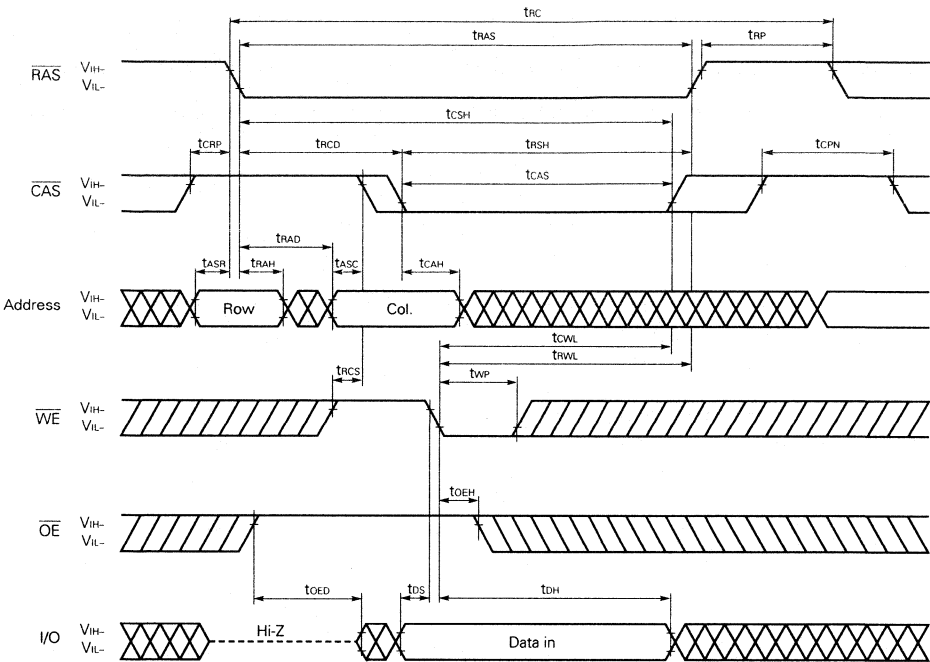


Early Write Cycle

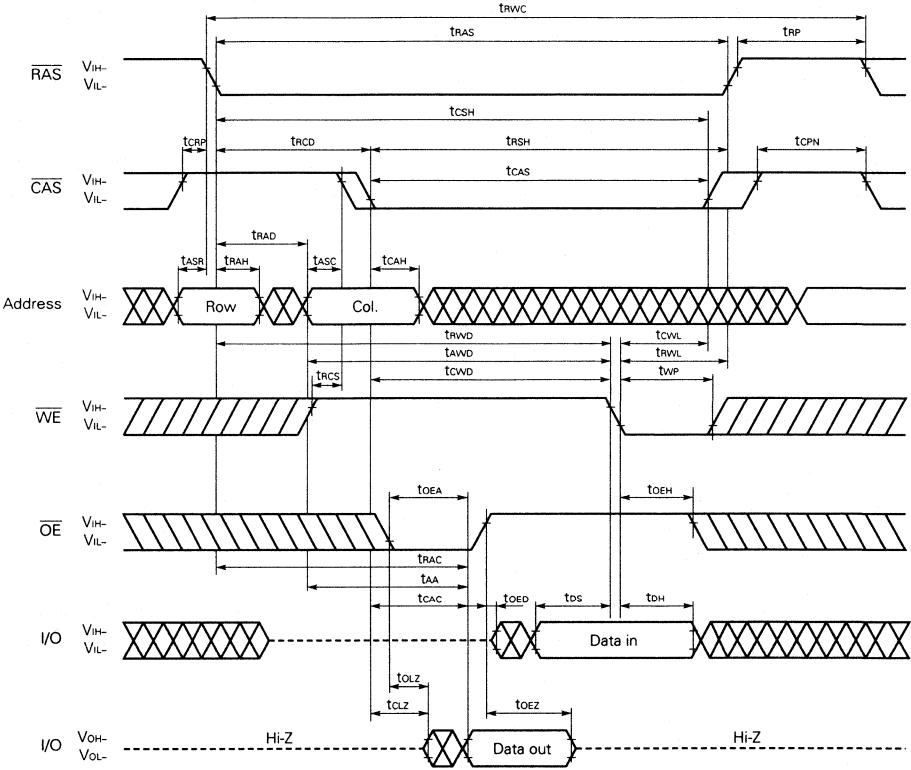


Remark $\overline{OE}$: Don't care

Late Write Cycle



Read Modify Write Cycle



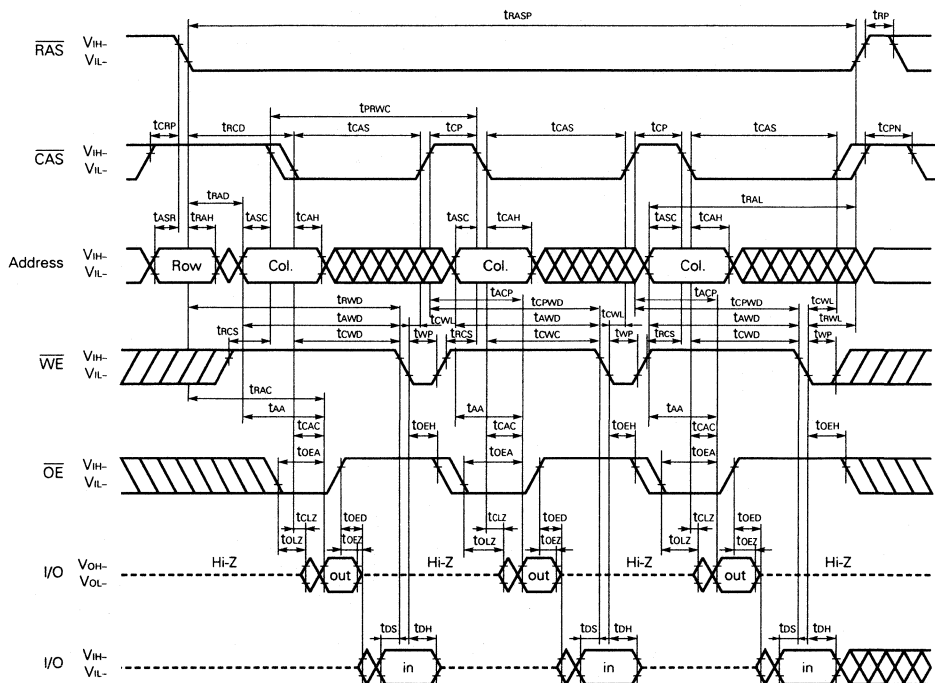
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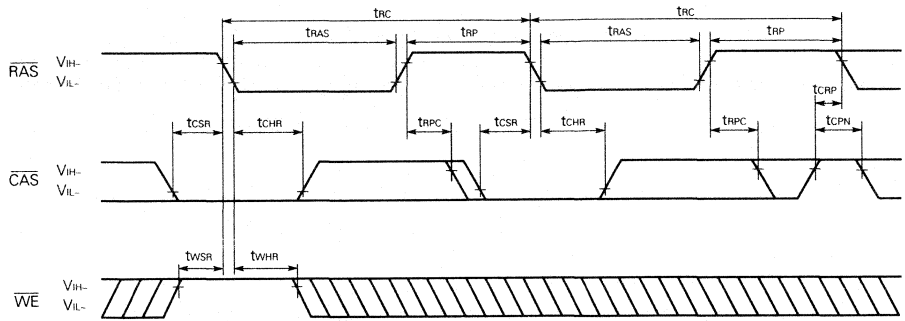
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Fast Page Mode Read Modify Write Cycle



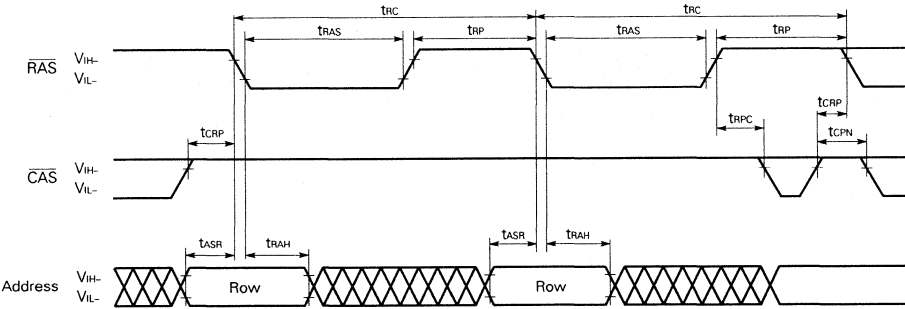
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



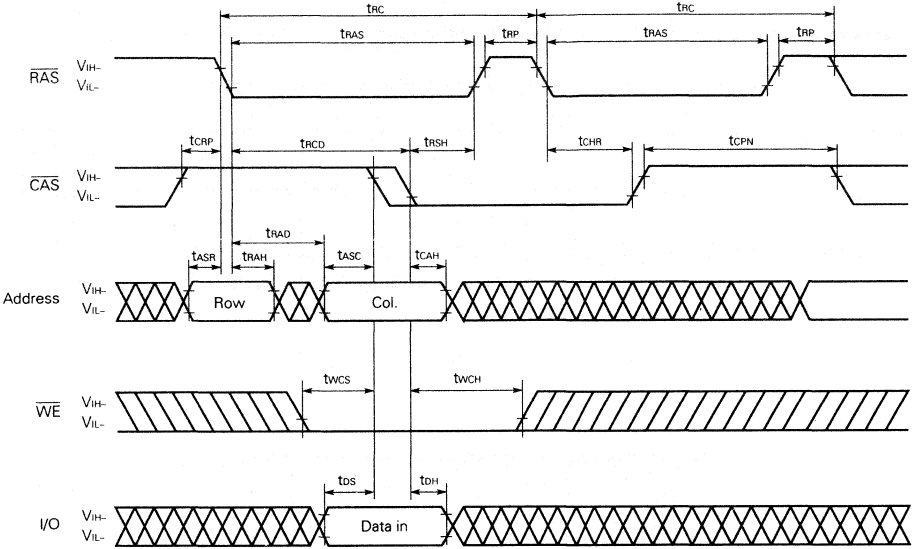
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

RAS Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

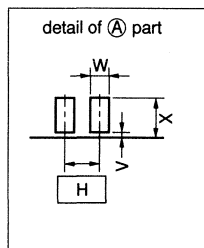
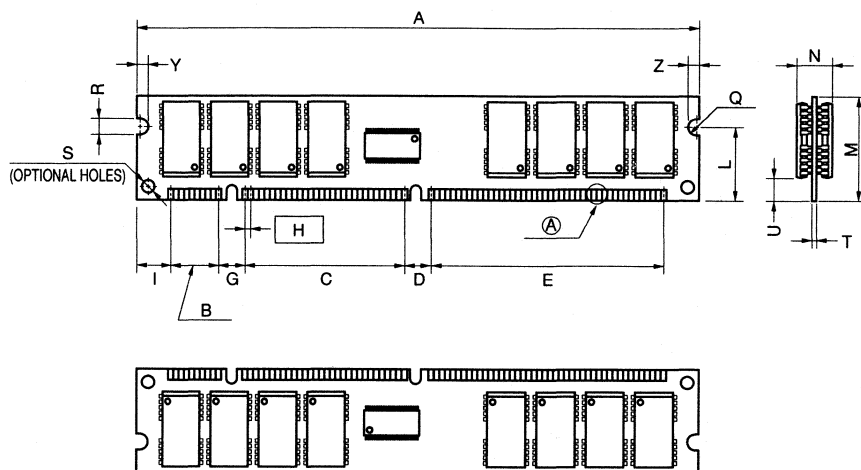
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
L	17.78	0.700
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039 ^{+0.003} _{-0.002}
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A1

1M -WORD BY 64-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-421000AA64FB is a 1 048 576 words by 64 bits dynamic RAM module on which 4 pieces of 16M DRAM (μ PD 4218160) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1 048 576 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC- 421000AA64-60	60ns	110ns	3.70 w	357 mw (CMOS level)
MC- 421000AA64-70	70ns	130ns	3.49 w	
MC- 421000AA64-80	80ns	150ns	3.28 w	

- 1 024 refresh cycles/16 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh , $\overline{\text{RAS}}$ only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +5.0V $\pm$ 0.25V power supply

The information in this document is subject to change without notice.

Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 421000AA64FB-60	60ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of uPD 4218160LE (400mil SOJ) [Single side]
MC- 421000AA64FB-70	70ns		
MC- 421000AA64FB-80	80ns		

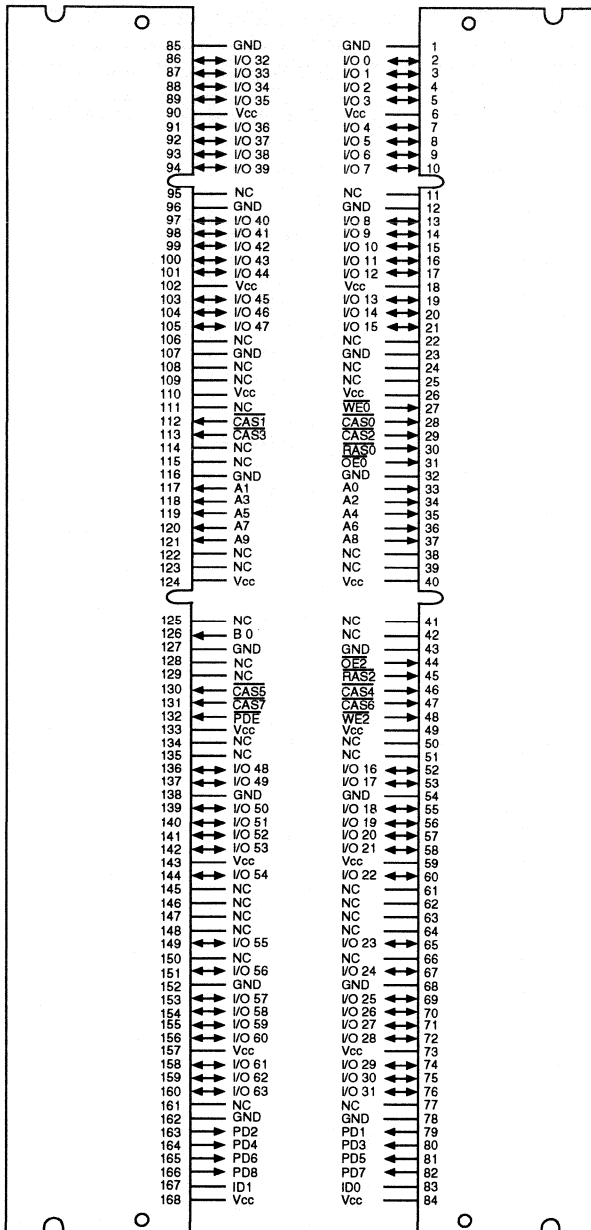
Quality grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



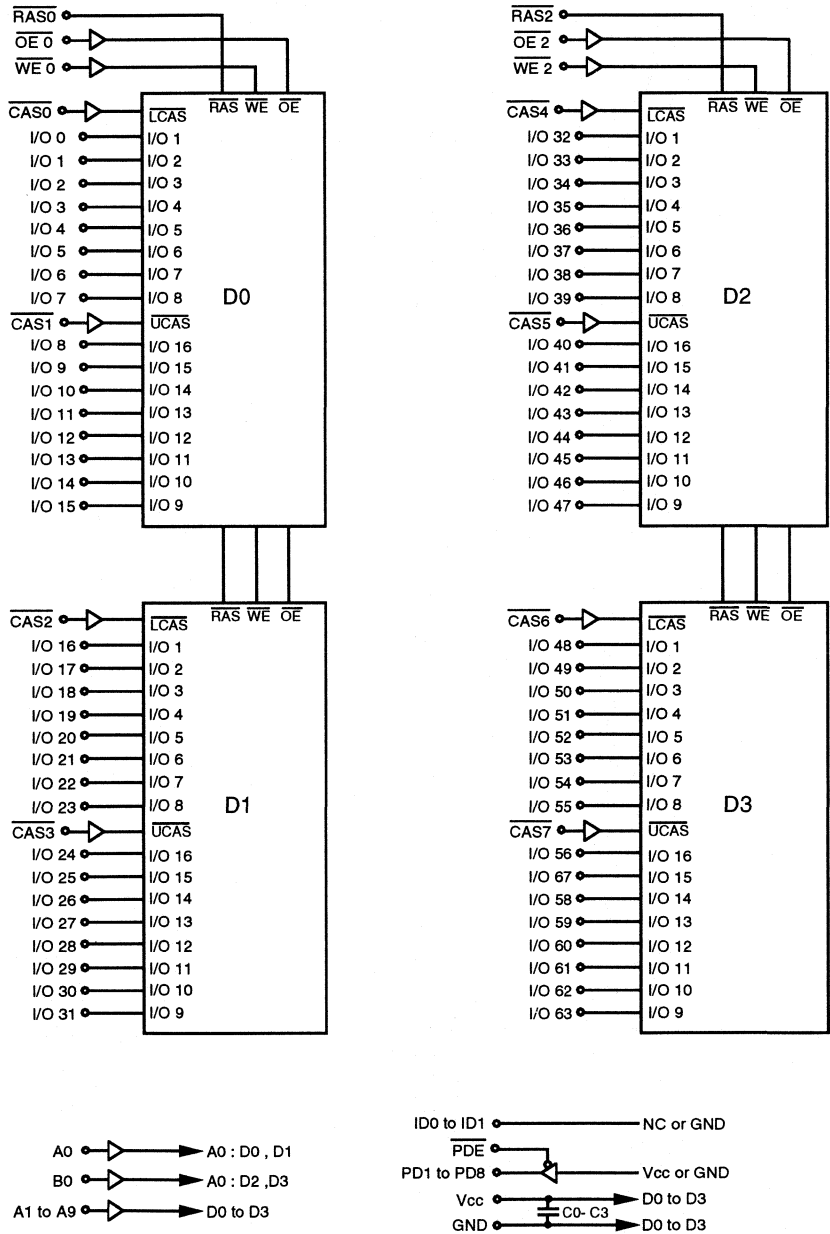
PD and ID Table

Pin Name	Pin No.	Access Time		
		60ns	70ns	80ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	H	H	H
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Note) H : VOH, L : VOL

A0 - A9, B0 : Address Inputs
 I/O 0-I/O 63 : Data Inputs / Outputs
 RAS0, RAS2 : Row Address Strobe
 CAS0-CAS7 : Column Address Strobe
 WE0, WE2 : Write Enable
 OE0, OE2 : Output Enable
 PDE : Presence Detect Enable
 PD1- PD8 : Presence Detect Pins
 ID0, ID1 : Identity pins
 Vcc : Power Supply
 GND : Ground
 NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0 to +7.0	V
Supply voltage	VCC		-1.0 to +7.0	V
Output current	IO		50	mA
Power dissipation	PD		4	W
Operating temperature	Topt		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES : 1, 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		4.75	5.0	5.25	V
High level input voltage	VIH		2.4		Vcc + 1.0	V
Low level input voltage	VIL		-1.0		+0.8	V
Ambient temperature	Ta		0		70	°C

CAPACITANCE (Ta=25°C , f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C I 1	A0 - A9,B0			20	pF
	C I 2	$\overline{WE} 0, \overline{WE} 2$			20	pF
	C I 3	$\overline{RAS} 0, \overline{RAS} 2$			45	pF
	C I 4	$\overline{CAS} 0 - \overline{CAS} 7$			20	pF
	C I 5	$\overline{OE} 0, \overline{OE} 2$			20	pF
Data Input/ Output capacitance	C I/O	I/O 0 - I/O 63			20	pF

DC CHARACTERISTICS**(Recommended Operating Conditions unless otherwise noted)**

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	I _{cc1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}}=t_{\text{RC}}(\text{MIN.}), I_{\text{O}}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		704	mA	3, 4, 7
			$t_{\text{RAC}}=70\text{ns}$		664		
			$t_{\text{RAC}}=80\text{ns}$		624		
Standby Current	I _{cc2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$			72	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}}-0.2\text{V}$			68		
$\overline{\text{RAS}}$ only refresh current	I _{cc3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}$ $t_{\text{RC}}=t_{\text{RC}}(\text{MIN.}), I_{\text{O}}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		704	mA	3, 4, 7
			$t_{\text{RAC}}=70\text{ns}$		664		
			$t_{\text{RAC}}=80\text{ns}$		624		
Operating Current (Fast Page Mode)	I _{cc4}	$\overline{\text{RAS}} \leq V_{\text{IL}}, \overline{\text{CAS}}$ Cycling $t_{\text{PC}}=t_{\text{PC}}(\text{MIN.}), I_{\text{O}}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		424	mA	3, 4, 6
			$t_{\text{RAC}}=70\text{ns}$		384		
			$t_{\text{RAC}}=80\text{ns}$		344		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{cc5}	$t_{\text{RC}}=t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		704	mA	3, 4
			$t_{\text{RAC}}=70\text{ns}$		664		
			$t_{\text{RAC}}=80\text{ns}$		624		
Input Leakage Current	I _{I(L)}	V _I =0 to 5.5V all other pins not under test = 0V	$\overline{\text{RAS}}$	-10	+10	μA	
			others	-5	+1		
Output Leakage Current	I _{O(L)}	Outputs are disabled (Hi - Z) V _O =0 to 5.5V		-10	+10	μA	
High level output voltage	V _{OH}	I _O =-5mA		2.4		V	
Low level output voltage	V _{OL}	I _O =+4.2mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8, 9

(1/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		tRAC = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	tRC	110	-	130	-	150	-	ns	
Read Modify Write Cycle Time	tRWC	173	-	195	-	215	-	ns	
Fast Page Mode Cycle Time (Read or Write)	tPC	40	-	45	-	50	-	ns	
Read Modify Write Cycle Time (Fast Page Mode)	tPRWC	85	-	90	-	105	-	ns	
Access Time from $\overline{\text{RAS}}$	tRAC	-	60	-	70	-	80	ns	10, 11
Access Time from $\overline{\text{CAS}}$	tCAC	-	20	-	25	-	25	ns	10, 11
Access Time from Column Address	tAA	-	35	-	40	-	45	ns	10, 11
Access Time from $\overline{\text{CAS}}$ Precharge	tACP	-	40	-	45	-	50	ns	11
Access Time from $\overline{\text{OE}}$	tOEA	-	15	-	20	-	20	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	tRAD	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	tCLZ	0	-	0	-	0	-	ns	11
$\overline{\text{OE}}$ to Data Setup Time	tOLZ	0	-	0	-	0	-	ns	11
Output Buffer Turn-off Delay Time($\overline{\text{CAS}}$)	tOFF	0	13	0	15	0	15	ns	12
$\overline{\text{OE}}$ to Data Delay Time	tOED	13	-	15	-	15	-	ns	
Output Buffer Turn-off Delay Time($\overline{\text{OE}}$)	tOEZ	0	13	0	15	0	15	ns	12
$\overline{\text{OE}}$ Command Hold Time	tOEH	0	-	0	-	0	-	ns	
$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ inactive Setup Time	tOES	0	-	0	-	0	-	ns	
Transition Time (Rise and Fall)	tT	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	tRP	40	-	50	-	60	-	ns	
$\overline{\text{RAS}}$ Pulse Width(Random Read, Write Cycle)	tRAS	60	10 000	70	10 000	80	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	tRASP	60	125 000	70	125 000	80	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	tRSH	15	-	18	-	20	-	ns	
$\overline{\text{CAS}}$ Pulse Width	tCAS	15	10 000	20	10 000	20	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	tCSH	60	-	70	-	80	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	tRCD	20	45	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	tCRP	5	-	5	-	5	-	ns	13
$\overline{\text{CAS}}$ Precharge Time	tCPN	10	-	10	-	10	-	ns	
$\overline{\text{CAS}}$ Precharge Time(Fast Page Mode)	tCP	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	tRPC	5	-	5	-	5	-	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	tRHCP	40	-	45	-	50	-	ns	
Row Address Set Up Time	tASR	5	-	5	-	5	-	ns	
Row Address Hold Time	tRAH	10	-	10	-	12	-	ns	
Column Address Set Up Time	tASC	0	-	0	-	0	-	ns	
Column Address Hold Time	tCAH	15	-	15	-	15	-	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	tRAL	30	-	35	-	40	-	ns	
Lead Command Setup Time	tRCS	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	tRRH	0	-	0	-	0	-	ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	tRCH	0	-	0	-	0	-	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	tWCH	10	-	10	-	15	-	ns	15

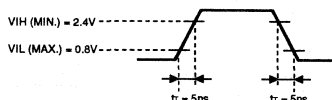
(2/2)

PARAMETER	SYMBOL	t _{TRAC} = 60ns		t _{TRAC} = 70ns		t _{TRAC} = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Command Set-Up Time	t _{WP}	10	-	10	-	15	-	ns	15
Data-in Setup Time	t _{DS}	0	-	0	-	0	-	ns	16
Data-in Hold Time	t _{DH}	10	-	15	-	15	-	ns	16
Write Command Setup Time	t _{WCS}	0	-	0	-	0	-	ns	17
CAS to WE Delay Time	t _{CWD}	38	-	40	-	45	-	ns	17
RAS to WE Delay Time	t _{RWD}	93	-	105	-	115	-	ns	17
CAS Precharge Delay Time Referenced to WE (Fast Page Mode)	t _{CPWD}	60	-	65	-	70	-	ns	17
Column Address Delay Time Referenced to WE	t _{AWD}	58	-	65	-	70	-	ns	17
Write Command Lead Time Referenced to RAS	t _{RWL}	25	-	25	-	25	-	ns	
Write Command Lead Time Referenced to CAS	t _{CWL}	15	-	15	-	15	-	ns	
CAS Setup Time for CAS before RAS Refresh	t _{CSR}	5	-	5	-	5	-	ns	
CAS Hold Time for CAS before RAS Refresh	t _{CHR}	10	-	10	-	10	-	ns	
WE Hold Time	t _{WHR}	15	-	15	-	15	-	ns	
Refresh Time	t _{REF}	-	16	-	16	-	16	ms	

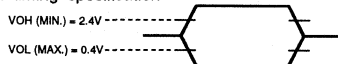
Notes:

1. All voltages are referenced to GND .
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. tCC1 , tCC3 , tCC4 and tCC5 depend on cycle rates (tRC and tPC) .
4. Specified values are obtained with outputs unloaded.
5. tCC3 is measured assuming that all column address inputs are held at either high or low.
6. tCC4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. tCC1 and tCC3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$ and $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$.
8. AC measurements assume $\text{tr} = 5\text{ns}$.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



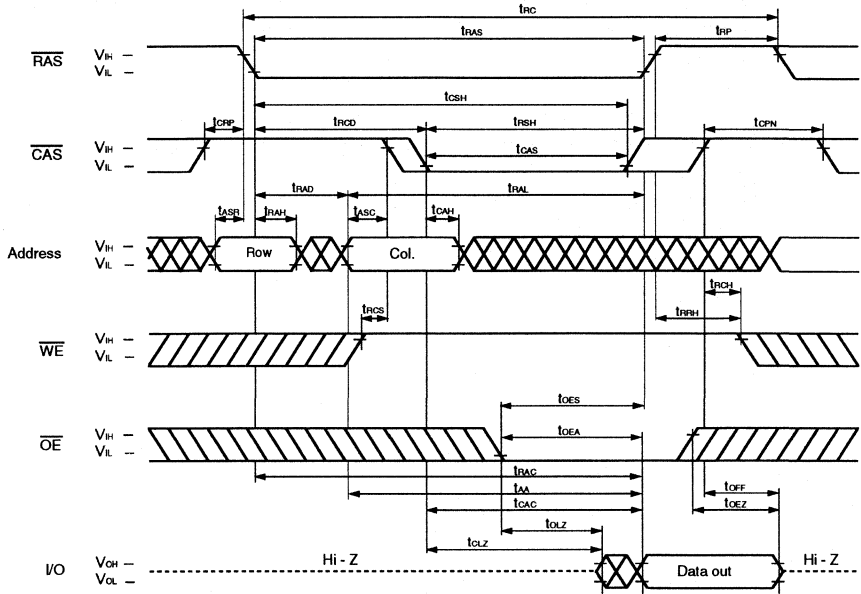
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$\text{t}_{\text{RAD}} \leq \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \leq \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{RAC}}(\text{MAX.})$	$\text{t}_{\text{RAC}}(\text{MAX.})$
$\text{t}_{\text{RAD}} > \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \leq \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{AA}}(\text{MAX.})$	$\text{t}_{\text{RAD}} + \text{t}_{\text{AA}}(\text{MAX.})$
$\text{t}_{\text{RCD}} > \text{t}_{\text{RCD}}(\text{MAX.})$	$\text{t}_{\text{CAC}}(\text{MAX.})$	$\text{t}_{\text{RCD}} + \text{t}_{\text{CAC}}(\text{MAX.})$

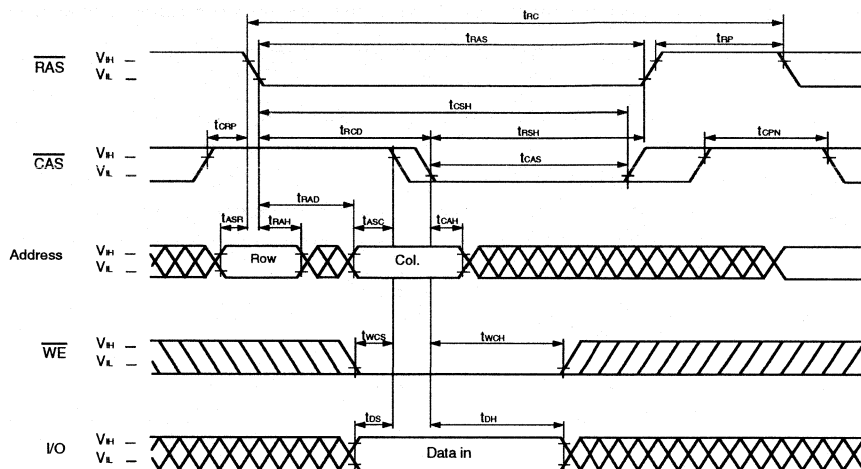
$\text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}}(\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $\text{t}_{\text{RAD}} \geq \text{t}_{\text{RAD}}(\text{MAX.})$ and $\text{t}_{\text{RCD}} \geq \text{t}_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

11. Loading conditions are 1 TTLs and 100 pF.
12. $\text{t}_{\text{OFF}}(\text{MAX.})$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $\text{t}_{\text{CRP}}(\text{MIN.})$ requirement should be applied to $\overline{\text{RAS}} / \overline{\text{CAS}}$ cycles.
14. Either $\text{t}_{\text{RCH}}(\text{MIN.})$ or $\text{t}_{\text{RRH}}(\text{MIN.})$ should be met in read cycles.
15. $\text{t}_{\text{WP}}(\text{MIN.})$ is applied to late write cycles or read modify write cycles. In early write cycles, $\text{t}_{\text{WCH}}(\text{MIN.})$ should be met.
16. $\text{t}_{\text{DS}}(\text{MIN.})$ and $\text{t}_{\text{DH}}(\text{MIN.})$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
17. If $\text{t}_{\text{WCS}} \geq \text{t}_{\text{WCS}}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle . If $\text{t}_{\text{RW}} \geq \text{t}_{\text{RW}}(\text{MIN.})$, $\text{t}_{\text{CWD}} \geq \text{t}_{\text{CWD}}(\text{MIN.})$, $\text{t}_{\text{AWD}} \geq \text{t}_{\text{AWD}}(\text{MIN.})$ and $\text{t}_{\text{CPWD}} \geq \text{t}_{\text{CPWD}}(\text{MIN.})$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Read Cycle

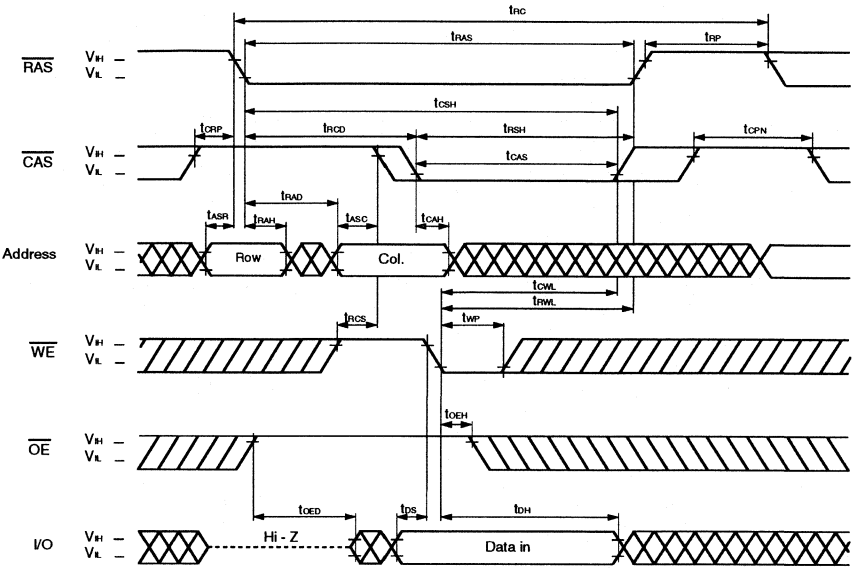


Early Write Cycle

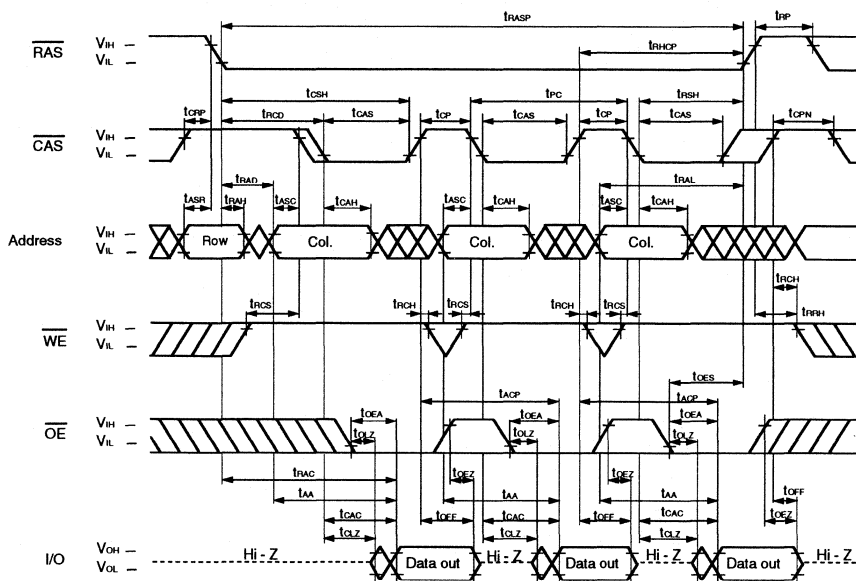


Remark $\overline{OE}$: Don't care

Late Write Cycle

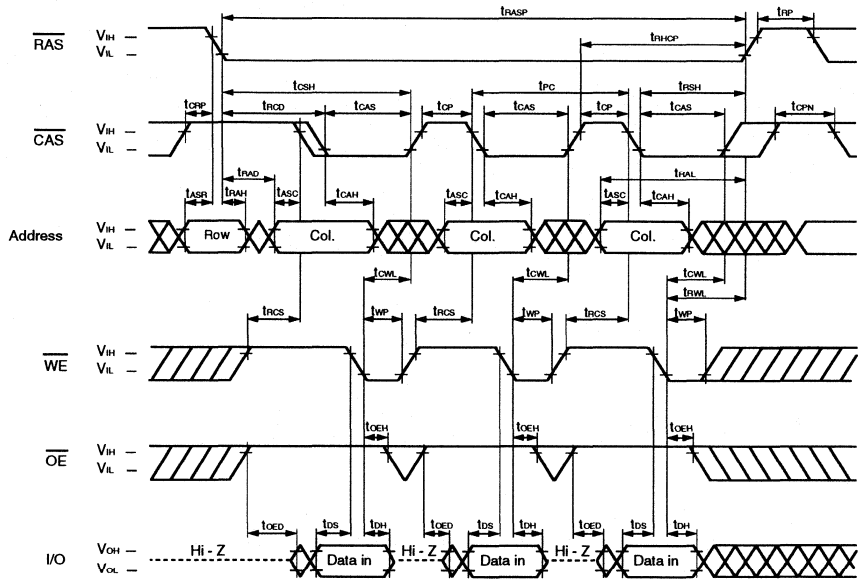


Fast Page Mode Read Cycle



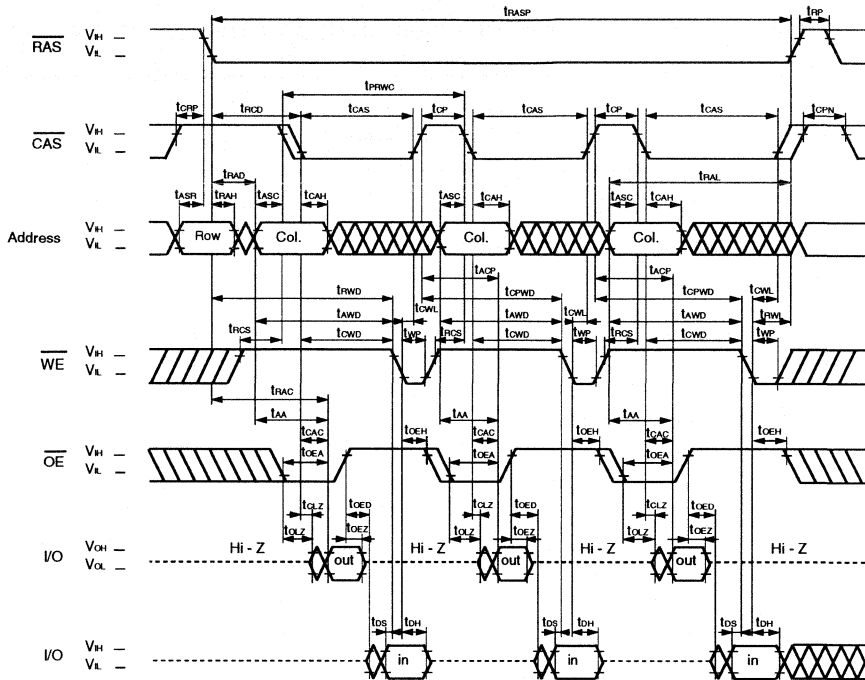
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Late Write Cycle

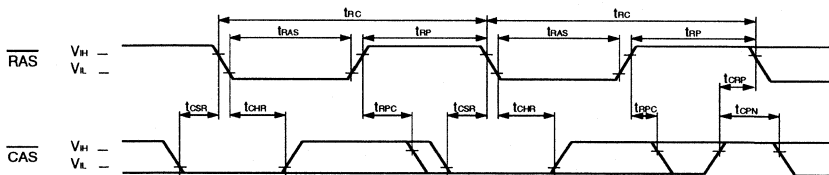


Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

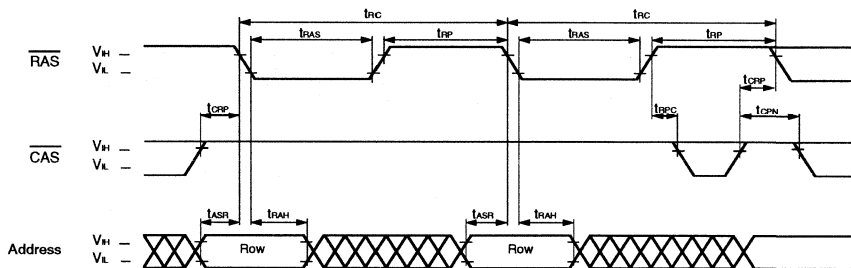
Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

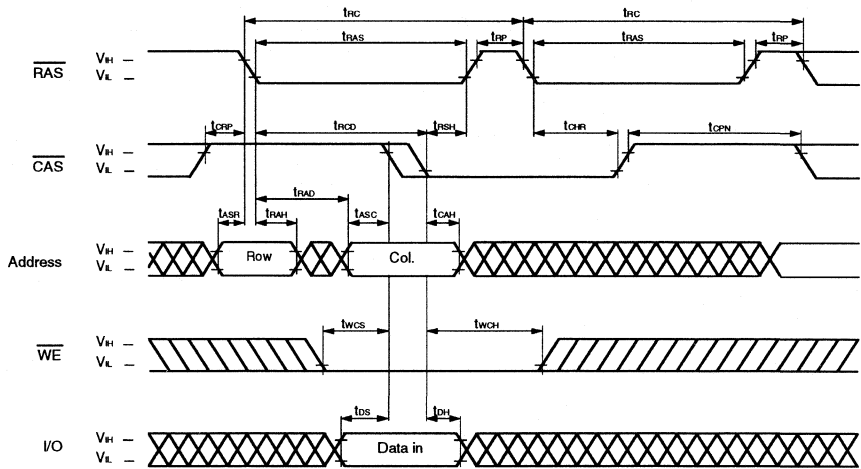
CAS Before RAS Refresh Cycle

Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O : Hi - Z

RAS Only Refresh Cycle

Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O : Hi - Z

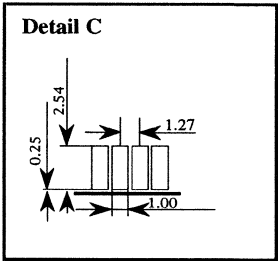
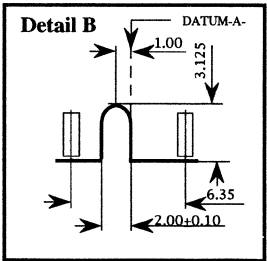
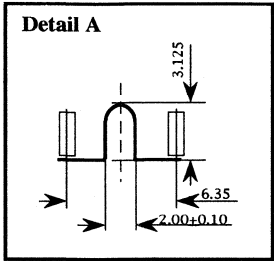
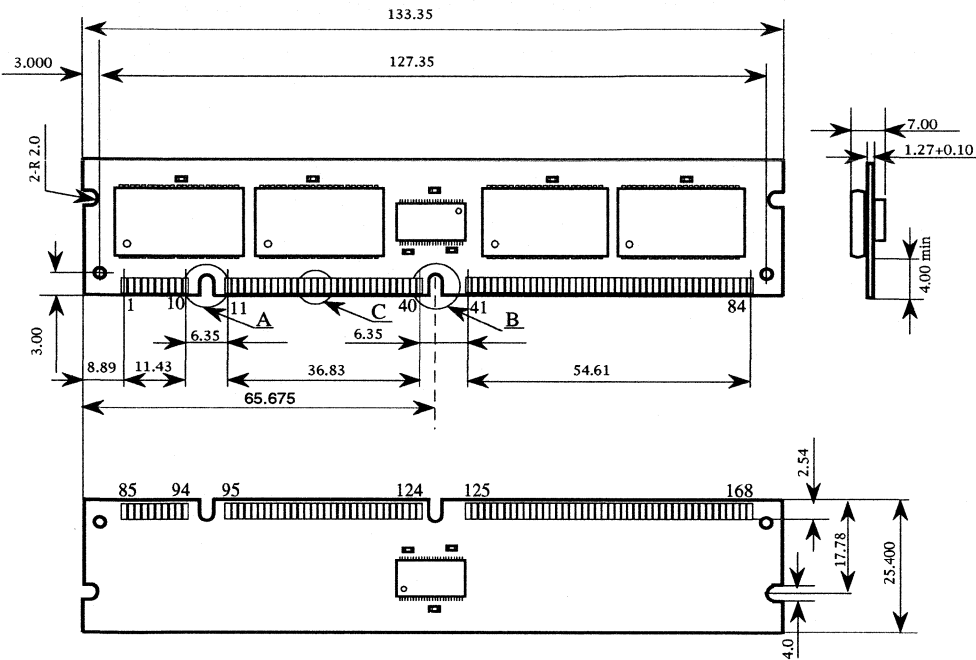
Hidden Refresh Cycle (Write)



Remark OE : Don't care

Package Drawing

UNIT: mm



3.3 V OPERATION 4M -WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-424000LAB72F is a 4 194 304 words by 72 bits dynamic RAM module on which 18 pieces of 16M DRAM (μ PD 4217400L) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4 194 304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC- 424000LAB72-60	60ns	110ns	6.52 w	68.4 mw (CMOS level)
MC- 424000LAB72-70	70ns	130ns	5.87 w	
MC- 424000LAB72-80	80ns	150ns	5.22 w	

- 2 048 refresh cycles/32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh , $\overline{\text{RAS}}$ only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +3.3 V $\pm$ 0.3V power supply

The information in this document is subject to change without notice.

Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 424000LAB72F-60	60ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of uPD 4217400LG3 (300mil TSOP) [Double side]
MC- 424000LAB72F-70	70ns		
MC- 424000LAB72F-80	80ns		

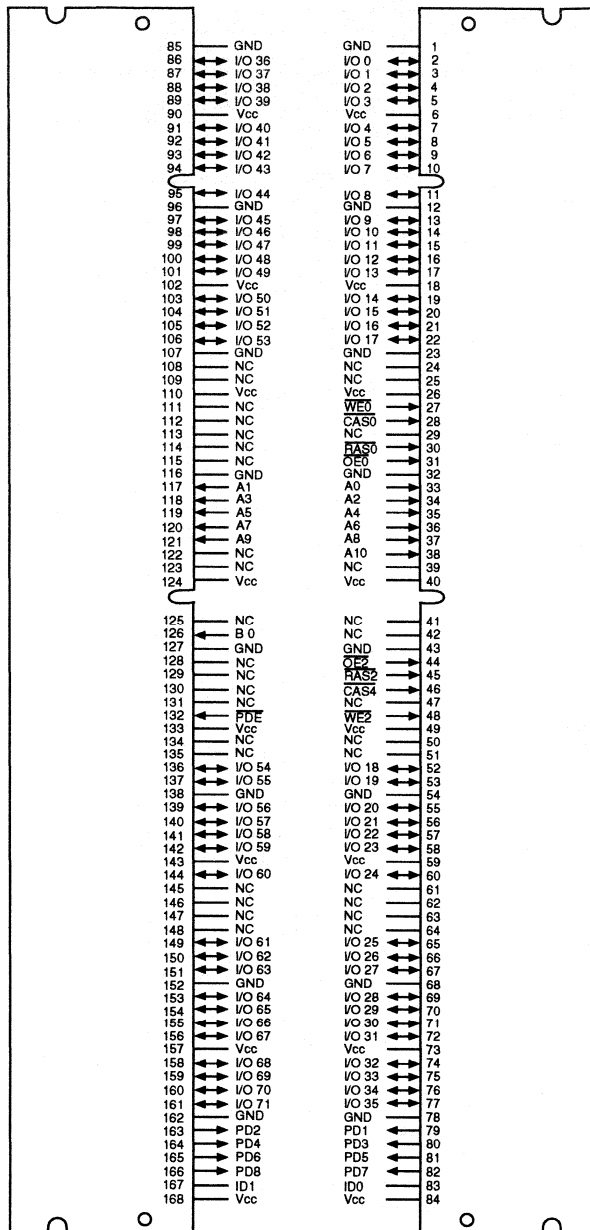
Quality grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



PD and ID Table

Pin Name	Pin No.	Access Time		
		60ns	70ns	80ns
PD1	79	H	H	H
PD2	163	H	H	H
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Note) H : VOH, L : VOL

A0 - A10, B0 : Address Inputs

I/O 0-I/O 71 : Data Inputs / Outputs

RAS0, RAS2 : Row Address Strobe

CAS0, CAS4 : Column Address Strobe

WE0, WE2 : Write Enable

OE0, OE2 : Output Enable

PDE : Presence Detect Enable

PD1- PD8 : Presence Detect Pins

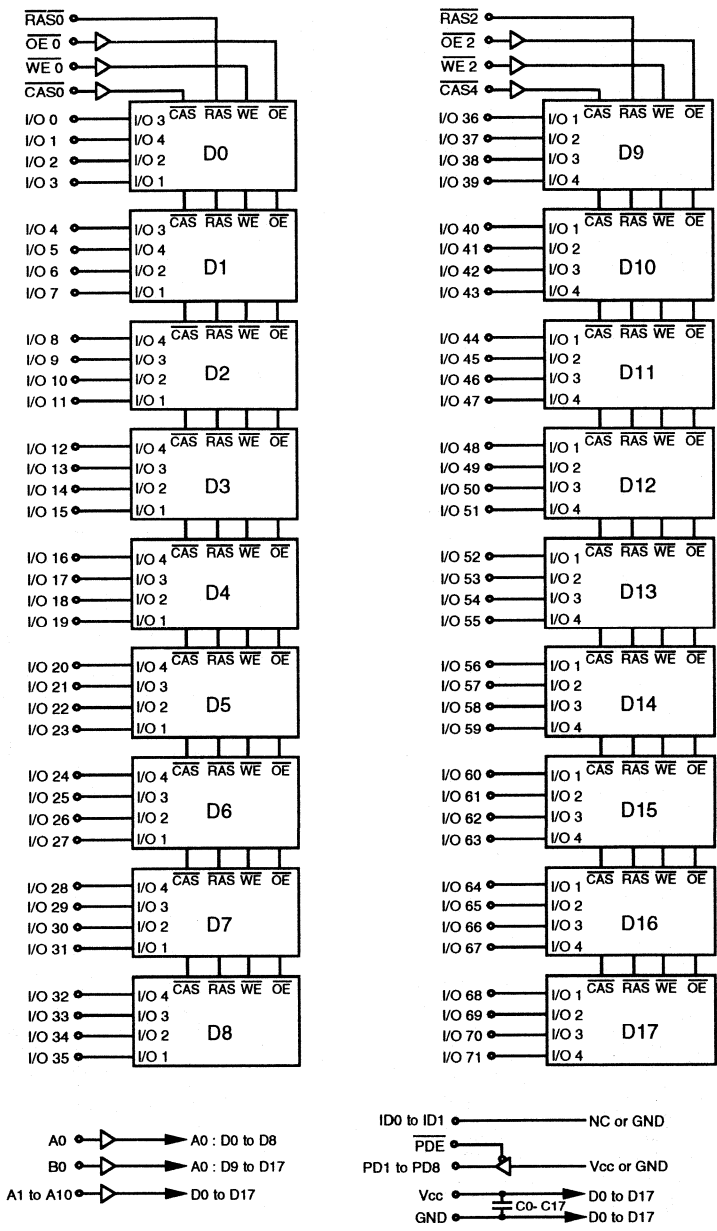
ID0, ID1 : Identity pins

Vcc : Power Supply

GND : Ground

NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-0.5 to +4.6	V
Supply voltage	VCC		-0.5 to +4.6	V
Output current	IO		20	mA
Power dissipation	PD		20	W
Operating temperature	T _{opt}		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES : 1, 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		3.0	3.3	3.6	V
High level input voltage	VIH		2.0		V _{CC} + 0.3	V
Low level input voltage	VIL		-0.3		+0.8	V
Ambient temperature	T _a		0		70	°C

CAPACITANCE (T_a=25°C , f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C I 1	A0 - A10, B0			20	pF
	C I 2	$\overline{\text{WE}} 0, \overline{\text{WE}} 2$			20	pF
	C I 3	$\overline{\text{RAS}} 0, \overline{\text{RAS}} 2$			78	pF
	C I 4	$\overline{\text{CAS}} 0, \overline{\text{CAS}} 4$			20	pF
	C I 5	$\overline{\text{OE}} 0, \overline{\text{OE}} 2$			20	pF
Data Input/ Output capacitance	C I/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS**(Recommended Operating Conditions unless otherwise noted)**

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	I _{cc1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}}=t_{\text{RC}}(\text{MIN.}), I_{\text{O}}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		1 810	mA	3,4,7
			$t_{\text{RAC}}=70\text{ns}$		1 630		
			$t_{\text{RAC}}=80\text{ns}$		1 450		
Standby Current	I _{cc2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$			46	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}}-0.2\text{V}$			19		
$\overline{\text{RAS}}$ only refresh current	I _{cc3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}$ $t_{\text{RC}}=t_{\text{RC}}(\text{MIN.}), I_{\text{O}}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		1 810	mA	3,4,5,7
			$t_{\text{RAC}}=70\text{ns}$		1 630		
			$t_{\text{RAC}}=80\text{ns}$		1 450		
Operating Current (Fast Page Mode)	I _{cc4}	$\overline{\text{RAS}} \leq V_{\text{IL}}, \overline{\text{CAS}}$ Cycling $t_{\text{PC}}=t_{\text{PC}}(\text{MIN.}), I_{\text{O}}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		1 270	mA	3,4,6
			$t_{\text{RAC}}=70\text{ns}$		1 090		
			$t_{\text{RAC}}=80\text{ns}$		910		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{cc5}	$t_{\text{RC}}=t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		1 810	mA	3,4
			$t_{\text{RAC}}=70\text{ns}$		1 630		
			$t_{\text{RAC}}=80\text{ns}$		1 450		
Input Leakage Current	I _{I(L)}	V _I =0 to 3.6V all other pins not under test = 0V	$\overline{\text{RAS}}$	-5	+5	μA	
			others	-5	+1		
Output Leakage Current	I _{O(L)}	Outputs are disabled (Hi - Z) V _O =0 to 3.6V		-5	+5	μA	
High level output voltage	V _{OH}	I _O =-2.0mA		2.4		V	
Low level output voltage	V _{OL}	I _O =+2.0mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

PARAMETER	SYMBOL	t _{RAC} = 60ns		t _{RAC} = 70ns		t _{RAC} = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	110	-	130	-	150	-	ns	
Read Modify Write Cycle Time	t _{RWC}	175	-	195	-	220	-	ns	
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40	-	45	-	50	-	ns	
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	85	-	90	-	105	-	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	-	60	-	70	-	80	ns	10,11
Access Time from $\overline{\text{CAS}}$	t _{CAC}	-	20	-	23	-	25	ns	10,11
Access Time from Column Address	t _{AA}	-	35	-	40	-	45	ns	10,11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	-	40	-	45	-	50	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEA}	-	15	-	18	-	20	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0	-	0	-	0	-	ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0	-	0	-	0	-	ns	11
Output Buffer Turn-off Delay Time($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	15	-	15	-	20	-	ns	
Output Buffer Turn-off Delay Time($\overline{\text{OE}}$)	t _{OEZ}	0	15	0	15	0	20	ns	12
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	0	-	0	-	0	-	ns	
$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ inactive Setup Time	t _{OES}	0	-	0	-	0	-	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	-	50	-	60	-	ns	
$\overline{\text{RAS}}$ Pulse Width(Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	-	18	-	20	-	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10 000	18	10 000	20	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60	-	70	-	80	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	-	5	-	5	-	ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10	-	10	-	10	-	ns	
$\overline{\text{CAS}}$ Precharge Time(Fast Page Mode)	t _{CP}	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5	-	5	-	5	-	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40	-	45	-	50	-	ns	
Row Address Set Up Time	t _{ASR}	5	-	5	-	5	-	ns	
Row Address Hold Time	t _{RAH}	10	-	10	-	12	-	ns	
Column Address Set Up Time	t _{ASC}	0	-	0	-	0	-	ns	
Column Address Hold Time	t _{CAH}	15	-	15	-	15	-	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30	-	35	-	40	-	ns	
Lead Command Setup Time	t _{RCS}	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0	-	0	-	0	-	ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0	-	0	-	0	-	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10	-	10	-	15	-	ns	15

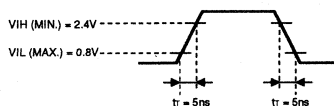
(2/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		tRAC = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Comand Set-Up Time	tWP	10	-	10	-	15	-	ms	15
Data-in Seup Time	tDS	0	-	0	-	0	-	ns	16
Data-in Hold Time	tDH	10	-	15	-	15	-	ns	16
Write Comand Setup Time	tWCS	0	-	0	-	0	-	ns	17
CAS to WE Delay Time	tCWD	40	-	43	-	50	-	ns	17
RAS to WE Delay Time	tRWD	95	-	105	-	120	-	ns	17
CAS Precharge Delay Time Referenced to WE (Fast Page Mode)	tCPWD	58	-	65	-	70	-	ns	17
Column Address Delay Time Referenced to WE	tAWD	60	-	65	-	75	-	ns	17
Write Command Lead Time Referenced to RAS	tRWL	25	-	25	-	25	-	ns	
Write Command Lead Time Referenced to CAS	tCWL	15	-	15	-	15	-	ns	
CAS Setup Time for CAS before RAS Refresh	tCSR	5	-	5	-	5	-	ns	
CAS Hold Time for CAS before RAS Refresh	tCHR	10	-	10	-	10	-	ns	
WE Setup Time	tWSR	10	-	10	-	10	-	ns	
WE Hold Time	tWHR	15	-	15	-	15	-	ns	
Refresh Time	tREF	-	32	-	32	-	32	ms	

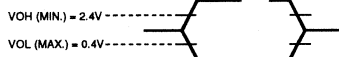
Notes:

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. Icc3 is measured assuming that all column address inputs are held at either high or low.
6. Icc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL(MAX.)}}$ and $\overline{\text{CAS}} \geq V_{\text{IH(MIN.)}}$.
8. AC measurements assume $t_r = 5\text{ns}$.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification

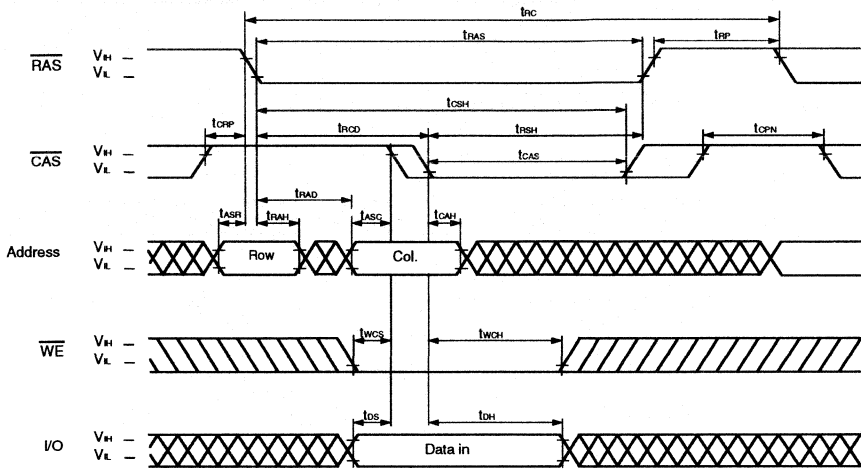


10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD(MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD(MAX.)}}$	$t_{\text{RAC(MAX.)}}$	$t_{\text{RAC(MAX.)}}$
$t_{\text{RAD}} > t_{\text{RAD(MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD(MAX.)}}$	$t_{\text{AA(MAX.)}}$	$t_{\text{RAD}} + t_{\text{AA(MAX.)}}$
$t_{\text{RCD}} > t_{\text{RCD(MAX.)}}$	$t_{\text{CAC(MAX.)}}$	$t_{\text{RCD}} + t_{\text{CAC(MAX.)}}$

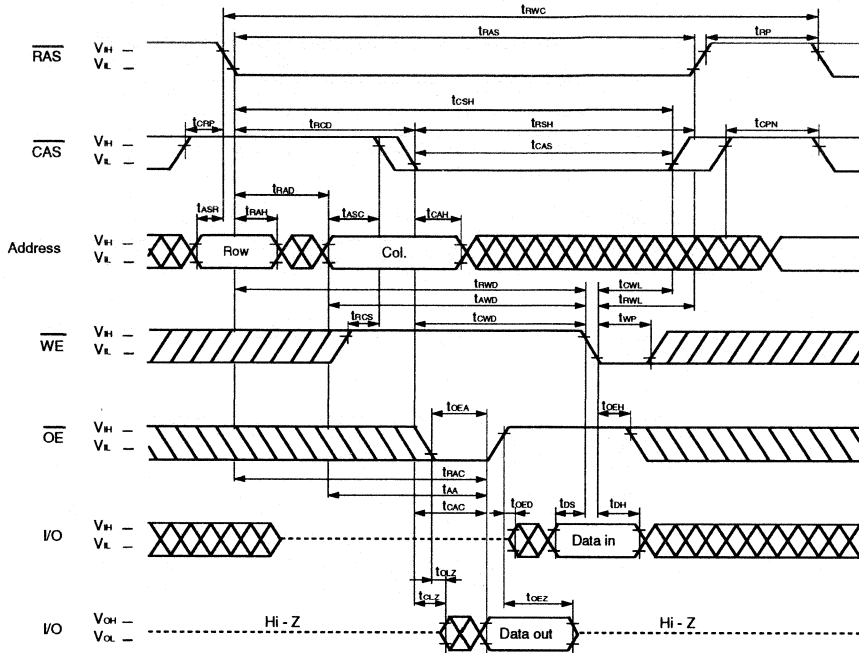
$t_{\text{RAD(MAX.)}}$ and $t_{\text{RCD(MAX.)}}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD(MAX.)}}$ and $t_{\text{RCD}} \geq t_{\text{RCD(MAX.)}}$ will not cause any operation problems.

11. Loading conditions are 1 TTLs and 100 pF.
12. $t_{\text{OFF(MAX.)}}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $t_{\text{CRP(MIN.)}}$ requirement should be applied to $\overline{\text{RAS}} / \overline{\text{CAS}}$ cycles.
14. Either $t_{\text{RCH(MIN.)}}$ or $t_{\text{RRH(MIN.)}}$ should be met in read cycles.
15. $t_{\text{WP(MIN.)}}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{\text{WCH(MIN.)}}$ should be met.
16. $t_{\text{DS(MIN.)}}$ and $t_{\text{DH(MIN.)}}$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
17. If $t_{\text{WCS}} \geq t_{\text{WCS(MIN.)}}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD(MIN.)}}$, $t_{\text{CWD}} \geq t_{\text{CWD(MIN.)}}$, $t_{\text{AWD}} \geq t_{\text{AWD(MIN.)}}$ and $t_{\text{CPWD}} \geq t_{\text{CPWD(MIN.)}}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

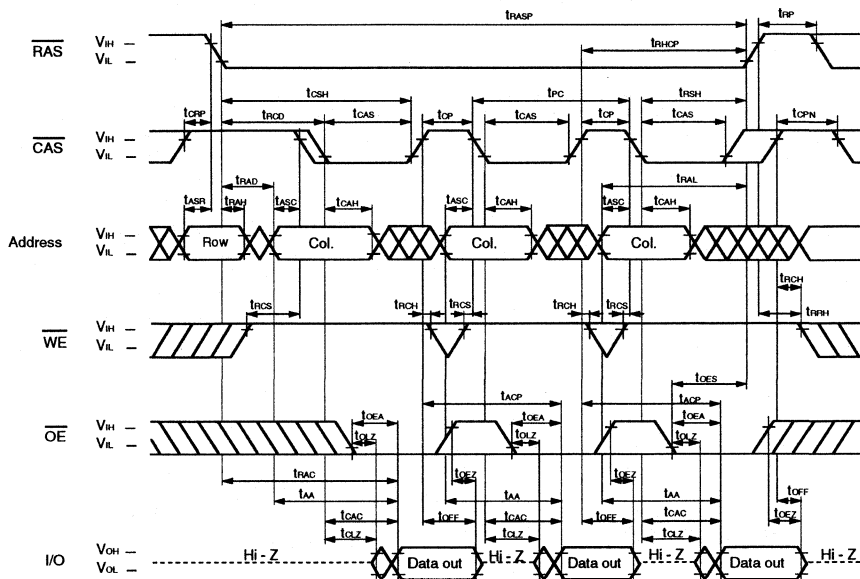
Early Write Cycle

Remark $\overline{\text{OE}}$: Don't care

Read Modify Write Cycle

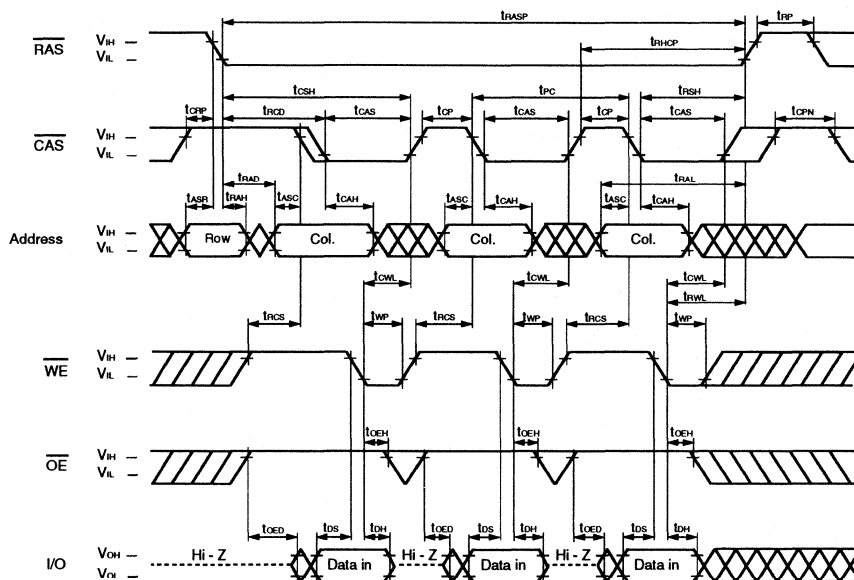


Fast Page Mode Read Cycle

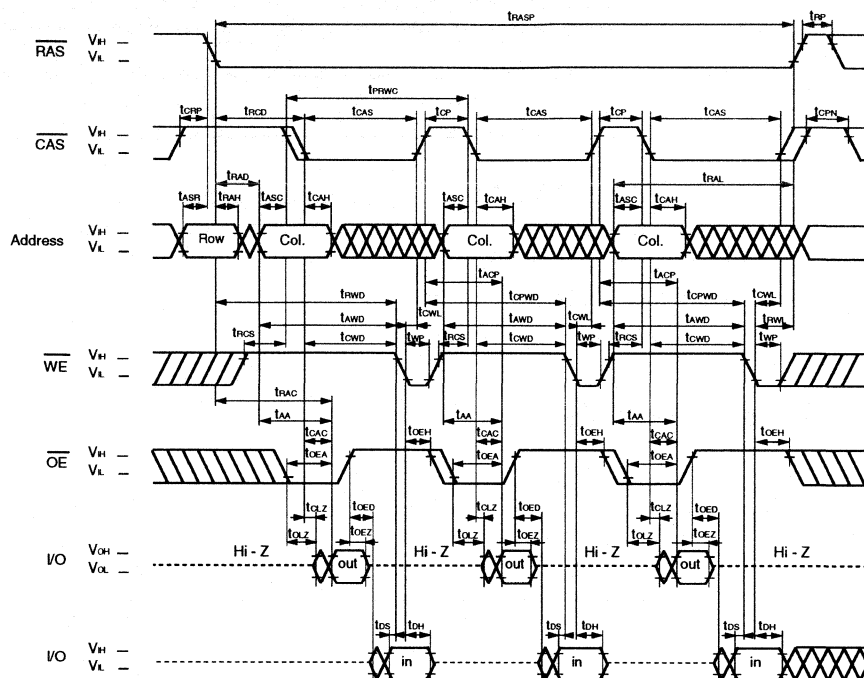


Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Late Write Cycle

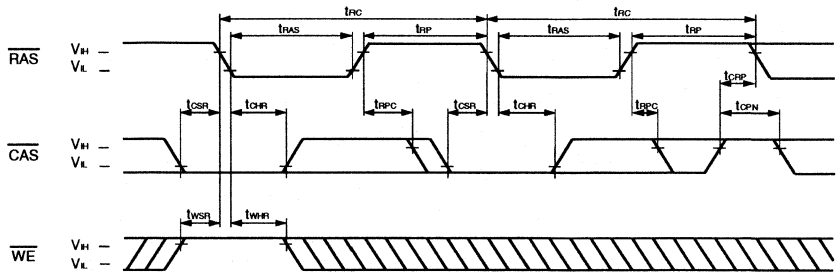


Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.



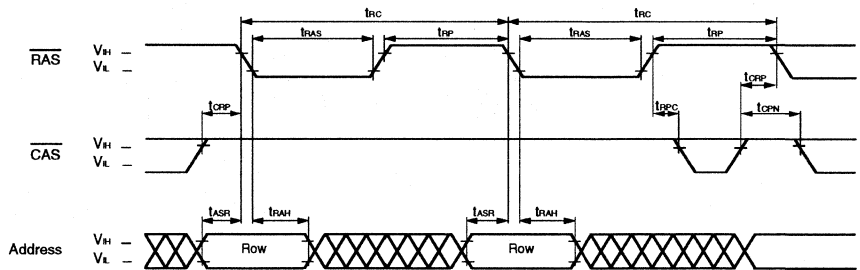
1419

CAS Before RAS Refresh Cycle

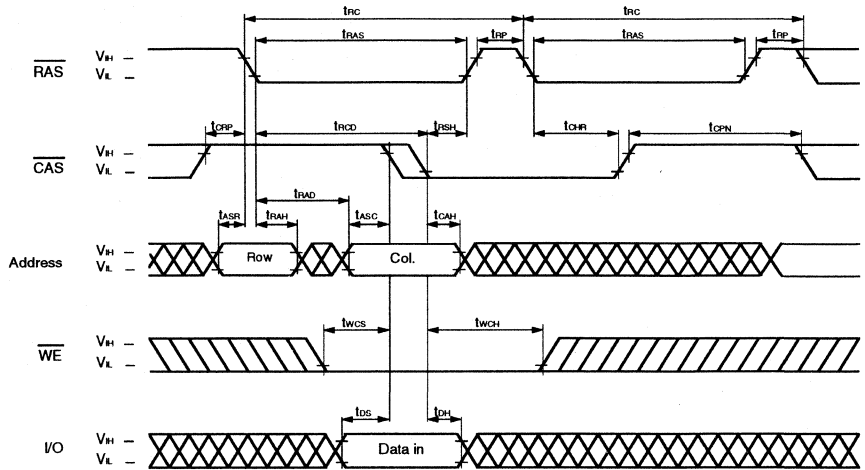


Remark Address, $\overline{OE}$: Don't care I/O : Hi - Z

RAS Only Refresh Cycle

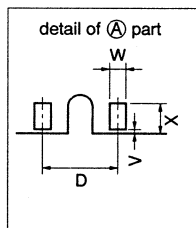
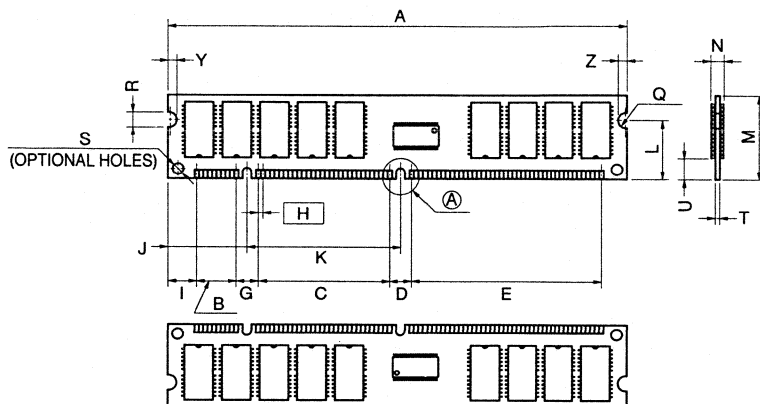


Remark $\overline{WE}, \overline{OE}$: Don't care I/O : Hi - Z

Hidden Refresh Cycle (Write)

Remark OE : Don't care

Package Drawing



ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	43.18	1.700
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A3

3.3 V OPERATION 2M -WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-422000LAB72F is a 2 097 152 words by 72 bits dynamic RAM module on which 9 pieces of 16M DRAM (μ PD 4217800L) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2 097 152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC- 422000AB72-60	60ns	110ns	3.28 w	73.5 mw (CMOS level)
MC- 422000AB72-70	70ns	130ns	2.95 w	
MC- 422000AB72-80	80ns	150ns	2.63 w	

- 2 048 refresh cycles/32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh , $\overline{\text{RAS}}$ only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +3.3 V $\pm$ 0.3V power supply

The information in this document is subject to change without notice.

Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 422000LAB72F-60	60ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of uPD 4217800LG5 (400mil TSOP) [Double side]
MC- 422000LAB72F-70	70ns		
MC- 422000LAB72F-80	80ns		

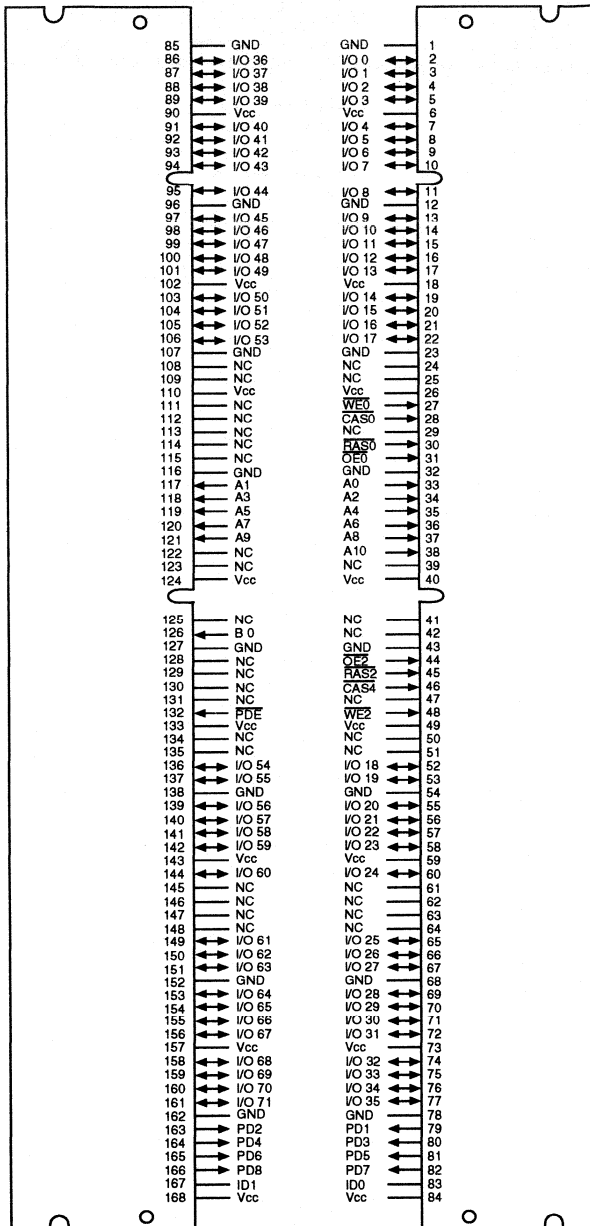
Quality grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



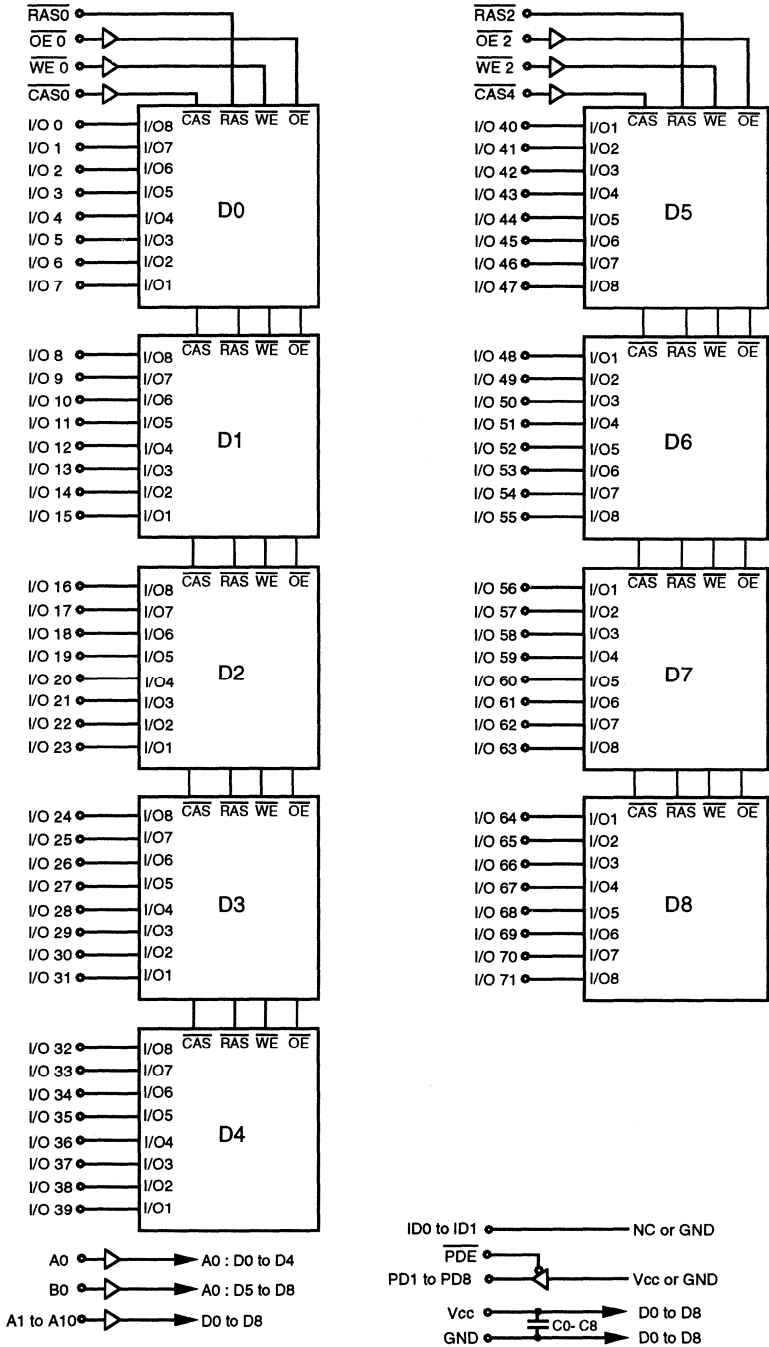
PD and ID Table

Pin Name	Pin No.	Access Time		
		60ns	70ns	80ns
PD1	79	H	H	H
PD2	163	L	L	L
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

(Note) H : VOH, L : VOL

A0 - A10, B0 : Address Inputs
 I/O 0-I/O 71 : Data Inputs / Outputs
 RAS0, RAS2 : Row Address Strobe
 CAS0, CAS4 : Column Address Strobe
 WE0, WE2 : Write Enable
 OE0, OE2 : Output Enable
 PDE : Presence Detect Enable
 PD1- PD8 : Presence Detect Pins
 ID0, ID1 : Identity pins
 Vcc : Power Supply
 GND : Ground
 NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-0.5 to +6.4	V
Supply voltage	VCC		-0.5 to +6.4	V
Output current	IO		20	mA
Power dissipation	PD		11	W
Operating temperature	T _{opt}		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES : 1, 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		3.0	3.3	3.6	V
High level input voltage	VIH		2.0		V _{CC} + 0.3	V
Low level input voltage	VIL		-0.3		+0.8	V
Ambient temperature	T _a		0		70	°C

CAPACITANCE (T_a=25°C , f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C I 1	A0 - A10, B0			20	pF
	C I 2	$\overline{\text{WE}} 0, \overline{\text{WE}} 2$			20	pF
	C I 3	$\overline{\text{RAS}} 0, \overline{\text{RAS}} 2$			50	pF
	C I 4	$\overline{\text{CAS}} 0, \overline{\text{CAS}} 4$			20	pF
	C I 5	$\overline{\text{OE}} 0, \overline{\text{OE}} 2$			20	pF
Data Input/ Output capacitance	C I/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS**(Recommended Operating Conditions unless otherwise noted)**

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	I _{cc1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}}=t_{\text{RC}}(\text{MIN.}), \text{IO}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		910	mA	3,4,7
			$t_{\text{RAC}}=70\text{ns}$		820		
			$t_{\text{RAC}}=80\text{ns}$		730		
Standby Current	I _{cc2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$			28	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}}-0.2\text{V}$			14		
$\overline{\text{RAS}}$ only refresh current	I _{cc3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}$ $t_{\text{RC}}=t_{\text{RC}}(\text{MIN.}), \text{IO}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		910	mA	3,4,5,7
			$t_{\text{RAC}}=70\text{ns}$		820		
			$t_{\text{RAC}}=80\text{ns}$		730		
Operating Current (Fast Page Mode)	I _{cc4}	$\overline{\text{RAS}} \leq V_{\text{IL}}, \overline{\text{CAS}}$ Cycling $t_{\text{PC}}=t_{\text{PC}}(\text{MIN.}), \text{IO}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		640	mA	3,4,6
			$t_{\text{RAC}}=70\text{ns}$		550		
			$t_{\text{RAC}}=80\text{ns}$		460		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{cc5}	$t_{\text{RC}}=t_{\text{RC}}(\text{MIN.})$ $\text{IO}=0\text{mA}$	$t_{\text{RAC}}=60\text{ns}$		910	mA	3,4
			$t_{\text{RAC}}=70\text{ns}$		820		
			$t_{\text{RAC}}=80\text{ns}$		730		
Input Leakage Current	I _{I(L)}	V _I =0 to 3.6V all other pins not under test = 0V	$\overline{\text{RAS}}$	-5	+5	μA	
			others	-5	+1		
Output Leakage Current	I _{O(L)}	Outputs are disabled (Hi - Z) V _O =0 to 3.6V		-5	+5	μA	
High level output voltage	V _{OH}	IO=-2.0mA		2.4		V	
Low level output voltage	V _{OL}	IO=+2.0mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

PARAMETER	SYMBOL	t _{RAC} = 60ns		t _{RAC} = 70ns		t _{RAC} = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	110	-	130	-	150	-	ns	
Read Modify Write Cycle Time	t _{RWC}	173	-	195	-	215	-	ns	
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40	-	45	-	50	-	ns	
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	85	-	90	-	100	-	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	-	60	-	70	-	80	ns	10,11
Access Time from $\overline{\text{CAS}}$	t _{CAC}	-	20	-	23	-	25	ns	10,11
Access Time from Column Address	t _{AA}	-	35	-	40	-	45	ns	10,11
Access Time from CAS Precharge	t _{ACP}	-	40	-	45	-	50	ns	11
Access Time from $\overline{\text{OE}}$	t _{OEa}	-	15	-	18	-	20	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0	-	0	-	0	-	ns	11
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0	-	0	-	0	-	ns	11
Output Buffer Turn-off Delay Time($\overline{\text{CAS}}$)	t _{OFF}	0	13	0	15	0	15	ns	12
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	13	-	15	-	15	-	ns	
Output Buffer Turn-off Delay Time($\overline{\text{OE}}$)	t _{OEZ}	0	13	0	15	0	15	ns	12
$\overline{\text{OE}}$ Command Hold Time	t _{OEh}	0	-	0	-	0	-	ns	
$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ inactive Setup Time	t _{OES}	0	-	0	-	0	-	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	-	50	-	60	-	ns	
$\overline{\text{RAS}}$ Pulse Width(Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	-	18	-	20	-	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10 000	18	10 000	20	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60	-	70	-	80	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	45	20	50	25	60	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	-	5	-	5	-	ns	13
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10	-	10	-	10	-	ns	
$\overline{\text{CAS}}$ Precharge Time(Fast Page Mode)	t _{CP}	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5	-	5	-	5	-	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40	-	45	-	50	-	ns	
Row Address Set Up Time	t _{ASR}	5	-	5	-	5	-	ns	
Row Address Hold Time	t _{RAH}	10	-	10	-	12	-	ns	
Column Address Set Up Time	t _{ASC}	0	-	0	-	0	-	ns	
Column Address Hold Time	t _{CAH}	15	-	15	-	15	-	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30	-	35	-	40	-	ns	
Lead Command Setup Time	t _{RCS}	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0	-	0	-	0	-	ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0	-	0	-	0	-	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	10	-	10	-	15	-	ns	15

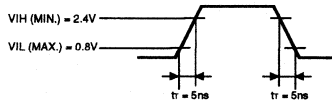
(2/2)

PARAMETER	SYMBOL	t _{RAC} = 60ns		t _{RAC} = 70ns		t _{RAC} = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Command Set-Up Time	t _{WP}	10	-	10	-	15	-	ns	15
Data-in Setup Time	t _{DS}	0	-	0	-	0	-	ns	16
Data-in Hold Time	t _{DH}	10	-	15	-	15	-	ns	16
Write Command Setup Time	t _{WCS}	0	-	0	-	0	-	ns	17
CAS to $\overline{\text{WE}}$ Delay Time	t _{CWD}	38	-	43	-	45	-	ns	17
RAS to $\overline{\text{WE}}$ Delay Time	t _{RWD}	93	-	105	-	115	-	ns	17
CAS Precharge Delay Time Referenced to $\overline{\text{WE}}$ (Fast Page Mode)	t _{CPWD}	58	-	65	-	70	-	ns	17
Column Address Delay Time Referenced to $\overline{\text{WE}}$	t _{AWD}	58	-	65	-	70	-	ns	17
Write Command Lead Time Referenced to RAS	t _{RWL}	25	-	25	-	25	-	ns	
Write Command Lead Time Referenced to CAS	t _{CWL}	15	-	15	-	15	-	ns	
CAS Setup Time for $\overline{\text{CAS}}$ before RAS Refresh	t _{CSR}	5	-	5	-	5	-	ns	
CAS Hold Time for $\overline{\text{CAS}}$ before RAS Refresh	t _{CHR}	10	-	10	-	10	-	ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10	-	10	-	10	-	ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15	-	15	-	15	-	ns	
Refresh Time	t _{REF}	-	32	-	32	-	32	ms	

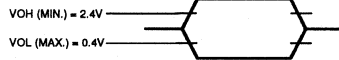
Notes:

1. All voltages are referenced to GND .
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. t_{CC1} , t_{CC3} , t_{CC4} and t_{CC5} depend on cycle rates (t_{AC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. t_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. t_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. t_{CC1} and t_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{IL(\text{MAX})}$ and $\overline{\text{CAS}} \leq V_{IH(\text{MIN})}$.
8. AC measurements assume $t_r = 5\text{ns}$.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



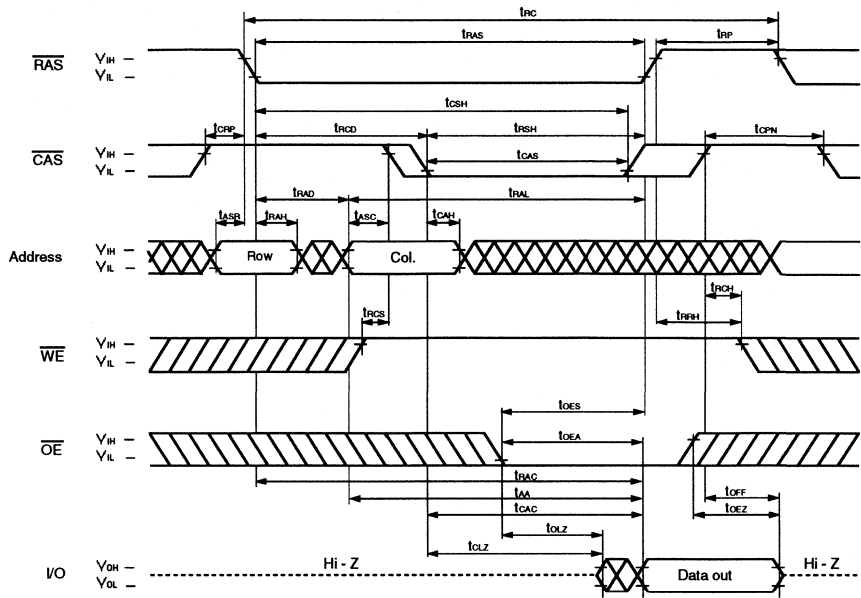
10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \leq t_{\text{RCD}(\text{MAX})}$	$t_{\text{RAC}(\text{MAX})}$	$t_{\text{RAC}(\text{MAX})}$
$t_{\text{RAD}} > t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \leq t_{\text{RCD}(\text{MAX})}$	$t_{\text{AA}(\text{MAX})}$	$t_{\text{RAD}} + t_{\text{AA}(\text{MAX})}$
$t_{\text{RCD}} > t_{\text{RCD}(\text{MAX})}$	$t_{\text{CAC}(\text{MAX})}$	$t_{\text{RCD}} + t_{\text{CAC}(\text{MAX})}$

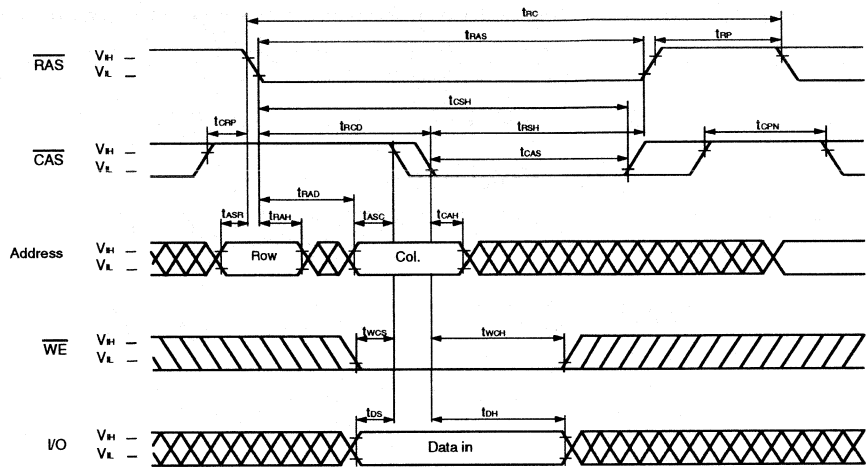
$t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}(\text{MAX})}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \leq t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \leq t_{\text{RCD}(\text{MAX})}$ will not cause any operation problems.

11. Loading conditions are 1 TTLs and 100 pF.
12. $t_{\text{OFF}(\text{MAX})}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $t_{\text{CRP}(\text{MIN})}$ requirement should be applied to $\overline{\text{RAS}} / \overline{\text{CAS}}$ cycles.
14. Either $t_{\text{RCH}(\text{MIN})}$ or $t_{\text{RRH}(\text{MIN})}$ should be met in read cycles.
15. $t_{\text{WP}(\text{MIN})}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{\text{WCH}(\text{MIN})}$ should be met.
16. $t_{\text{DS}(\text{MIN})}$ and $t_{\text{DH}(\text{MIN})}$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
17. If $t_{\text{WCS}} \leq t_{\text{WCS}(\text{MIN})}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle . If $t_{\text{RW}} \leq t_{\text{RW}(\text{MIN})}$, $t_{\text{CWD}} \leq t_{\text{CWD}(\text{MIN})}$, $t_{\text{AWD}} \leq t_{\text{AWD}(\text{MIN})}$ and $t_{\text{CPWD}} \leq t_{\text{CPWD}(\text{MIN})}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Read Cycle

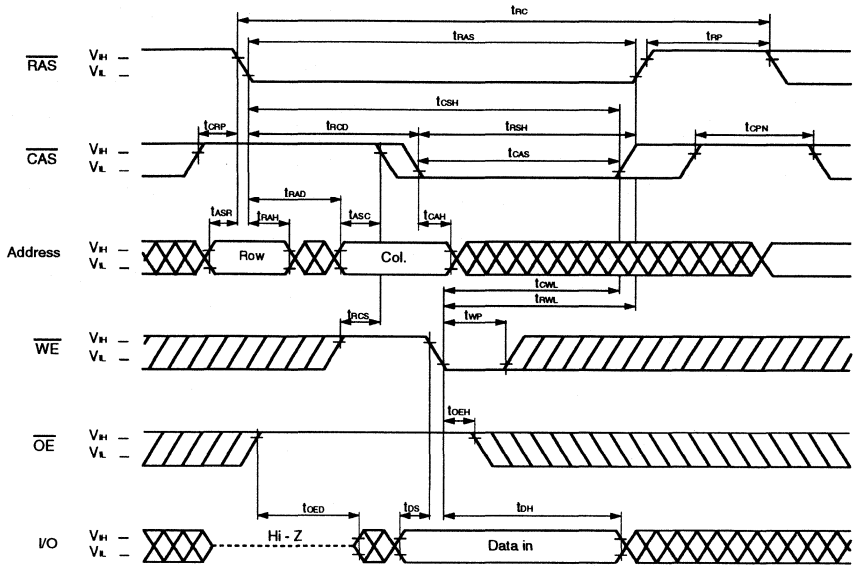


Early Write Cycle

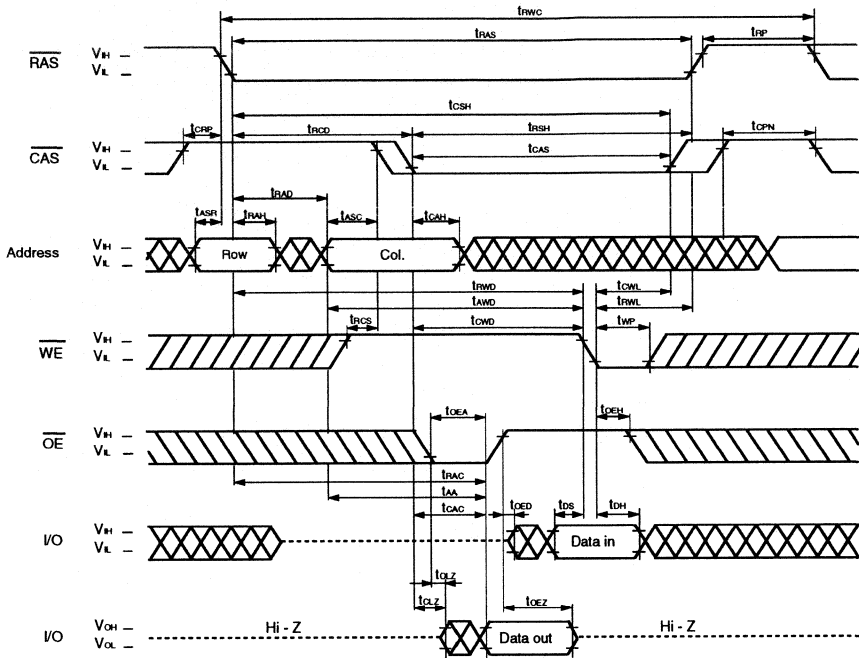


Remark $\overline{\text{OE}}$: Don't care

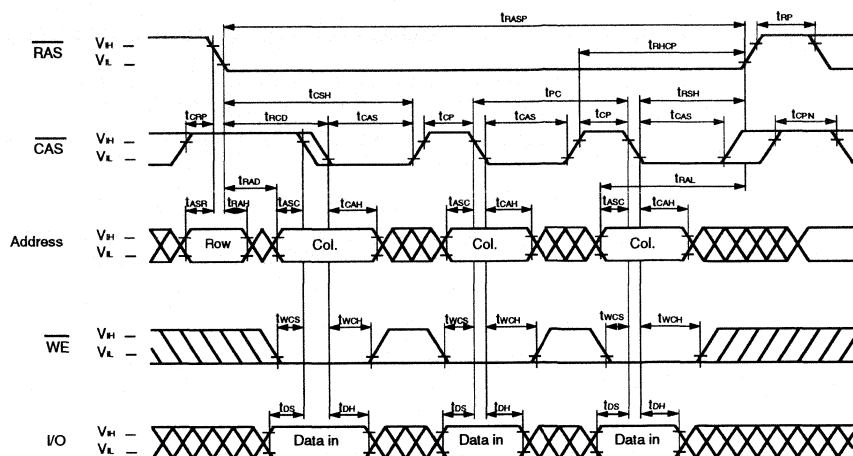
Late Write Cycle



Read Modify Write Cycle



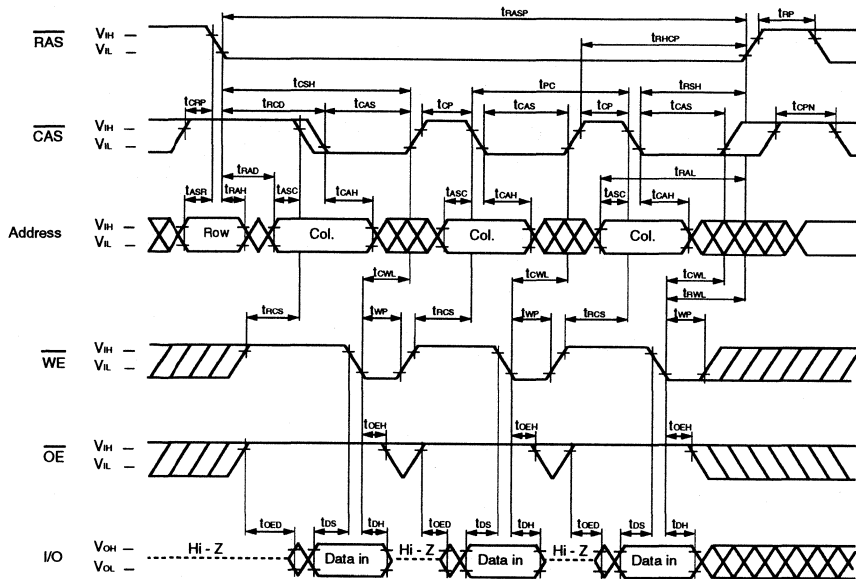
Fast Page Mode Early Write Cycle



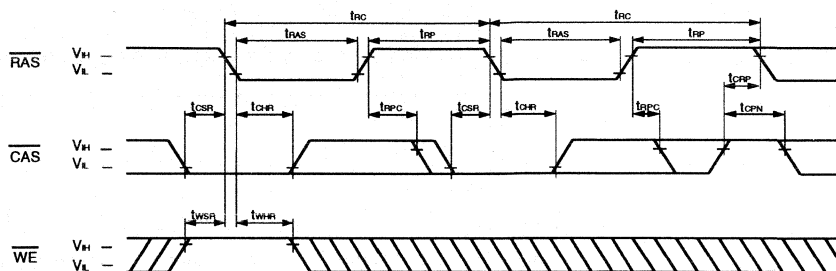
Remark $\overline{OE}$: Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

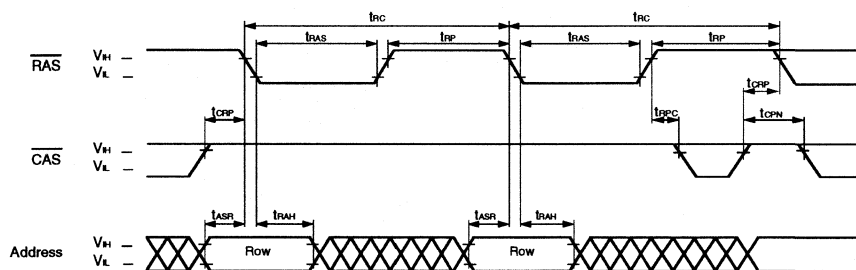
Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

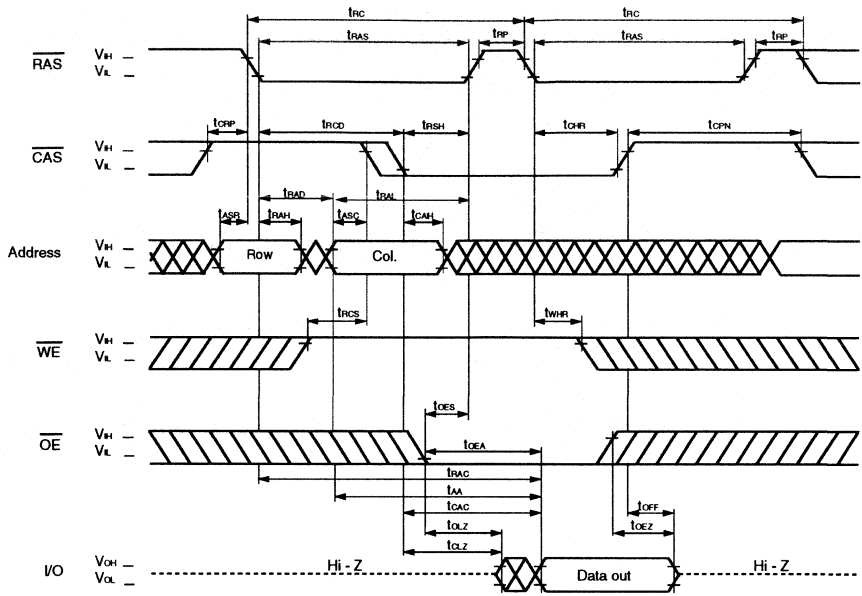
CAS Before RAS Refresh Cycle

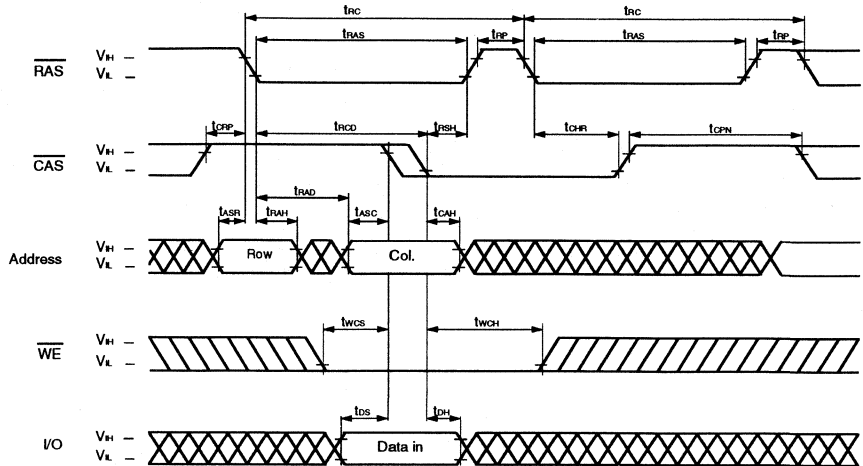
Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi - Z

RAS Only Refresh Cycle

Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O: Hi - Z

Hidden Refresh Cycle (Read)

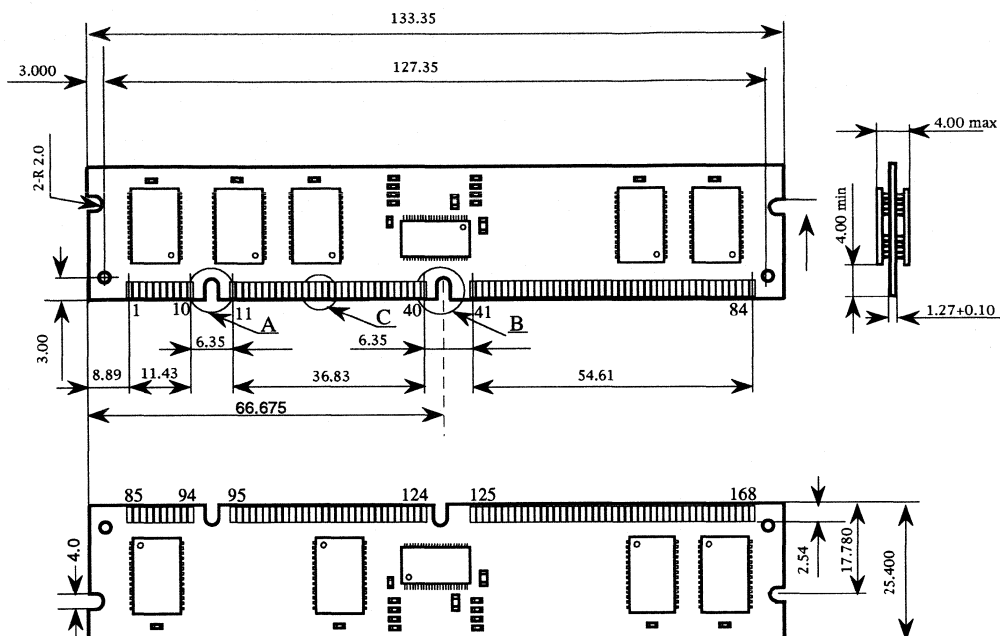


Hidden Refresh Cycle (Write)

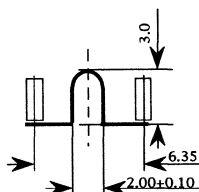
Remark OE : Don't care

Package Drawing

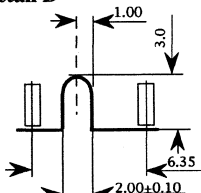
UNIT: mm



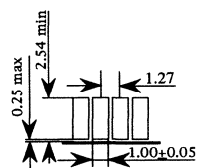
Detail A



Detail B



Detail C



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